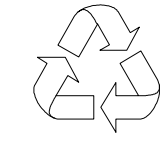
V58LA System

Service Guide



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About this Manual

Purpose

This service guide aims to furnish technical information to the service engineers and advanced users when upgrading, configuring, or repairing the V58LA system.

Manual Structure

This service guide consists of three chapters and four appendices as follows:

Chapter 1 System Introduction

This chapter gives the technical specifications for the V58LA system and its peripherals.

Chapter 2 Major Chipsets

This chapter lists the major chips used in the system and includes pin descriptions and related diagrams of these chips.

Chapter 3 BIOS Setup Information

This chapter includes the system BIOS information, focusing on the BIOS setup utility.

Appendix A Model Number Definition

This appendix describes each parameter in the model number.

Appendix B Spare Parts List

This appendix lists the spare parts for the system board with their part numbers and other information.

Appendix C Schematics

This appendix contains the schematic diagrams for the system board.

Appendix D BIOS POST Check Points

This appendix lists and describes the BIOS POST check points.

Conventions

The following are the conventions used in this manual:

`Text entered by user`	Represents text input by the user.
`Screen messages`	Denotes actual messages that appear onscreen.
a, e, s, etc.	Represent the actual keys that you have to press on the keyboard.

NOTE
Gives bits and pieces of additional information related to the current topic.

WARNING
Alerts you to any damage that might result from doing or not doing specific actions.

CAUTION
Gives precautionary measures to avoid possible hardware or software problems.

IMPORTANT
Reminds you to do specific actions relevant to the accomplishment of procedures.

TIP
Tells how to accomplish a procedure with minimum steps through little shortcuts.

Table of Contents

Chapter 1 System Introduction

Chapter 2 Major Chipsets

Chapter 3 BIOS Setup Information

List of Figures

List of Tables

System Introduction

1.1. Overview

The V58LA is an all-in-one Pentium-based system board that utilizes the PCI local bus architecture. It is capable of offering multimedia and network functions by simply integrating a VGA controller with 3D support, a Sound Blaster-compatible audio chip, and a Fast Ethernet controller.

The system memory is expandable to 256 MB via two onboard 168-pin DIMM (double in-line memory module) sockets. To further enhance system performance, the board also comes with 256/512-KB pipelined-burst second-level cache and 1/2/4-MB video memory.

Standard onboard I/O interfaces comprise of two UART 16C550 serial ports, a parallel port with Enhanced Parallel Port (EPP)/Extended Capabilities Port (EPP) feature, PS/2 keyboard and mouse ports, and VGA port. Two Universal Serial Bus (USB) interfaces are added to the design to enable the system to support more peripherals. For full multimedia support, video, audio and network interfaces are also provided.

Other special features supported are the Hardware Monitoring and the Wake-on Ring-in functions. For details, read the following sections.

The system is fully compatible with Windows 95, Windows NT, NetWare, MS-DOS V6.X, OS/2, and UNIX operating systems.

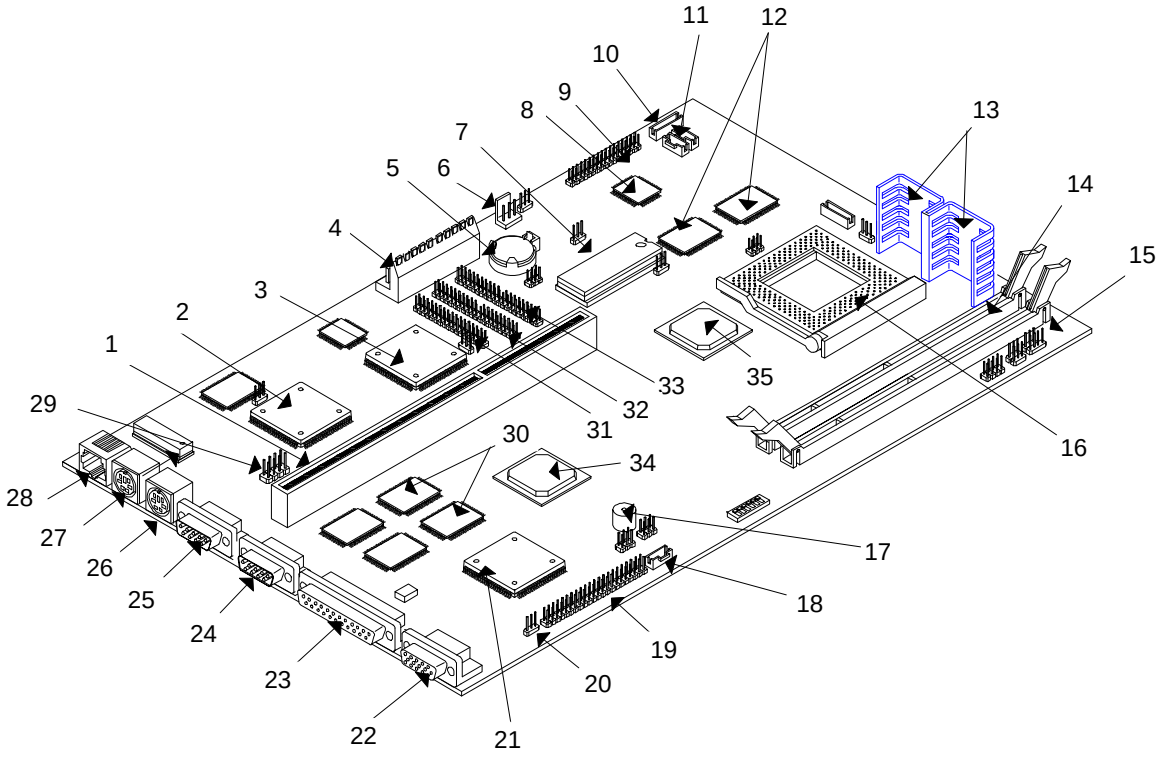
1.1.1 Features

- A ZIF socket that supports 3.3V Intel Pentium P54C/P55C processor running at 90/60, 100/66, 120/60, 133/66, 150/60, 166/66, 200/66, or 233/66 MHz. Also supports Cyrix M1/M2 or AMD K5/K6 processor
- Two 168-pin DIMM sockets that accept SDRAMs with 8, 16, 32, 64, and 128-MB capacities
- 256-MB maximum system memory
- 256 or 512-KB pipelined-burst second-level cache
- Onboard video memory (1/2/4-MB SGRAM)
- One riser card slot for future expansion
- Enhanced PCI local bus IDE controller
- Onboard VGA with 2D/3D support
- Onboard 16-bit PnP audio controller, Sound Blaster-compatible

- Onboard 100Base-TX/10Base-T Ethernet controller with Wake-on LAN solution (optional)
- APM-compliant DMI BIOS
- Ultra I/O controller
- Two 16C550 buffered serial ports and one SPP/ECP/EPP parallel port
- Two USB interfaces, Open HCI 1.0a compliant
- VGA AMC connector to support TV-tuner, MPEG and H/W capture
- Audio interface, includes fax/modem and CD-audio
- Fast Ethernet interface
- PS/2 mouse and keyboard interface

1.2. Board Layout

1.2.1 System Board



1 Riser card slot
2 Ultra I/O controller (SMC 37C935APM)
3 LAN controller (Intel S82557)
4 Power connector
5 RTC Battery
6 Standby connector
7 BIOS chip
8 Audio controller (Creative CT2510)
9 AIO board connector
10 Fax/modem connector
11 CD-in and Line-in connectors
12 Pipelined-burst cache
13 Voltage regulators with heatsink
14 DIMM sockets
15 Reset switch connector
16 CPU socket
17 Buzzer
18 INT line-in connector
19 AMC connector
20 Modem ring-in connector
21 Video controller (ATI 264GT RAGE II+)
22 Video port
23 Printer port
24 COM2/USB port
25 COM1 port
26 PS/2 mouse port
27 PS/2 keyboard
28 LAN port
29 USB board connector
30 SGRAMs (video memory)
31 Floppy disk drive connector
32 IDE 2 connector
33 IDE 1 connector
34 PCI-to-ISA bus bridge (ALI M1533)
35 Host bus-to-PCI bus bridge (ALI M1531)

Figure 1-1 System Board Layout

1.2.2 Slot Boards

The system board comes with a slot board already installed. The slot board carries the PCI and ISA bus slots for system enhancements and future expansion.

The slot board may vary in size and layout depending on your system housing. Figures 1-2 to 1-6 show the available slot board types.

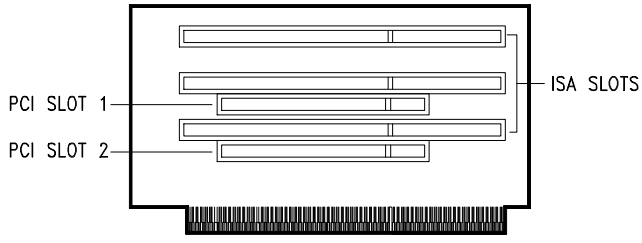


Figure 1-2 2-PCI/3-ISA Slot Board (for desktop systems)

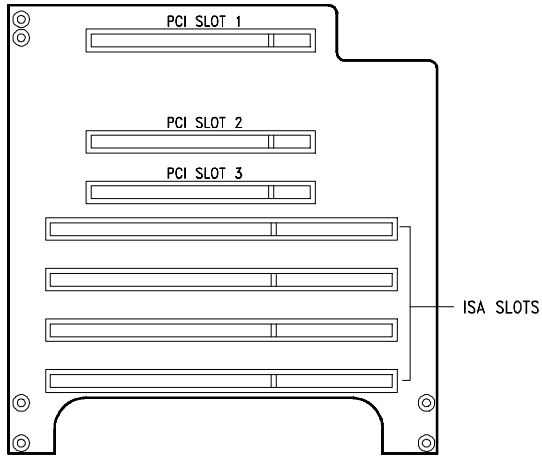


Figure 1-3 3-PCI/4-ISA Slot Board (for minitower systems)

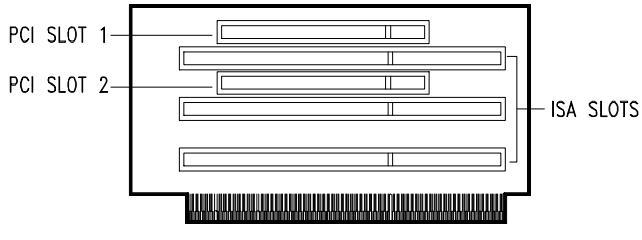


Figure 1-4 2-PCI/3-ISA Slot Board (for Aspire desktop systems)

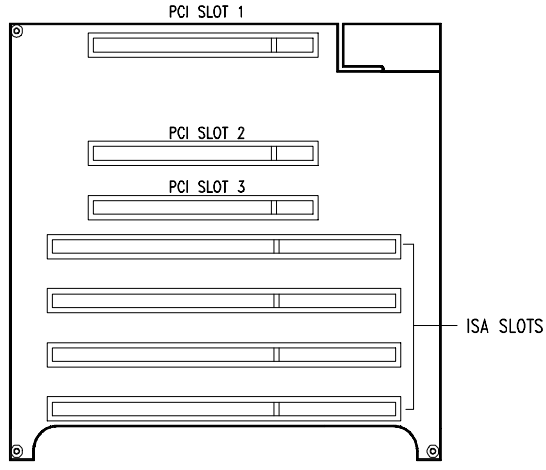


Figure 1-5 3-PCI/4-ISA Slot Board (for Aspire minitower systems)

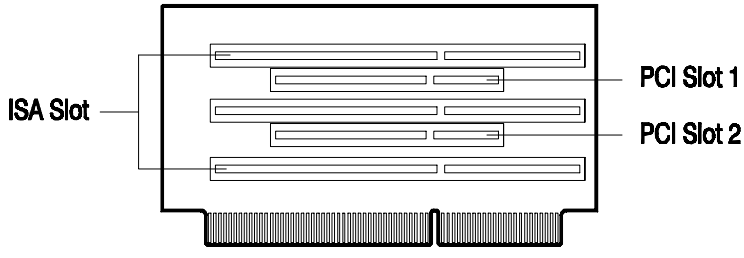


Figure 1-6 3-ISA Slot Board (for AcerBasic system)

Refer to the corresponding housing manual for slot board installation instructions.

1.3. Specifications

Table 1-1 Specifications

Item	Description
CPU	3.3V Intel Pentium P54C/P55C running at 90/60, 100/66, 120/60, 133/66, 150/60, 166/66, 200/66, or 233/66 MHz Cyrix M1/M2 or AMD K5/K6 processor
System Memory	256 MB (maximum) Two 168-pin DIMM sockets that accept 8, 16, 32, 64, and 128-MB 3.3V SDRAMs
BIOS	256/512-KB Block Flash ROM 29EE020
Chipset	ALI Aladdin IV M1531/M1533
Audio Controller	Creative CT2510 16-bit PnP
Video Controller	ATI 264GT Rage II+/Rage III (with 1/2/4-MB video SGRAM video memory)
LAN Controller	Intel 82557 (100Base-TX/10Base-T Ethernet with Wake-on LAN support)
I/O Controller	SMC 935APM
Hard Disk Interface	Two embedded PCI bus master type E-IDE interfaces support up to four IDE devices
Floppy Drive Interface	One floppy disk drive interface that supports 2.88/1.44/1.2-MB floppy drives and three-mode floppy disk types
Onboard I/O	One PS/2 keyboard port One PS/2 mouse port Two NS16C550-compatible serial header interfaces One parallel port header interface (SPP) with ECP/EPP support One Universal BUS interface
Real-time Clock Battery	CR2032 lithium battery
Expansion Slots	One riser card
Power Supply	145W switching power supply
Housing	ID2PN, IDABN, Aspire Desktop, Aspire Minitower
Operating System	MS-DOS v6.X, OS/2, UNIX, NetWare, Windows NT, and Windows 95

1.4. Jumpers and Connectors

1.4.1 Jumper and Connector Locations

Figure 1-2 shows the jumper and connector locations.

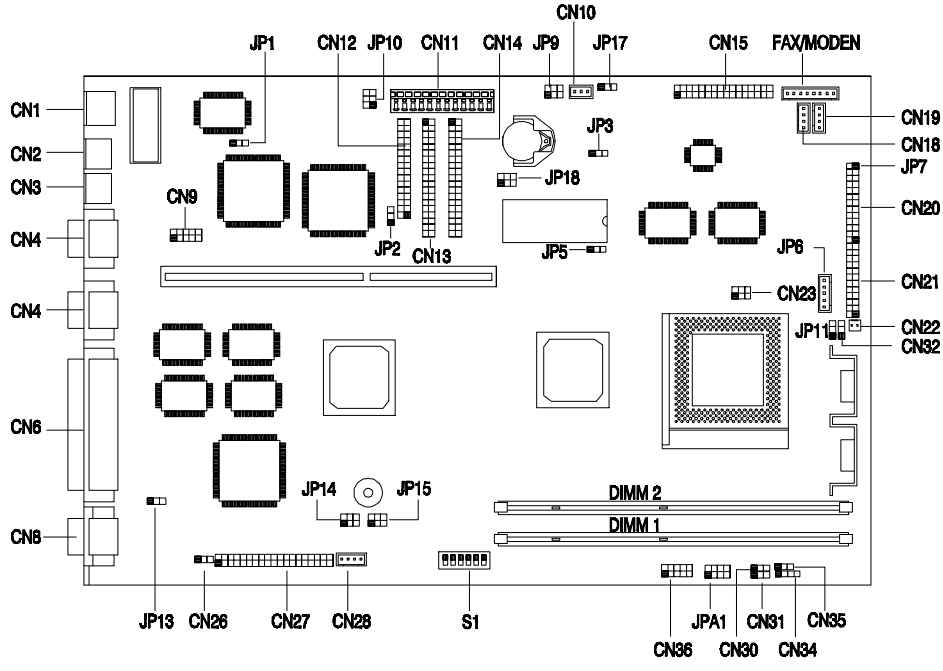


Figure 1-2 Jumper and Connector Locations

The shaded pin indicates pin 1.

1.4.2 Jumper Settings

The following tables list the jumper settings and their corresponding functions:

Table 1-1 Jumper Settings

Jumper	Setting	Function
JP1	1-2 2-3	**BIOS Logo** Acer OEM
JP2	1-2 2-3	**LED Function** for IDE and FDD for IDE only
JP3	1-2 2-3 *	**Suspend/Reset Switch Function** Suspend Reset
JP5	1-2 2-3	**L2 Cache Mode** Intel or Cyrix M1/M2 “1+4” mode Cyrix M1/M2 linear-burst mode
JP10	3-5, 4-6 1-3, 2-4	**Power Supply Type** With standby power current ≥ 1A With standby power current < 1A
CN23	1-3, 2-4 3-5, 4-6	**CPU Voltage Option** Single-voltage CPU (P54C) Dual-voltage CPU (P55C)
CN36	1-2 3-4 5-6 7-8 9-10	**Vcore Select** 2.8V 2.9V 3.2V 3.31V 3.52V
S1	**Switch 1** On Off	**Password Check** Bypass password Check password
S1	**Switch 2** On Off **Switch 3** On Off **Switch 6** On Off	**Onboard Sound** Disabled Enabled **Onboard LAN** Disabled Enabled **Clock Select** Cypress CY2273 Clk 9148

Table 1-2 Host Bus Frequency Select

Jumper	60 MHz	66 MHz	75 MHz	83 MHz
CY2273				
JP14	1-3, 2-4	1-3, 2-4	3-5, 4-6	3-5, 4-6
JP15	1-3, 2-4	3-5, 4-6	1-3, 2-4	3-5, 4-6

Table 1-3 CPU/Host Bus Frequency Ratio Select

JP11	S1		CPU/Host Bus Frequency Ratio		
	switch 4	switch 5	Intel	AMD	Cyrix
2-3	On	On	2.5	2.5	2.5
2-3	Off	Off	1.5/3.5	1.5/3.5	3.5
2-3	Off	On	2.0	2.0	2.0
2-3	On	Off	3.0	3.0	3.0
1-2	Off	On		4.0	
1-2	On	On		4.5	

Table 1-4 CPU Type and Frequency Select

CPU Freq. (MHz)	JP11	JP14	JP15	S1 switch 4	S1 switch 5	CN23	CN36
Intel P54C							
P90	2-3	1-3, 2-4	1-3, 2-4	Off	Off	1-3, 2-4	7-8
P100	2-3	1-3, 2-4	3-5, 4-6	Off	Off	1-3, 2-4	7-8
P120	2-3	1-3, 2-4	1-3, 2-4	Off	On	1-3, 2-4	7-8
P133	2-3	1-3, 2-4	3-5, 4-6	Off	On	1-3, 2-4	7-8
P150	2-3	1-3, 2-4	1-3, 2-4	On	On	1-3, 2-4	7-8
P166	2-3	1-3, 2-4	3-5, 4-6	On	On	1-3, 2-4	7-8
P200	2-3	1-3, 2-4	3-5, 4-6	On	Off	1-3, 2-4	7-8
Intel P55C							
P150	2-3	1-3, 2-4	1-3, 2-4	On	On	3-5, 4-6	1-2
P166	2-3	1-3, 2-4	3-5, 4-6	On	On	3-5, 4-6	1-2
P200	2-3	1-3, 2-4	3-5, 4-6	On	Off	3-5, 4-6	1-2
P233	2-3	1-3, 2-4	3-5, 4-6	Off	Off	3-5, 4-6	1-2
Cyrix M1 (6x86)							
P150+	2-3	1-3, 2-4	1-3, 2-4	Off	On	1-3, 2-4	7-8
P166+	2-3	1-3, 2-4	3-5, 4-6	Off	On	1-3, 2-4	7-8
P200+	2-3	3-5, 4-6	1-3, 2-4	Off	On	1-3, 2-4	7-8
Cyrix M1 (6x86L)							
P150+	2-3	1-3, 2-4	1-3, 2-4	Off	On	3-5, 4-6	1-2
P166+	2-3	1-3, 2-4	3-5, 4-6	Off	On	3-5, 4-6	1-2
P200+	2-3	3-5, 4-6	1-3, 2-4	Off	On	3-5, 4-6	1-2
Cyrix MX							
PR166	2-3	1-3, 2-4	1-3, 2-4	On	On	3-5, 4-6	3-4
PR200	2-3	1-3, 2-4	3-5, 4-6	On	On	3-5, 4-6	3-4
PR233	2-3	3-5, 4-6	1-3, 2-4	On	On	3-5, 4-6	3-4
AMD K5							
PR90	2-3	1-3, 2-4	1-3, 2-4	Off	Off	1-3, 2-4	9-10
PR100	2-3	1-3, 2-4	3-5, 4-6	Off	Off	1-3, 2-4	9-10
PR120	2-3	1-3, 2-4	1-3, 2-4	Off	On	1-3, 2-4	9-10

CPU Freq. (MHz)	JP11	JP14	JP15	S1 switch 4	S1 switch 5	CN23	CN36
PR133	2-3	1-3, 2-4	3-5, 4-6	Off	On	1-3, 2-4	9-10
PR166	2-3	1-3, 2-4	3-5, 4-6	On	On	1-3, 2-4	9-10
AMD K6							
PR166	2-3	1-3, 2-4	3-5, 4-6	On	On	3-5, 4-6	5-6
PR200	2-3	1-3, 2-4	3-5, 4-6	On	Off	3-5, 4-6	5-6
PR233	2-3	1-3, 2-4	3-5, 4-6	Off	Off	3-5, 4-6	5-6

1.4.3 Onboard Connectors

Table 1-5 lists the onboard connectors.

Table 1-5 Onboard Connectors

Connector	Function
CN1	Ethernet connector
CN2	PS/2 keyboard port
CN3	PS/2 mouse port
CN4	COM1 port
CN6	COM2 port (USB port - optional)
CN7	Printer port
CN8	Monitor port
CN9	USB board connector
CN10	Standby power connector
CN11	Power connector
CN12	Floppy disk drive connector
CN13	IDE 2 connector
CN14	IDE 1 connector
CN15	AIO board connector
CN18	CD-in connector
CN19	Line-in connector
CN22	Two-pin fan connector
CN26	Modem ring-in connector
CN27	AMC connector
CN28	Auxiliary line-in connector (for add-on card)
CN30	Power LED connector
CN31	Message-in LED/HDD LED connector
CN32	Power button connector
CN34	External speakers connector
CN35	Reset/Suspend switch connector
JPA1 2-4 7-8	 Turbo LED connector Power button connector (for Aspire 6-pin connector

1.5. Hardware Configurations

1.5.1 Memory Configurations

The system memory is upgradable to a maximum of 256 MB via two 168-pin DIMM sockets onboard. These DIMM sockets accept 8, 16, 32, 64, and 128-MB, 3.3V SDRAMs. See Figure 1-1 for the location of the DIMM sockets.

Table 1-6 lists the possible memory configurations.

Table 1-6 Memory Configurations

DIMM 1	DIMM 2	Total Memory
8 MB		8 MB
	8 MB	8 MB
8 MB	8 MB	16 MB
16 MB		16 MB
	16 MB	16 MB
16 MB	16 MB	32 MB
32 MB		32 MB
	32 MB	32 MB
32 MB	16 MB	48 MB
32 MB	32 MB	64 MB
32 MB	64 MB	96 MB
64 MB		64 MB
	64 MB	64 MB
64 MB	64 MB	128 MB
64 MB	128 MB	192 MB
128 MB	128 MB	256 MB

1.5.2 Second-level Cache Configurations

The board may come with either 256-KB or 512-KB pipelined-burst second-level cache. Refer to the following table for the possible cache configurations.

Table 1-7 Second-level Cache Configurations

Cache Size	Data RAM (12 ns)	Location	Tag RAM (12 ns)	Cacheable Memory
256 KB	32K x 32 x 2 pcs.	U24, U25	32K x 8 x 1 pc	64 MB
512 KB	64K x 32 x 2 pcs.	U24, U25	32K x 8 x 1 pc	64 MB

1.5.3 Video Memory

The system board may come with 1, 2, or 4-MB SGRAM video memory. Larger video memory allows you to display higher resolutions and more colors.

The following table lists the possible video memory configurations.

Table 1-8 Video Memory Configurations

Memory Size	SGRAM	Location
4 MB	256K x 32 x 4 pcs.	U31, U32, U33, U34
2 MB	256K x 32 x 2 pcs.	U33, U34
1 MB	256K x 32 x 1 pc.	U34

1.5.4 Supported Video Resolutions

The following table lists the video resolutions supported by the onboard VGA:

Table 1-9 Supported Video Resolutions

Resolution	bpp	V-Freg. (Hz)	H-Freq. (KHz)	Pixel Clock (MHz)
640 x 480	8/16	60	31.4	25.2
640 x 480	8/16	72	37.5	31.2
640 x 480	8/16	75	37.5	31.5
640 x 480	8/16	90	47.9	39.9
640 x 480	8/16	100	52.9	44.9
800 x 600	8/16	48 *int.*	33.8	36.0
800 x 600	8/16	56	35.1	36.0
800 x 600	8/16	60	37.8	40.0
800 x 600	8/16	70	44.5	44.9
800 x 600	8/16	72	48.0	50.0
800 x 600	8/16	75	46.8	49.5
800 x 600	8	90	57.0	56.6
800 x 600	8	100	62.5	67.5
1024 x 768	8/16	43 *int.*	35.5	44.9
1024 x 768	8/16	60	48.3	65.0
1024 x 768	8/16	70	56.4	75.0
1024 x 768	8/16	72	58.2	75.0
1024 x 768	8/16	75	60.0	78.8
1024 x 768	8/16	90	76.2	100
1024 x 768	8/16	100	79.0	110
1152 x 864	8	43 *int.*	45.8	65.0
1152 x 864	8	60	54.9	80.0
1152 x 864	8	70	66.1	100
1152 x 864	8	75	75.1	110
1280 x 1024	8	43 *int.*	50.0	80.0
1280 x 1024	8	47 *int.*	50.0	80.0

Table 1-9 Supported Video Resolutions

Resolution	bpp	V-Freg. (Hz)	H-Freq. (KHz)	Pixel Clock (MHz)
1280 x 1024	8	60	63.9	110
1280 x 1024	8	70	74.6	126
1280 x 1024	8	72	78.8	130
1280 x 1024	8	75	79.9	135

int. interlaced

1.5.5 Parallel Port Configurations

The onboard parallel port interface supports a 25-pin header. The interface functions in different operation modes and is adjustable to select LPT1, LPT2, and LPT3 by changing the CMOS settings.

Table 1-10 lists the operation mode settings and their corresponding functions.

Table 1-10 Parallel Port Operation Mode Settings

Setting	Function
Standard Parallel Port (SPP)	Allows normal speed one-way operation
Standard and Bidirectional	Allows normal speed operation in a two-way mode
Enhanced Parallel Port (EPP)	Allows bidirectional parallel port operation at maximum speed
Extended Capabilities Port (ECP)	Allows parallel port to operate in bidirectional mode and at a speed higher than the maximum data transfer rate

1.5.6 Serial Port Configurations

The system board has two high-speed 9-pin D-type serial ports. These ports are NS16C550-compatible UARTs with 16-byte FIFO send/receive capability. The port functions are software adjustable to select COM1, COM2, COM3, and COM4.

1.5.7 IDE Interface Configurations

The system board includes PCI enhanced local bus IDE interfaces that accommodate up to four IDE devices. The interfaces function as PCI bus master IDE and support PIO mode 4 and DMA mode 2. The interfaces are fully compatible with ANSIS ATA Rev. 3.0 and ATAPI specifications.

1.5.8 Memory Address Map

Table 1-11 Memory Address Map

Address	Size	Function
0000000 ~ 007FFFF	512 KB	Host memory
0080000 ~ 009FFFF	128 KB	Host/PCI memory
00A0000 ~ 00BFFFF	128 KB	PCI/ISA video buffer memory
00C0000 ~ 00C7FFF	32 KB	Video BIOS memory
00C8000 ~ 00DFFFF	96 KB	ISA card BIOS and buffer memory
0E0000 ~ 00EFFFF	64 KB	BIOS extension memory Setup and POST memory ROM DOS
00F0000 ~ 00FFFFF	64 KB	System BIOS memory
1000000 ~ UPPER LIMIT		Main memory
UPPER LIMIT ~ 4GB		PCI memory

1.5.9 PCI INTx and IDSEL Map

Table 1-12 I/O Address Map

PCI INTx#	Device IDSEL: Address	PCI Device
INTA#	AD31	PCI-Slot 1
INTB#	AD30	PCI-Slot 2
INTC#	AD25	PCI-Slot 3
INTD#	Reserved	Reserved

1.5.10 Interrupt Channels Map

Table 1-13 Interrupt Channels Map

IRQ	System Device
IRQ0	Timer
IRQ1	Keyboard
IRQ2	Cascade interrupt control
IRQ3	Reserved
IRQ4	Serial port 1
IRQ5	Reserved
IRQ6	Floppy drive
IRQ7	Parallel port
IRQ8	Real-time clock
IRQ9	Reserved
IRQ10	Reserved
IRQ11	Reserved
IRQ12	PS/2 mouse

Table 1-13 Interrupt Channels Map

IRQ	System Device
IRQ13	Math coprocessor
IRQ14	IDE channel 1
IRQ15	IDE channel 2

1.5.11 DMA Channels Map

Table 1-14 DMA Channels Map

DRQ	System Device
DRQ0	Reserved
DRQ1	Reserved
DRQ2	Floppy drive
DRQ3	Reserved
DRQ4	Cascade
DRQ5	Reserved
DRQ6	Reserved
DRQ7	Reserved

1.5.12 I/O Address Map

Table 1-15 I/O Address Map

Hex Range	Device
000 ~ 01F	DMA controller 1
020 ~ 03F	Interrupt controller 1
040 ~ 047	System timer
050 ~ 057	System timer
060 ~ 06F	Keyboard controller 8742
070	CMOS RAM address and NMI mask
078 ~ 07B	Real-time clock
080 ~ 09F	DMA page register
0A0 ~ 0BF	Interrupt controller 2
0C0 ~ 0DF	DMA controller 2
0F0	Clear math coprocessor
0F1	Reset math coprocessor
0F8 ~ 0FF	Math coprocessor
1F0 ~ 1F8	Hard disk
278 ~ 27F	Parallel port 2
2F8 ~ 2FF	Serial port 2
378 ~ 37F	Parallel port 1

Table 1-15 I/O Address Map

Hex Range	Device
3F0 ~ 3F7	Floppy disk controller
3F8 ~ 3FF	Serial port 1
OCF8 ~ OCFB	PCI mechanism 1 configuration register
0CF8	PCI mechanism 2 configuration space enable register
0CFA	PCI mechanism 2 forward register
C000 ~ C0FF	M1451C PCI configuration space
C200 ~ C2FF	M1449 PCI configuration space
C100 ~ C1FF	PCI configuration space
C300 ~ CFFF	PCI configuration space

1.6. System Block Diagram

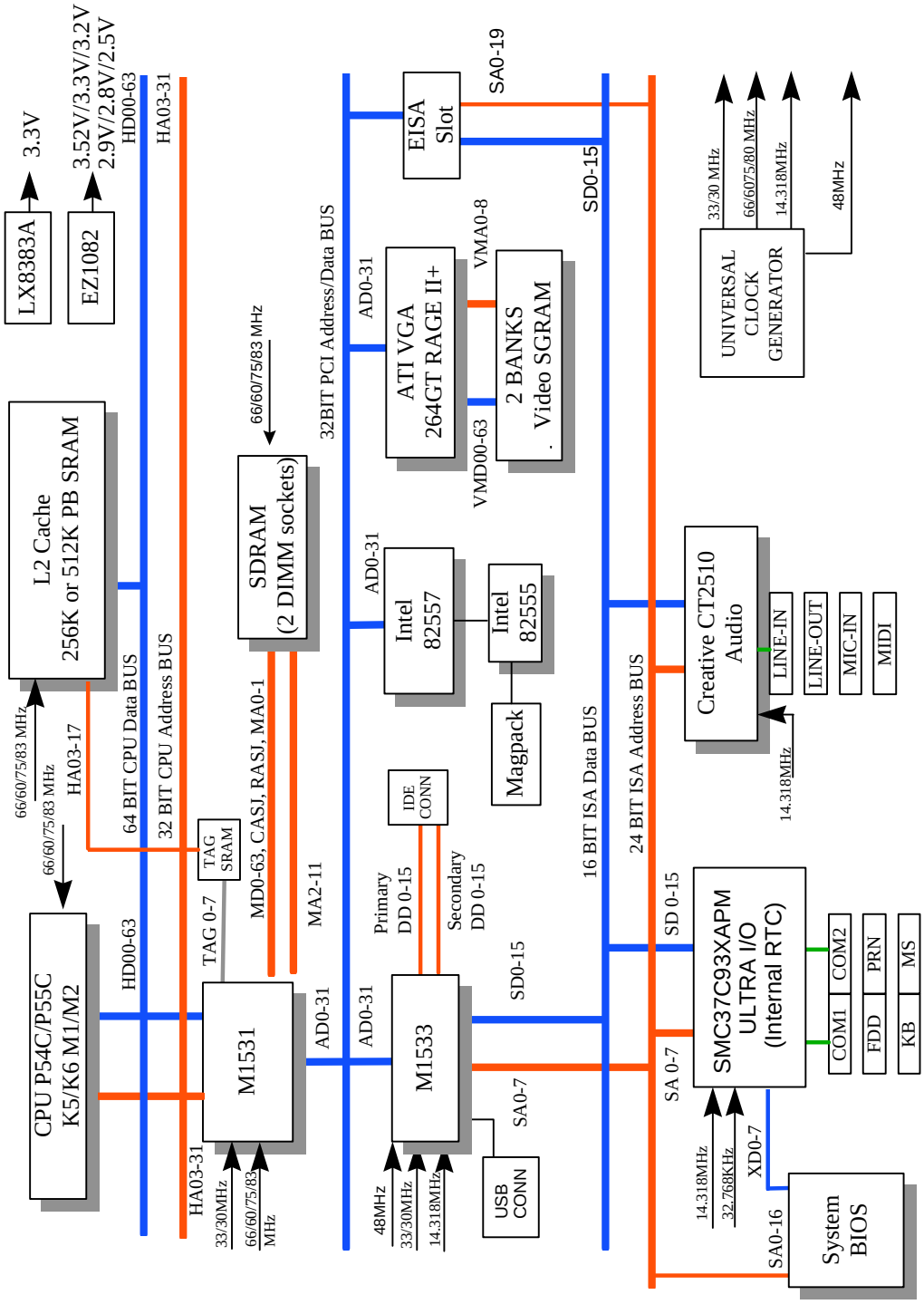


Figure 1-8 System Operation Block Diagram

1.7. Power Management

1.7.1 Power Management Modes

The system has three power management modes: normal mode, IDE hard disk standby mode, and system suspend mode.

1.7.1.1 Normal Mode

The normal operating mode of the system.

1.7.1.2 IDE Hard Disk Standby Mode

The IDE hard disk standby mode that controls ATA power-management-compliant hard disk drives. This feature allows the device to enter into IDE hard disk standby mode after a specified HDD non-activity period, and to return to normal mode immediately after a hard disk access.

The IDE hard disk standby mode has the following features:

- HDD power-management timer (1-15 minutes, time step = 1 minute)
- Allows HDD to go into standby mode (for ATA standard interface)
- Resume method: Any IDE HDD activity

1.7.1.3 System Suspend Mode

This is a fast-on, power-saving mode, allowing the PC to return to full power immediately. It allows the VGA monitor to enter standby mode and turns off the hard disk drive spindle motor. Any system activity returns the system to full power.

The system standby mode has the following features:

- Global power-management timer (1-15 minutes, time step = 1 minute)
- HDD goes into standby mode (for ATA standard interface)
- Disables H-sync and V-sync signals to control the VESA DPMS monitor
- LED on the panel flashes at 1.6-second intervals
- Resume method: Activity from keyboard, mouse, or any IRQ/DRQ enabled in the CMOS

1.7.2 Power Saving Flowchart

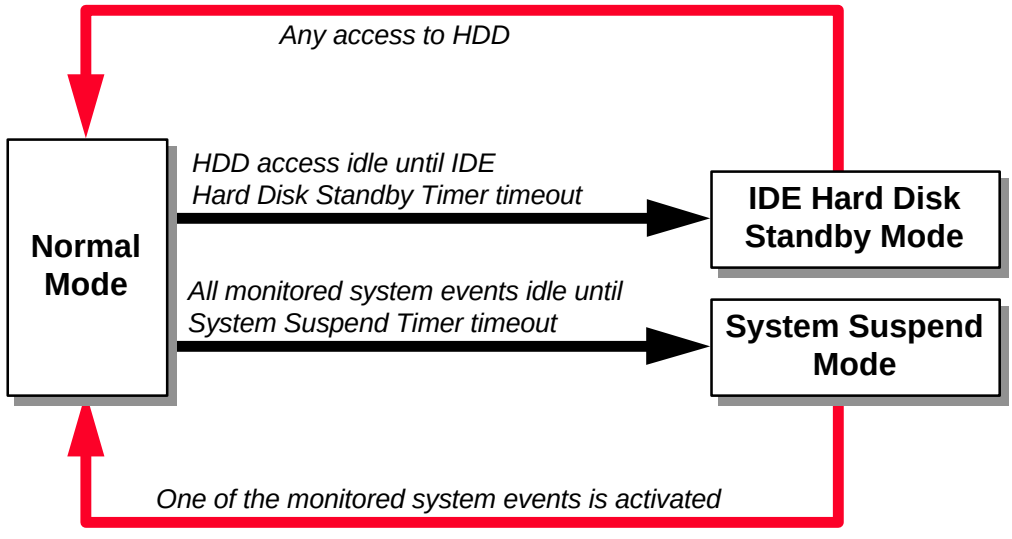


Figure 1-9 Power Saving Flowchart

1.8. Environmental Requirements

1.8.1 Temperature

Table 1-16 Temperature Requirements

Item Condition	Specification
Operating	+10 ~ +35°C
Non-operating	-20 ~ +60°C

1.8.2 Humidity

Table 1-17 Humidity Requirements

Item Condition	Specification
Operating	20% to 80% RH
Non-operating	20% to 80% RH

1.8.3 Vibration

Table 1-18 Vibration Requirements

Item Condition	Specification
Operating (unpacked)	5 ~ 18 Hz : 0.015 in 18 ~ 250 Hz : 0.25 G
Non-operating (packed)	5 ~ 27.1 Hz : 0.6 G 27.1 ~ 50 Hz : 0.016 in 50 ~ 500 Hz : 2 G

1.9. Mechanical Specifications

1.9.1 ID2PN Housing

Table 1-19 ID2PN Housing Specifications

Item	Description
Housing type	Desktop
Supported M/B form factor	Baby AT or LPX
Dimension (h x d x ww, mm)	128 x 418 x 368
Net Weight (kg)	7.7
Expansion slot	4
Supported SPS type	PS/2 type
Indicator	Power, HDD, Turbo
Drive bay	1 x 3.5-inch internal 1 x 3.5-inch external 2 x 5.25-inch external

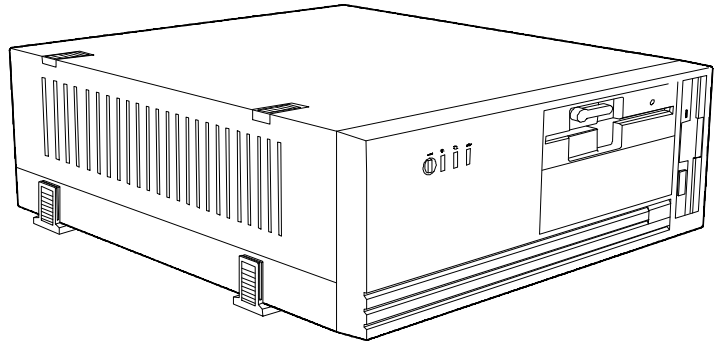


Figure 1-10 ID2PN Housing

1.9.2 IDABN Housing

Table 1-20 IDABN Housing Specifications

Item	Description
Housing type	Minitower
Supported M/B form factor	Baby AT or LPX
Dimension (h x d x ww, mm)	400 x 433.5 x 190
Net Weight (kg)	7
Expansion slot	8
Supported SPS type	PS/2 type
Indicator	Power, HDD, Turbo
Drive bay	2 x 3.5-inch internal 2 x 3.5-inch external 3 x 5.25-inch external
Unique feature	• Screwless design • Front door with dual openings (i.e., left and right sides)

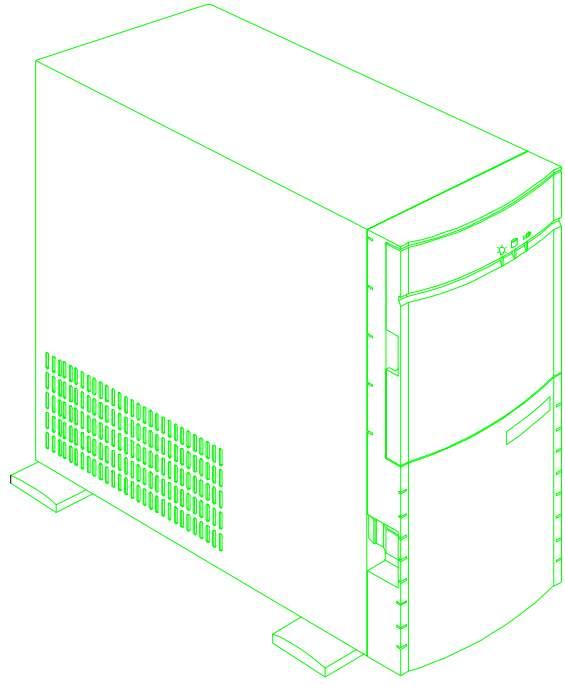


Figure 1-11 IDABN Housing

1.9.3 Aspire Desktop Housing

Table 1-21 Aspire Desktop Housing Specifications

Item	Description
Housing type	Desktop
Supported M/B form factor	LPX
Dimension (h x d x ww, mm)	115 x 442 x 405
Net Weight (kg)	6.7
Expansion slot	
Supported SPS type	PS/2 type
Indicator	Power, HDD, Turbo
Drive bay	1 x 3.5-inch internal 1 x 3.5-inch external 1 x 5.25-inch external

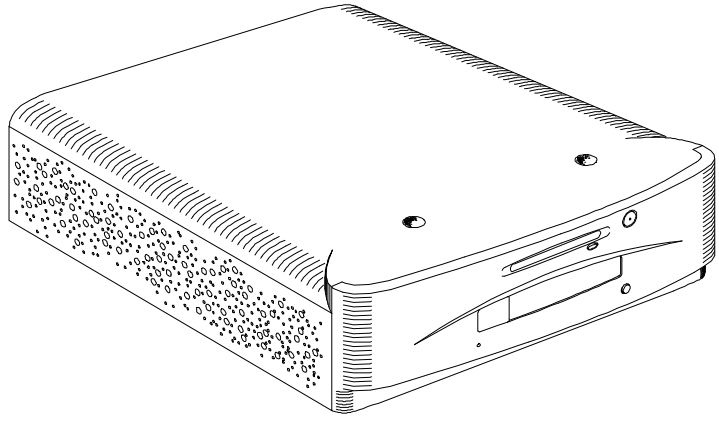


Figure 1-12 Aspire Desktop Housing

1.9.4 Aspire Minitower Housing

Table 1-22 Aspire Minitower Housing Specifications

Item	Description
Housing type	Minitower
Supported M/B form factor	Baby-AT or LPX
Dimension (h x d x ww, mm)	414 x 487 x 189
Net Weight (kg)	
Expansion slot	
Supported SPS type	PS/2 type
Indicator	Power, HDD, Turbo
Drive bay	2 x 3.5-inch internal 2 x 3.5-inch external 3 x 5.25-inch external

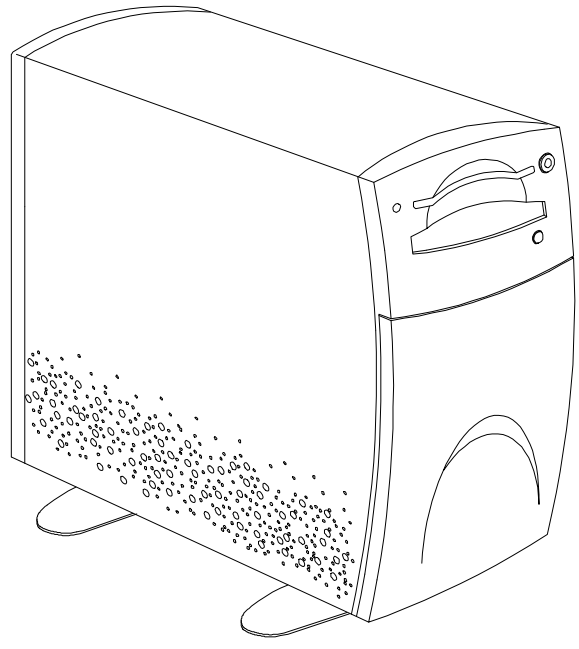


Figure 1-13 Aspire Minitower Housing

Major Chipsets

2.1. M1531

M1531 includes the higher CPU bus frequency (up to 83.3MHz) interface for the incoming Cyrix M2 and AMD K6, PBSRAM and Memory Cache L2 controller, internal MESI tag bits (8K*2) to reduce cost and enhance performance, high performance FPM/EDO/SDRAM DRAM controller, PCI 2.1 compliant bus interface, smart deep buffer design for CPU-to-DRAM, CPU-to-PCI, and PCI-to-DRAM to achieve the best system performance, and also the highly efficient PCI fair arbiter. M1531 also provides the most flexible 32/64-bit memory bus interface for the best DRAM upgrade ability and ECC/Parity design to enhance the system reliability.

With the concurrent bus design, PCI-to-PCI access can run concurrently with CPU-to-L2 and CPU-to-DRAM access, PCI-to-DRAM access can run concurrently with CPU-to-L2 access. M1531 also supports the snoop ahead feature to achieve the PCI master full bandwidth access (133Mbytes). M1531 also provides the enhanced power management features including ACPI support, suspend DRAM refresh, and internal chip power control to support the Microsoft's On Now technology OS.

2.1.1 Features

- Supports all Intel/Cyrix/AMD/TI/IBM 586 processors. Host bus at 83.3, 75, 66, 60 and 50 MHz at 3.3V/2.5V

- Supports Linear Wrap mode for Cyrix M1 and M2
    - Write-Allocation feature for K6
    - Pseudo-synchronous PCI bus access
      (CPU bus: 75 MHz - PCI bus: 30 MHz, CPU bus: 83.3 MHz - PCI bus: 33 MHz)

- Supports Pipelined-burst SRAM/Memory Cache
    - Direct mapped, 256 KB/512 KB/1 MB
    - Write-Back/Dynamic-Write-Back cache policy
    - Built-in 8K x 2 bit SRAM for MESI protocol to reduce cost and enhance performance
    - Cacheable memory up to 64 MB with 8-bit Tag SRAM
    - Cacheable memory up to 512 MB with 11-bit Tag SRAM
    - 3-1-1-1-1-1-1-1 for Pipelined-burst SRAM/Memory Cache at back-to-back burst read and write cycles
    - 3.3V/5V SRAMs for Tag address
    - CPU single-read cycle L2 allocation

- Supports FPM/EDO/SDRAM DRAMs
    - 8 RAS lines up to 1 GB support
    - 64-bit data path to memory

- Symmetrical/Asymmetrical DRAMs
- 3.3V or 5V DRAMs
- Duplicated MA[1:0] driving pins for burst access
- No buffer needed for RASJ and CASJ and MA[1:0]
- CBR and RAS-only refresh for FPM
- CBR and RAS-only refresh and Extended refresh and self refresh for EDO
- CBR and Self refresh for SDRAM
- 16 Qword deep merging buffer for 3-1-1-1-1-1-1-1 posted-write cycle to enhance high-speed CPU burst access
- 6-3-3-3-3-3-3-3 for back-to-back FPM read page hit, 5-2-2-2-2-2-2-2 for back-to-back EDO read page hit, 6-1-1-1-2-1-1-1 for back-to-back SDRAM read page hit, 2-2-2-2 for retired data for posted write on FPM and EDO page-hit, x-1-1-1 for retired data for posted write SDRAM page-hit
- Enhanced DRAM page miss performance
- Supports 64 Mbit (16M x 4, 8M x 8, 4M x 16) technology of DRAMs
- Supports Programmable-strength RAS/CAS/ MWEJ/MA buffers
- Supports Error Checking and Correction (ECC) and Parity for DRAM
- Supports the most flexible six 32-bit populated banks of DRAM for easy DRAM upgrade
- Supports SIMM and DIMM
- Synchronous/Pseudo Synchronous 25/30/33 MHz 3.3V/5V tolerance PCI interface
- Concurrent PCI architecture
- PCI bus arbiter: five PCI masters and M1533/ M1543 (ISA Bridge) supported
- 6 DWords for CPU-to-PCI memory write posted buffers
- Converts back-to-back CPU to PCI memory write to PCI burst cycle
- 38/22 Dwords for PCI-to-DRAM Write-posted/ Read-prefetching buffers
- PCI-to-DRAM up to 133 MB/sec bandwidth (even when L1/L2 write-back)
- L1/L2 pipelined-snoop ahead for PCI-to-DRAM cycle
- Supports PCI mechanism #1 only
- Complies with PCI spec. 2.1 (N(32/16/8)+8 rule, passive release, fair arbitration)
- Enhanced performance for Memory-Read-Line, Memory-Read-Multiple and Memory-write- Invalidate PCI commands

- Enhanced Power Management
  - ACPI support
  - PCI bus CLKRUN function
  - Dynamic Clock Stop

- Power-on Suspend
- Suspend to Disk
- Suspend to DRAM
- Self refresh during Suspend

- 328-pin (27mm x 27mm) BGA package

2.1.2 Pin Diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
A	NC	PHLDAJ	AD3	AD6	AD8	AD12	PAR	TRDYJ	AD17	AD22	AD25	AD30	REQJ3	GNTJ2	GNTJ3	MPD2	MPD0	MD61	MD29	MD62
B	BEJ0	PHLDJ	AD2	AD5	AD7	AD11	CBEJ1	DEVSELJ	AD16	AD21	AD24	AD29	REQJ2	GNTJ1	MPD5	MPD1	MD63	MD27	MD60	MD28
C	BEJ3	BEJ2	BEJ1	AD4	CBEJ0	AD10	AD15	STOPJ	CBEJ2	AD20	CBEJ3	AD28	REQJ1	GNT0J	MPD4	MD30	MD25	MD58	MD26	MD59
D	BEJ6	BEJ5	BEJ4	AD0	AD1	AD9	AD14	LOCKJ	FRAMEJ	AD19	AD23	AD27	REQJ0	MPD7	MPD3	MD55	MD23	MD56	MD24	MD57
E	DCJ	HITMJ	EADSJ	BEJ7	RSTJ	PCIMRQJ	AD13	SERRJ	IRDYJ	AD18	PCLKIN	AD26	AD31	MPD6	MD31	MD20	MD53	MD21	MD54	MD22
F	BRDYJ	BOFFJ	SMIACTJ	HLOCKJ	ADSJ	VCC_B								VCC_C	VCC_C	MD50	MD18	MD51	MD19	MD52
G	HD63	CACHEJ	AHOLD	KENJ	NAJ	VCC_A			**M1531**						VCC_C	MD15	MD48	MD16	MD49	MD17
H	HD60	HD61	HD62	WRJ	MIOJ			GND	GND	GND	GND	GND	GND			MD45	MD13	MD46	MD14	MD47
J	HD55	HD56	HD57	HD58	HD59			GND	GND	GND	GND	GND	GND			MD10	MD43	MD11	MD44	MD12
K	HD51	HD52	HD53	HD54	HCLKIN			GND	GND	GND	GND	GND	GND			MD40	MD8	MD41	MD9	MD42
L	HD46	HD47	HD48	HD49	HD50			GND	GND	GND	GND	GND	GND			MD5	MD38	MD6	MD39	MD7
M	HD41	HD42	HD43	HD44	HD45			GND	GND	GND	GND	GND	GND			MD35	MD3	MD36	MD4	MD37
N	HD36	HD37	HD38	HD39	HD40			GND	GND	GND	GND	GND	GND		VDD5S	REQJ4	GNTJ4	MD1	MD34	MD2
P	HD31	HD32	HD33	HD34	HD35	VCC_A									VCC_C	32K	SUSPEND	MD32	MD0	MD33
R	HD26	HD27	HD28	HD29	HD30	VDD5	VCC_A							VCC_B	VCC_C	RASJ6	RASJ7	CASJ2	CASJ7	CASJ3
T	HD21	HD22	HD23	HD24	HD25	HD0	A12	A5	GWEJ	COEJ	CADVJ	TWEJ	MAA0	MAA1	TIO8	TIO9	TIO10	RASJ1	RASJ0	CASJ6
U	HD16	HD17	HD18	HD19	HD20	HD1	A13	A8	CCSJ	BWEJ	CADSJ	TIO0	TIO1	MAB0	MAB1	MA5	MWEJ	RASJ4	RASJ3	RASJ2
V	HD15	HD14	HD13	HD6	HD3	A17	A14	A10	A4	A29	A25	A24	A23	TIO2	MA2	MA4	MA8	CASJ5	CASJ1	RASJ5
W	HD12	HD11	HD10	HD5	HD2	A18	A15	A11	A7	A30	A31	A22	A21	TIO4	TIO6	MA3	MA7	MA10	CASJ0	CASJ4
Y	HD9	HD8	HD7	HD4	A20	A19	A16	A9	A6	A3	A28	A26	A27	TIO3	TIO5	TIO7	MA6	MA9	MA11	NC

Figure 2-1 M1531 Pin Diagram (Top View)

2.1.3 Signal Descriptions

Table 2-1 M1531 Signal Descriptions

Signal	Type	Pin No.	Description
Host Interface 3.3V/2.5V			
A[31:3]	I/O Group A	W11,W10, V10, Y11, Y13, Y12, V11, V12, V137, W12, W13, Y5, Y6, W6, V6, Y7, W7, V7, U7, T7, W8, V8, Y8, U8, W9, Y9, T8, V9, Y10	**Host Address Bus Lines.** A[31:3] have two functions. As inputs, along with the byte enable signals, these pins serve as the address lines of the host address bus which define the physical area of memory or I/O being accessed. As outputs, the M1531 drives them during inquiry cycles on behalf of PCI masters.
BEJ[7:0]	I Group A	E4, D1, D2, D3, C1, C2, C3, B1,	**Byte Enables.** These are the byte enable signals for the data bus. BEJ[7] applies to the most significant byte and BEJ[0] applies to the least significant byte. They determine which byte of data must be written to the memory, or are requested by the CPU. In local memory read and line-fill cycles, these inputs are ignored by the M1531.
ADSJ	I Group A	F5	**Address Strobe.** The CPU will start a new cycle by asserting ADSJ first. The M1531 will not precede to execute a cycle until it detects ADSJ active.
BRDYJ	O Group A	F!	**Burst Ready.** The assertion of BRDYJ means the current transaction is complete. The CPU terminates the cycle by receiving 1 or 4 active BRDYJs depending on different types of cycles.
NAJ	O Group A	G5	**Next Address.** This signal is asserted by the M1531 to inform the CPU that pipelined cycles are ready for execution.
AHOLD	O Group A	G3	**CPU AHold Request Output.** It connects to the input of CPU's AHOLD pin and is actively driven for inquiry cycles.
EADSJ	O Group A	E3	**External Address Strobe.** This signal is connected to the CPU EADSJ pin. During PCI cycles, the M1531 asserts this signal to proceed snooping.
BOFFJ	O Group A	F2	**CPU Back-Off.** If BOFFJ is sampled active, CPU will float all its buses in the next clock. M1531 asserts this signal to request CPU floating all its output buses.
HITMJ	I Group A	E2	**Primary Cache Hit and Modified.** When snooped, the CPU asserts HITMJ to indicate that a hit to a modified line in the data cache occurred. It is used to prohibit another bus master from accessing the data of this modified line in the memory until the line is completely written back.
MIOJ	I Group A	H5	**Host Memory or I/O.** This bus definition pin indicates the current bus cycle is either memory or input/ output.
DCJ	I Group A	E1	**Host Data or Code.** This bus definition pin is used to distinguish data access cycles from code access cycles.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
Host Interface 3.3V/2.5V			
WRJ	I Group A	H4	**Host Write or Read.** When WRJ is driven high, it indicates the current cycle is a write. Inversely, if WRJ is driven low, a read cycle is performed.
HLOCKJ	I Group A	F4	**Host Lock.** When HLOCKJ is asserted by the CPU, the M1531 will recognize the CPU is locking the current cycles.
CACHEJ	I Group A	G2	**Host Cacheable.** This pin is used by the CPU to indicate the system that CPU wants to perform a line fill cycle or a burst write back cycle. If it is driven inactive in a read cycle, the CPU will not cache the returned data, regardless of the state of KENJ.
KENJ/INV	O Group A	G4	**Cache Enable Output.** This signal is connected to the CPU's KENJ and INV pins. KENJ is used to notify the CPU whether the address of the current transaction is cacheable. INV is used during L1 snoop cycles. The M1531 drives this signal high (low) during the EADSJ assertion of a PCI master write (read) snoop cycle.
SMIACTJ	I Group A	F3	**SMM Interrupt Active.** This signal is asserted by the CPU to inform the M1531 that SMM mode is being entered.
HD[63:0]	I/O Group A	G1, H3, H2, H1, J5, J4, J3, J2, J1, K4, K3, K2, K1, L5, L4, L3, L2, L1, M5, M4, M3, M2, M1, N5, N4, N3, N2, N1, P5, P4, P3, P2, P1, R5, R4, R3, R2, R1, T5, T4, T3, T2, T1, U5, U4, U3, U2, U1, V1, V2, V3, W1, W2, W3, Y1, Y2, Y3, V4, W4, Y4, V5, W5, U6, T6,	**Host Data Bus Lines.** These signals are connected to the CPU's data bus. HD[63] applies to the most significant bit and HD[0] applies to the least significant bit.
MPD[7:0]	I/O Group C	D14, E14, B15, C15, D15, A16, B16, A17,	**DRAM Parity /ECC check bits.** These are the 8 bits for parities/ECC check bits over DRAM data bus. MPD[7] applies to the most significant bit and MPD[0] applies to the least significant bit.
RASJ[7] / SRASJ[0]	O Group C	R17	**Row Address Strobe 7, (FPM/EDO) of DRAM row 7.** SDRAM Row Address Strobe (SDRAM) copy 0. It connects to SDRAM RASJ. This is a multifunction pin and determined by Index-5Ch bit0.
RASJ[6] / SCASJ[0]	O Group C	R16	**Row Address Strobe 6, (FPM/EDO) of DRAM row 6.** SDRAM Column address strobe (SDRAM) copy 0. It connects to SDRAM CASJ. This is a multifunction pin and determined by Index-5Ch bit0.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
Host Interface 3.3V/2.5V			
RASJ[5:0]	O Group C	V20, U18, U19, U20, T18, T19,	**Row Address Strobes.** These signals are used to drive the corresponding RASJs of FPM/EDO DRAMs. In SDRAM, they are used to drive the corresponding SDRAM CSJs.
CASJ[7:0] / DQM[7:0]	O Group C	R19, T20, V18, W20, R20, R18, V19, W19,	**Column Address Strobes or Synchronous DRAM Input/Output Data Mask.** These CAS signals should be connected to the corresponding CASJs of each bank of DRAM. The value of CASJs equals that of HBEJs for write cycles. During DRAM read cycles, all of CASJs will be active. In SDRAM, these pins act as synchronized output enables during a read cycle and the byte mask during write cycle, these pins are connected to SDRAM DQM[7:0].
MA[11:2]	O Group C	Y19, W18, Y18, V17, W17, Y17, U16, V16, W16, V15,	**DRAM Address Lines.** These signals are the address lines[11:2] of all DRAMs. The M1531 supports DRAM types ranging from 256K to 64Mbits.
MAA[1:0]	O Group C	T14, T13,	**Memory Address copy A for [1:0].** These signals are the address lines[1:0] copy 0 of all DRAMs.
MAB[1:0]	O Group C	U15, U14,	**Memory Address copy B for [1:0].** These signals are the address lines[1:0] copy 1 of all DRAMs.
MWEJ[0]	O Group C	U17	**DRAM Write Enable.** This is the DRAM write enable pin and behaves according to the early-write mechanism, i.e. , it activates before the CASJs do. For refresh cycles, it will remain deasserted.
MD[63:0]	I/O Group C	B17, A20, A18, B19, C20, C18, D20, D18, D16, E19, E17, F20, F18, F16, G19, G17, H20, H18, H16, J19, J17, K20, K18, K16, L19, L17, M20, M18, M16, N19, P20, P18, E15, C16, A19, B20, B18, C19, C17, D19, D17, E20, E18, E16, F19, F17, G20, G18, G16, H19, H17, J20, J18, J16, K19, K17, L20, L18, L16, M19, M17, N20, N18, P19,	**Memory Data.** These pins are connected to DRAM's data bits. MD[63] applies to the most significant bit and MD[0] applies to the least significant bit.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
Host Interface 3.3V/2.5V			
CLKEN[0]/ REQJ[4]	I/O Group C	N16	**SDRAM Clock Enable Copy 0 or PCI Master Request.** This signal is used as SDRAM clock enable copy 0 to do self refresh during suspend. It can also be used as bus request signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
CLKEN[1]/ GNTJ[4]	O Group C	N17	**SDRAM Clock Enable Copy 1 or PCI Master Grant.** This signal is used as SDRAM clock enable copy 1 to do self refresh during suspend. It can also be used as grant signal of the fifth PCI master. This function is controlled by Index -5Dh bit 1.
Secondary Cache Interface 3.3V/2.5V Tolerance			
CADVJ	O Group A	T11	**Synchronous SRAM Advance.** This signal will make PBSRAM/Memory Cache internal burst address counter advance.
CADSJ	O Group A	U11	**Synchronous SRAM Address Strobe.** This signal connects to PBSRAM/ Memory Cache ADSCJ.
CCSJ	O Group A	U9	**Synchronous SRAM Chip Select.** This signal connects to PBSRAM/Memory Cache CE1J to mask ADSPJ and enable ADSCJ sampling.
GWEJ	O Group A	T9	**Synchronous SRAM Global Write Enable.** This signal will write all the byte lanes data into PBSRAM/Memory Cache.
COEJ	O Group A	T10	**Synchronous SRAM Output Enable.** This signal will enable the data output driving of PBSRAM/Memory Cache.
BWEJ	O Group A	U10	**Synchronous SRAM Byte-Write Enable.** This signal connects to byte write enable of PBSRAM/Memory Cache.
TIO[10]/ MWEJ[1]/ MKREFRQJ	I/O Group C	T17	**SRAM Tag[10] or another copy of MWEJ or DRAM Cache MKREFRQJ.** This pin is used for multifunction. It can be SRAM tag address bit 10, or another copy of MWEJ connected to DRAM, or MKREFRQJ connected to DRAM Cache. Refer to Register Index-41h bit 6, bit3 and bit0 description.
TIO[9]/ SRASJ[1]	I/O Group C	T16	**SRAM Tag[9] or Synchronous DRAM (SDRAM) RAS copy 1.** This pin is used for multifunction. It can be SRAM tag address bit 9, or another copy of SRASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.
TIO[8]/ SCASJ[1]	I/O Group C	T15	**SRAM Tag[8] or Synchronous DRAM (SDRAM) CAS copy 1.** This pin is used for multifunction. It can be SRAM tag address bit 8, or another copy of SCASJ connected to SDRAM. Refer to Register Index-41h bit3 and bit0 description.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
Secondary Cache Interface 3.3V/2.5V Tolerance			
TIO[7:0]	I/O Group B	Y16, W15, Y15, W14, Y14, V14, U13, U12	**SRAM Tag[7:0].** This pin contains the L2 tag address for 256-KB L2 caches. TIO[6:0] contain the L2 tag address and TIO7 contains the L2 cache valid bit for 512-KB caches. TIO[5:0] contain L2 tag address, TIO7 contains L2 cache valid bit and TIO6 contains the L2 cache dirty bit for 1-MB cache. Refer to index-41h cache configuration table.
TAGWEJ	O Group B	T12	**Tag Write Enable.** This signal, when asserted, will write into the external tag new state and tag addresses.
PCI Interface 3.3V/2.5V Tolerance			
AD[31:0]	I/O Group B	E13, A12, B12, C12, D12, E12, A11, B11, D11, A10, B10, C10, D10, E10, A9, B9, C7, D7, E7, A6, B6, C6, D6, A5, B5, A4, B4, C4, A3, B3, D5, D4,	**PCI Address and Data Bus Lines.** These lines are connected to the PCI bus. AD[31:0] contain the information of address or data for PCI transactions.
CBEJ[3:0]	I/O Group B	C11, C9, B7, C5,	**PCI Bus Command and Byte Enables.** Bus commands and byte enables are multiplexed in these lines for address and data phases, respectively.
FRAMEJ	I/O Group B	D9	**Cycle Frame of PCI Buses.** This indicates the beginning and duration of a PCI access. It will be as an output driven by M1531 on behalf of CPU, or as an input during PCI master access.
DEVSELJ	I/O Group B	B8	**Device Select.** When the target device has decoded the address as its own cycle, it will assert DEVSELJ.
IRDYJ	I/O Group B	E9	**Initiator Ready.** This signal indicates the initiator is ready to complete the current data phase of transaction.
TRDYJ	I/O Group B	A8	**Target Ready.** This pin indicates the target is ready to complete the current data phase of transaction.
STOPJ	I/O Group B	C8	**Stop.** This signal indicates the target is requesting the master to stop the current transaction.
LOCKJ	I/O Group B	D8	**Lock Resource Signal.** This pin indicates the PCI master or the bridge intends to do exclusive transfers.
REQJ[3:0]	I Group B	A13, B13, C13, D13,	**Bus Request signals of PCI Masters.** When asserted, it means the PCI Master is requesting the PCI bus ownership from the arbiter.
GNTJ[3:0]	O Group B	A15, A14, B14, C14	**Grant signals to PCI Masters.** When asserted by the arbiter, it means the PCI master has been legally granted to own the PCI bus.

Signal	Type	Pin No.	Description
PHLDJ	I Group B	B2	**PCI bus Hold Request.** This active low signal is a request from M1533/M1543 for the PCI bus.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
PCI Interface 3.3V/2.5V Tolerance			
PHLDAJ	O Group B	A2	**PCI bus Hold Acknowledge.** This active low signal grants PCI bus to M1533/M1543.
PAR	I/O Group B	A7	**Parity bit of PCI bus.** It is the even parity bit across PAD[31:0] and CBEJ[3:0].
SERRJ/ CLKRUNJ	I/O Group B	E8	**System Error or PCI Clock RUN.** If the M1531 detects parity errors in DRAMs, it will assert SERRJ to notify the system. As CLKRUNJ, this signal will connect to M1533 CLKRUNJ to start, or maintain the PCI CLOCK. It is a multifunction pin and determined by Index-77h bit0.
Clock, Reset, and Suspend			
HCLKIN	I Group A	K5	**CPU bus Clock Input.** This signal is used by all of the M1531 logic that is in the Host clock domain.
RSTJ	I Group B	E5	**System Reset.** This pin, when asserted, resets the M1531 state machine, and sets the register bits to their default values.
Clock, Reset, and Suspend			
PCICLK	I Group B	E11	**PCI bus Clock Input.** This signal is used by all of the M1531 logic that is in the PCI clock domain.
PCIMRQJ	O Group B	E6	**Total PCI Request.** This signal is used to notify M1533/M1543 that there is PCI master requesting PCI bus.
SUSPENDJ	I Group C	P17	**Suspend.** When actively sampled, the M1531 will enter the I/O suspend mode. This signal should be pulled high when the suspend feature is disabled.
OSC32KO	I Group C	P16	**The refresh reference clock of frequency 32 KHz during suspend mode.** This signal should be pulled to a fixed value when the suspend feature is disabled.
Power Pins			
VCC_A	P	G6, P6, P6,	**Vcc 3.3V or 2.5V Power for Group A.** This power pin is used for CPU interface and L2 control signals. If this power pin connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power pin connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VCC_B	P	F6, R14,	**Vcc 3.3V Power for Group B.** This power pin is used for PCI interface and Tag signals. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.
VCC_C	P	F14, F15, G15, P15,	**Vcc 3.3V Power for Group C.** This power pin is used for DRAM interface signals during normal operation and suspend refresh. It must connect to 3.3V. The relative signals will output 3.3V and 5V input tolerance.

Pin Description Table (continued) :

Signal	Type	Pin No.	Description
Power Pins			
VDD_5	P	R6	**Vcc 5.0V Power for Group A and Group B.** This pin supplies the 5V input tolerance circuit and the core power for the internal circuit except the suspend circuit.
VDD_5S	P	N15	**Vcc 5.0V Power for Group C.** This pin supplies the 5V input tolerance circuit and the core power for the internal suspend circuit.
Vss or Gnd	P	H10, H12, H8, J10, J12, J8, K10, K12, K8, L10, L12, L8, M10, M12, M8, N10, N12, N8,	**Ground**
N.C.		A1, Y12	**Non-Connected**

2.2. M1533

The M1533 is a bridge between PCI and ISA bus, providing full PCI and ISA compatible functions. This chip has Integrated System Peripherals (ISP) (2 x 82C59 and serial interrupt, 1 x 82C54), advanced features (Type F and Distributed DMA) in the DMA controller (2 x 82C54), PS/2 keyboard/mouse controller, two-channel dedicated IDE master controller with Ultra-33 specification, System Management Bus (SMB), and two OpenHCI 1.0a USB ports. The ACPI (Advanced Configuration and Power Interface) and PCI 2.1 (Delayed Transaction & Passive Release) specification have also been implemented. Furthermore, this chip supports the Advanced Programmable Interrupt Controller (APIC) interface for Multiple-Processors system.

The M1533 also supports the deep flexible green function for the best green system. It can connect to the ALi Pentium North Bridge (M1521/M1531/M1541) and ALi Pentium Pro North Bridge (M1615) to provide the best system solution. One eight-byte bidirectional line buffer is provided for ISA/DMA master memory read/writes; one 32-bit wide posted write buffer is provided for PCI memory write & I/O write (for audio) cycles to the ISA bus, to provide a PCI to ISA IRQ routing table, and level-to-edge trigger transfer.

The chip provides two extra IRQ lines and one programmable chip select for motherboard Plug-and-Play functions. The interrupt lines can be routed to any of the available ISA interrupts. The on-chip IDE controller supports two separate IDE connectors for up to four IDE devices providing an interface for IDE hard disks and CD ROMs. The Ultra 33 specification (that supports the 33 MB/second transfer rate) has been implemented at this IDE controller. The ATA bus pins and the buffer (read ahead and posted write) are all dedicated for separate channel to improve the performance of IDE master.

The M1533 supports Super Green function for Intel and Intel compatible CPUs. It implements SMI or SCI (System Controller Interrupt) to meet the ACPI specification. It also meets the requirement for OnNow design initiative. It also features powerful power management for power saving including On, Standby, Sleeping, SoftOff, and Mechanical Off states. To control the CPU power consumption, it provides CPU clock control (STPCLKJ). The STPCLKJ can be active (low) or inactive (high) in turn by throttling control. In addition, the M1533 offers the most flexible system clock design. It can be programmed to stop the CPU Clock, PCI Clock, the Clock cell, or to reduce the Clock frequency. The PBSRAM (Pipelined-burst SRAM) doze mode is also supported.

The M1533 is includes a PS/2 keyboard/mouse controller, SMBus, two OpenHCI 1.0a USB ports, and the dedicated GPIO (General Purpose Input/Output) pins. These components enable the chip to implement the best green and cost/performance system.

2.2.1 Features

- Provides a bridge between the PCI bus and ISA bus for both Pentium and Pentium Pro systems

- PCI interface
    - PCI master and slave interface
    - PCI master and slave initiated termination
    - PCI spec. 2.1 compliant (Delayed Transaction support)

- Buffers control
    - 8-byte bidirectional line buffers for DMA/ISA memory read/write cycles to PCI bus
    - 32-bit posted write buffer for PCI memory write and I/O data write (for sound card) to ISA bus
- Provides steerable PCI interrupts for PCI device plug-and-play
    - Up to eight PCI interrupt routing
    - Level-to-edge trigger transfer
- Enhanced DMA controller
    - Provides 7 programmable channels: 4 for 8-bit data size, 3 for 16-bit data size
    - 32-bit addressability
    - Provides compatible DMA transfers
    - Provides Type F transfers
- Interrupt controller
    - Provides 14 interrupt channels
    - Independent programmable level/edge triggered channels
- Counter/Timers
    - 8254 compatible timers for System Timer, Refresh Request, Speaker Output Use
- Distributed DMA supported
    - 7 DMA Channels can be arbitrarily programmed as distributed channel
- Serialized IRQ supported
    - Quiet/Continuous mode
    - Programmable (default 21) IRQ/DATA frames
    - Programmable START frame pulse width
- Plug-and-Play port supported
    - One programmable chip select
    - Two steerable interrupt request lines
- Built-in keyboard controller
    - Built-in PS/2/AT keyboard and PS/2 mouse controller
- Supports up to 256-KB ROM size decoding

- Supports positive/subtractive decode for ISA device
- PMU features
    - Full-support for ACPI and OS directed power management
    - CPU SMM Legacy mode and SMI feature supported
    - Supports programmable STPCLKJ: throttle/CKONSTP/CKOFFSTP control
    - Supports I/O trap for I/O restart feature
    - PMU operation states :
        - On
        - Standby
        - Sleeping (Power-On Suspend)
        - Suspend (Suspend to DRAM)
        - Suspend to HDD
        - Soft Off
        - Mechanical Off
    - APM state detection and control logic supported
    - Global and local device power control logic
    - Ten Programmable Timers: Standby / LB / LLB / APMA / APMB / Global_Display / Primary_IDE / Secondary_IDE / SIO&Audio / Programmable IO Region
    - Provides system activity and display activity monitorings, including:
        - Video
        - Audio
        - Hard disk
        - Floppy
        - Serial ports
        - Parallel port
        - Keyboard
        - Six programmable I/O groups
        - Three programmable memory spaces
    - Provides hot plugging events detection

  - CRT connector
  - AC power
  - Docking insert
  - Eject
  - Setup button
  - Hot key press
- Multiple external wakeup events of Standby mode
  - Power button
  - Cover open
  - Modem ring
  - RTC alarm
  - EXTSW
  - DRQ2
- Suspend wakeup detected
  - Hot key
  - Modem ring
  - RTC alarm
  - Cover open
  - Docking insert
  - Power button
  - USB events
  - IRQ
  - EJECT
  - ACPWR
  - GPIO[19:16] event
- Two-level battery warning monitor
- Thermal alarm supported

- Clock generator control logic supported
  - CPUCLK stop control
  - PCICLK stop control
  - PLL stop control
  - Down frequency control
- L2 cache power down and PCI CLKRUN control logic supported
- 21 general purpose input signals, 24 general purpose output signals, 20 general purpose input/output signals
- 16 external expandable general purpose inputs, 16 external expandable general purpose outputs
- LCD control
- All registers readable/restorable for proper resume from Suspend state

- Built-in PCI IDE controller
  - Supports Ultra 33 Synchronous DMA Mode transfers up to Mode 2 Timing (33 MB/sec)
  - Supports PIO Modes up to Mode 5 timings, and Multiword DMA Mode 0, 1 ,2 with independent timing of up to 4 drives
  - Integrated 10 x 32-bit read ahead & posted write buffers for each channel (total: 20 Dwords)
  - Dedicated pins of ATA interface for each channel
  - Supports tri-state IDE signals for swap bay

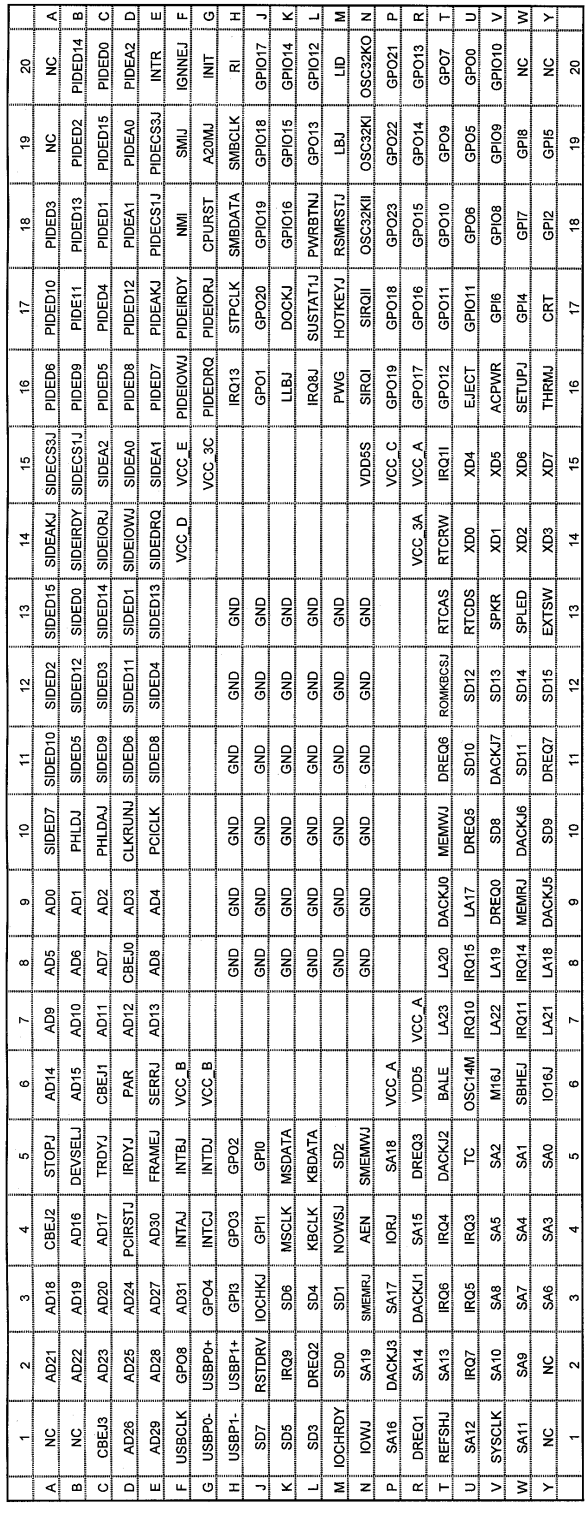
- USB interface
  - One root hub with two USB ports based on OpenHCI 1.0a specification
  - Supports FS (12Mbits/sec) and LS (1.5Mbits/sec) serial transfer
  - Supports Legacy keyboard and mouse software with USB-based keyboard and mouse

- SMBus interface
  - System Management Bus interface which meets the v1.0 specification

- External APIC interface supported

- 328-pin (27mm x 27mm) BGA package

2.2.2 Pin Diagram



	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	NC	AD21	AD18	CBEJ2	STOPJ	AD14	AD9	AD5	AD0	SIDED7	SIDED10	SIDED2	SIDED15	SIDEAKJ	SIDECS3J	PIDED6	PIDED10	PIDED3	NC	NC	A
B	NC	AD22	AD19	AD16	DEVSELJ	AD15	AD10	AD6	AD1	PHLDJ	SIDED5	SIDED12	SIDED0	SIDEIRDY	SIDECS1J	PIDED9	PIDE11	PIDED13	PIDED2	PIDED14	B
C	CBEJ3	AD23	AD20	AD17	TRDYJ	CBEJ1	AD11	AD7	AD2	PHLDAJ	SIDED9	SIDED3	SIDED14	SIDEIORJ	SIDEA2	PIDED5	PIDED4	PIDED1	PIDED15	PIDED0	C
D	AD26	AD25	AD24	PCIRSTJ	IRDYJ	PAR	AD12	CBEJ0	AD3	CLKRUNJ	SIDED6	SIDED11	SIDED1	SIDEIOWJ	SIDEA0	PIDED8	PIDED12	PIDEA1	PIDEA0	PIDEA2	D
E	AD29	AD28	AD27	AD30	FRAMEJ	SERRJ	AD13	AD8	AD4	PCICLK	SIDED8	SIDED4	SIDED13	SIDEDRQ	SIDEA1	PIDED7	PIDEAKJ	PIDECS1J	PIDECS3J	INTR	E
F	USBCLK	GPO8	AD31	INTAJ	INTBJ	VCC_B								VCC_D	VCC_E	PIDEIOWJ	PIDEIRDY	NMI	SMIJ	IGNNEJ	F
G	USBP0-	USBP0+	GPO4	INTCJ	INTDJ	VCC_B									VCC_3C	PIDEDRQ	PIDEIORJ	CPURST	A20MJ	INIT	G
H	USBP1-	USBP1+	GPI3	GPO3	GPO2			GND	GND	GND	GND	GND	GND			IRQ13	STPCLK	SMBDATA	SMBCLK	RI	H
J	SD7	RSTDRV	IOCHKJ	GPI1	GPI0			GND	GND	GND	GND	GND	GND			GPO1	GPO20	GPO19	GPO18	GPIO17	J
K	SD5	IRQ9	SD6	MSCLK	MSDATA			GND	GND	GND	GND	GND	GND			LLBJ	DOCKJ	GPO16	GPO15	GPIO14	K
L	SD3	DREQ2	SD4	KBCLK	KBDATA			GND	GND	GND	GND	GND	GND			IRQ8J	SUSTAT1J	PWRBTNJ	GPO13	GPIO12	L
M	IOCHRDY	SD0	SD1	NOWSJ	SD2			GND	GND	GND	GND	GND	GND			PWG	HOTKEYJ	RSMRSTJ	LBJ	LID	M
N	IOWJ	SA19	SMEMRJ	AEN	SMEMWJ			GND	GND	GND	GND	GND	GND		VDD5S	SIRQI	SIRQII	OSC32KII	OSC32KI	OSC32KO	N
P	SA16	DACKJ3	SA17	IORJ	SA18	VCC_A									VCC_C	GPO19	GPO18	GPO23	GPO22	GPO21	P
R	DREQ1	SA14	DACKJ1	SA15	DREQ3	VDD5	VCC_A							VCC_3A	VCC_A	GPO17	GPO16	GPO15	GPO14	GPO13	R
T	REFSHJ	SA13	IRQ6	IRQ4	DACKJ2	BALE	LA23	LA20	DACKJ0	MEMWJ	DREQ6	ROMKBCSJ	RTCAS	RTCRW	IRQ1I	GPO12	GPO11	GPO10	GPO9	GPO7	T
U	SA12	IRQ7	IRQ5	IRQ3	TC	OSC14M	IRQ10	IRQ15	LA17	DREQ5	SD10	SD12	RTCDS	XD0	XD4	EJECT	GPIO11	GPO6	GPO5	GPO0	U
V	SYSCLK	SA10	SA8	SA5	SA2	M16J	LA22	LA19	DREQ0	SD8	DACKJ7	SD13	SPKR	XD1	XD5	ACPWR	GPI6	GPIO8	GPIO9	GPIO10	V
W	SA11	SA9	SA7	SA4	SA1	SBHEJ	IRQ11	IRQ14	MEMRJ	DACKJ6	SD11	SD14	SPLED	XD2	XD6	SETUPJ	GPI4	GPI7	GPI8	NC	W
Y	NC	NC	SA6	SA3	SA0	IO16J	LA21	LA18	DACKJ5	SD9	DREQ7	SD15	EXTSW	XD3	XD7	THRMJ	CRT	GPI2	GPI5	NC	Y
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

Figure 2-2 M1533 Pin Diagram

2.2.3 Signal Descriptions

Pin Name	Pin No.	Type	Description
Clock & Reset Unit :			
PWG	M16	I-Group C Schmitt	**Power-Good Input.** This signal comes from the power supply to indicate that power is available and stable. The de-assertion of this input will enable the leakage control circuit between Soft-off (Suspend to Disk) resume circuit and no power circuit.
PCICLK	E10	I-Group B	**PCI Clock for Internal PCI Interface.** This is an input PCI clock, it should always be running at ON, STANDBY, SLEEP (Power-On Suspend) state. When CLKRUNJ is active, this clock should always keep on running. Internal PCI state machine and ISA state machine will use this clock.
OSC14M	U6	I-Group A	**14.318Mhz Clock Input.** This input clock will be used for Power Management timer, M8254 timer, SM bus base frequency and ISA state machine.
OSC32KI	N19	I-Group C	**32 Khz Oscillator Input1.** This is a crystal input 1 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a crystal is not used, an external 32 Khz clock input should connect to this pin.
OSC32KII	N18	I-Group C	**32 Khz Oscillator Input2.** This is a crystal input 2 from a 32.768 KHz Quartz Crystal. The M1533 will generate the 32 KHz clock for the internal Suspend circuit and output the clock from the CLK32KO to North Bridge DRAM Suspend Refresh Circuit. If a Crystal is not used, this pin should be floated.
USBCLK	F1	I-Group B	**48 MHz USB Clock Input.** This clock will send to USB state machine to generate USB signals.
PCI Bus Interface Unit :			
PCIRSTJ	D4	O-Group B 12/16 mA	**PCI Bus Reset.** This is an output signal to reset the entire PCI Bus. This signal will be asserted during system reset and is a logic invert of RSTDRV.
AD[31:0]	F3, E4, E1, E2, E3, D1, D2, D3, C2 B2, A2 C3, B3, A3, C4, B4, B6, A6, E7, D7, C7 B7, A7, E8, C8, B8, A8, E9, D9, C9, B9, A9	I/O Group B 12/16 mA	**Address and Data Multiplexed Bus.** During the first clock of a PCI transaction, AD[31:0] contain a physical address. During subsequent clocks, AD[31:0] contain data.
CBEJ[3:0]	C1, A4, C6, D8	I/O Group B 12/16 mA	**Bus Command and Byte enable.** During address phase, CBEJ[3:0] define the Bus Command. During data phase, CBEJ[3:0] define the Byte Enables.
FRAMEJ	E5	I/O Group B 12/16 mA	**Cycle Frame.** Cycle Frame is driven by current initiator to indicate the beginning and duration of a PCI access.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
PCI Bus Interface Unit :			
TRDYJ	C5	I/O Group B 12/16 mA	**Target Ready.** Target Ready indicates the target's ability to complete the current data phase of the transaction.
IRDYJ	D5	I/O Group B 12/16 mA	**Initiator Ready.** Initiator Ready indicates the initiator's ability to complete the current data phase of the transaction.
STOPJ	A5	I/O Group B 12/16 mA	**Cycle stop request.** Cycle Stop indicates the target is requesting the master to stop the current transaction.
DEVSELJ	B5	I/O Group B 12/16 mA	**Device Select.** This signal indicates that the target device has decoded the address as its own cycle. This pin is an output pin when M1533 acts as a PCI slave has decoded address as its own cycle including subtractive decoding.
SERRJ	E6	I-Group B	**System Error.** This signal may be pulsed active by any agent that detects a system error condition. When SERRJ is sampling low, M1533 will assert NMI to generate non-maskable interrupt to CPU.
PAR	D6	I/O Group B 12/16 mA	**Parity Signal.** PAR is an Even Parity and is calculated on AD[31:0] and CBEJ[3:0]. When M1533 acts as a PCI master, it drives PAR one PCI clock after address phase for read/write transaction and one PCI clock after data phase for write transaction. When the M1533 acts as a target, it drives PAR one PCI clock after data phase for PCI master read transaction.
PHLDAJ	C10	I-Group B	**PCI Bus Ownership Acknowledge.** When PCI bus arbiter asserts this pin, M1533 has owned the PCI bus.
PHLDJ	B10	O-Group B 4/4 mA	**PCI Bus Ownership Request.** M1533 requests the ownership of the PCI bus from the PCI bus arbiter on the North Bridge. M1533 will assert this signal on behalf of the ISA Master, DMA Device, IDE Master, and the USB Master.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
PCI Bus Interface Unit :			
INTAJ_MI	F4	I-Group B	**PCI INTA.** PCI interrupt input A or PCI interrupt polling input. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTAJ when 4 PCI Interrupts are supported, or connects to the 74F181 encoded output to support the 8 PCI Interrupts polling mode.
INTBJS0	F5	I/O Group B Schmitt 4/4 mA	**PCI INTB.** PCI interrupt input B or polling select_0 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is an INTBJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 0 to support the 8 PCI Interrupts polling mode.
INTCJS1	G4	I/O Group B Schmitt 4/4 mA	**PCI INTC.** PCI interrupt input C or polling select_1 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTCJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 1 to support the 8 PCI Interrupts polling mode.
INTDJS2	G5	I/O Group B Schmitt 4/4 mA	**PCI INTD.** PCI interrupt input D or polling select_2 output. M1533 can support up to 8 PCI Interrupts routing by using a 74F181 to do the polling. This pin is a multi-function pin: it is the INTDJ when 4 PCI Interrupts are supported, or connects to the 74F181 selection input 2 to support the 8 PCI Interrupts polling mode.
CPU interface :			
INIT	G20	O-Group E 2.4/2.4 mA	**CPU Initialize Interrupt.** CPU cold & warm reset. When CPU is Pentium Pro, this signal is low active. Otherwise, this signal is high active. When power on, KBC RC, port 92 RC, shutdown all will trigger INIT active.
CPURST	G18	O-Group E 2.4/2.4 mA	**CPU Cold Reset.** When power turn on, this reset signal will be asserted, and then will become de-asserted until 4 ms after PWG becomes high.
IGNNEJ	F20	O-Group E 2.4/2.4 mA	**Ignore Error.** This pin is used as the ignore numeric coprocessor error.
INTR	E20	O-Group E 2.4/2.4 mA	**Interrupt Request to CPU.** This is the interrupt signal generated by the internal 8259 and should connect to CPU INTR as a maskable interrupt.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
CPU interface :			
NMI	F18	O-Group E 2.4/2.4 mA	**Non-maskable Interrupt to CPU.** This is generated by the ISA Parity error (IOCHKJ assertion), PCI Parity error or DRAM Parity error (SERRJ assertion), and the other internal error event. This output should connect to CPU NMI as a non-maskable interrupt.
A20MJ	G19	O-Group E 2.4/2.4 mA	**CPU A20 Mask.** This is the CPU Address line 20 mask signal.
FERRJ/ IRQ13	H16	I-Group E	**Floating Point Error.** FERRJ input to generate IRQ13. When Coprocessor interface is disabled through configuration register Index-43h bit 6 setting, the function of this pin is IRQ13.
ISA Bus Interface Unit :			
IRQ[15:14], IRQ[11:9], IRQ[7:3]	U8,W8 W7, U7, K2 U2, T3, U3, T4, U4	I/O Group A Schmitt 9.6/9.6 mA	**Interrupt Request.** The Interrupt Request lines are directly from the ISA Bus, from the PCI Interrupt Routing, or from the steerable Interrupt pins. The M1533 will also drive the interrupt pins if the source is not from the ISA bus to support the APIC interface.
RSTDRV	J2	O-Group A 12/16 mA	**ISA Bus reset.** This output is used to reset the ISA Bus and the system device. This pin will be active if the system reset is needed.
SD[15:8]	Y12, W12, V12, U12, W11, U11, Y10, V10	I/O Group A 12/12 mA	**ISA High Byte Slot Data Bus.** These pins should connect to the ISA High Byte Slot Data Bus.
XD[7:0]	Y15, W15, V15, U15, Y14, W14, V14, U14	I/O Group A 12/12 mA	**XD Data Bus.** When the SD[7:0] pins are defined as the GPIO[7:0] pins, these pins can be used to drive SD[7:0] if TTL LS245 is used as a buffer. M1533 signal XDIR will control this buffer.
SD[7:0]/ GPIO[7:0]	J1, K3, K1, L3, L1, M5, M3, M2	I/O Group A 12/12 mA	**ISA Low Byte Slot Data Bus or General Purpose I/O.** When external SD[7:0] bus is supported by the XD[7:0] bus through a LS245 TTL, these pins are used as the GPIO pins for green control. Otherwise, these pins are SD[7:0]. No external LS245 is required.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
ISA Bus Interface Unit :			
SA[19:17]	N2, P5, P3	O-Group A 12/12 mA	**ISA Slot Address Bus A19-A17.** These pins should connect to the ISA System Address Bus.
SA[16:0]	P1, R4, R2, T2, U1, W1, V2, W2, V3, W3, Y3, V4, W4, Y4, V5, W5, Y5	I/O Group A 12/12 mA	**ISA Slot Address Bus A16-A0.** These pins should connect to the ISA System Address Bus.
SBHEJ	W6	I/O Group A 12/12 mA	**ISA Byte High Enable.** This pin should connect to the ISA System Byte High Enable pin.
LA[23:17]	T7, V7, Y7, T8, V8, Y8, U9	I/O Group A 12/12 mA	**ISA Latched Address Bus.** They are inputs during ISA master cycle and should connect to ISA Slot Latch Address Bus.
IO16J	Y6	I -Group A	**ISA 16 Bit I/O Device Indicator.** This is an input and will be driven by the device if the ISA I/O cycle is a 16-bit access.
M16J	V6	I/O Group A 12/20 mA	**ISA 16 Bit Memory Device Indicator.** This pin will be driven by the device or by the M1533 if the ISA Memory cycle is a 16-bit access.
MEMRJ	W9	I/O Group A 12/12 mA	**ISA Memory Read.** This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
MEMWJ	T10	I/O Group A 12/12 mA	**ISA Memory Write.** This signal is an output when the M1533 is the ISA Bus master, or an input during ISA master cycle.
AEN	N4	O-Group A 12/12 mA	**ISA I/O Address Enable.** This signal will become active high during DMA cycle to prevent I/O device to decode DMA cycles as valid I/O cycles.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
ISA Bus Interface Unit :			
IOCHRDY	M1	I/O Group A 12/20 mA	**ISA System Ready.** This signal is an output during ISA master cycle, or an input when the M1533 is the ISA Bus master.
NOWSJ	M4	I-Group A	**ISA Zero Wait-State for Input.** This input signal will terminate the CPU to ISA command instantly.
IOCHKJ	J3	I-Group A	**ISA Parity Error.** M1533 will generate NMI to CPU when this signal is asserted.
SYSCLK	V1	O-Group A 12/12 mA	**ISA System Clock.** This output is generated by the PCI clock and is used as the ISA system clock.
BALE	T6	O-Group A 12/12 mA	**Bus Address Latch Enable.** BALE will be asserted throughout DMA, ISA master , and the Refresh cycles. Otherwise, it will only assert half the SYSCLK before the ISA command is asserted.
IORJ	P4	I/O Group A 12/16 mA	**ISA I/O Read.** This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
IOWJ	N1	I/O Group A 12/12 mA	**ISA I/O write.** This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
SMEMRJ	N3	O-Group A 12/12 mA	**ISA System Memory Read.** This signal indicates that the memory read command is below 1M Byte address.
SMEMWJ	N5	O-Group A 12/12 mA	**ISA System Memory Write.** This signal indicates that the memory write command is below 1M Byte address.
DREQ[7:5], DREQ[3:0]	Y11, T11, U10 R5, L2, R1	I-Group A Schmitt	**DMA Request Signals.** These are inputs from the DMA Device or ISA Master Request. The M1533 will combine the DMA request, ISA Master request, IDE Bus Master request, and USB Master request to generate the PHOLDJ to the PCI Arbiter.
DACKJ[7:5], DACKJ[3:0]	V11, W10, Y9 P2, T5, R3, T9	O-Group A 9.6/9.6 mA	**DMA Acknowledge Signals.** After the M1533 has got the PCI Bus grant (PHLDAJ), the internal arbiter will assert the DMA acknowledge signal to the DMA Device Request.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
ISA Bus Interface Unit :			
TC	U5	O-Group A 12/12 mA	**DMA End of Process.** This signal will be asserted after the DMA Device has ended the transaction.
REFSHJ	T1	I/O Group A 12/20 mA	**ISA Refresh Cycle.** This signal is an input during ISA master cycle, and an output when the M1533 is the ISA Bus master.
Miscellaneous Logic :			
SPKR	V13	O-Group A 4/4 mA	**Speaker Output.** This pin is used to control the Speaker Output and should connect to the Speaker.
RTCAS	T13	O-Group A 4/4 mA	**RTC Address Strobe.** This pin is used as the RTC Address Strobe and should connect to the RTC.
RTCRW	T14	O-Group A 4/4 mA	**RTC Write strobe.** This pin is used as the RTC Read/Write Command and should connect to the RTC. The M1533 will drive the RTC command through dedicated pin instead of the 74F32 decode to save the system cost.
RTCDS	U13	O-Group A 4/4 mA	**RTC Data Strobe.** This pin is used as the RTC Data Strobe and should connect to the RTC.
SPLED	W13	O-Group A 4/4 mA	**Speed LED Output.** This pin is used to control the Speed LED Output and should connect to LED.
ROMKBCSJ	T12	O-Group A 4/4 mA	**ROM/Keyboard Chip Select.** This pin is the ROM chip select and is the Keyboard chip select also when internal KBC is disabled.
SERIRQ/ GPI[2]	Y18	B/I Group A 12/16 mA	**Serial Interrupt Request or General Purpose Input.** This pin is used to support the serial interrupt protocol or as a General Purpose Input.
SIRQI	N16	I-Group A Schmitt	**Steerable IRQ Input1.** This is a steerable Interrupt input, M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.
SIRQII	N17	I-Group A Schmitt	**Steerable IRQ Input2.** This is a steerable Interrupt input, M1533 will provide a Routing Mechanism to route this Interrupt to any 8259 input.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Miscellaneous Logic :			
IRQ8J	L16	I-Group C Schmitt	**RTC Interrupt Input.** This is the RTC Interrupt input. This pin belongs to the Power Group C, and it can support the RTC Alarm function during Soft-off or Suspend state.
XDIR/ GPO[12]	T16	O-Group A 4/4 mA	**XD Bus Direction Control or General Purpose Output.** When external XD bus is designed on motherboard, this pin is X-bus direction control. Otherwise, this pin is a general purpose output.
KBINH/ IRQ1I	T15	I/O Group A Schmitt 12/24 mA	**Keyboard Inhibit or Interrupt One Input.** This pin will be the Keyboard Inhibit input when internal KBC is enabled. Otherwise, it will be the IRQ1 input.
IRQ1O/ GPO[13]	R20	O-Group A 4/4 mA	**IRQ1 Output or General Purpose Output.** When both external APIC and internal KBC are enabled, this pin is IRQ1 output. Otherwise, it is a general purpose output.
KBCLK/ GPI[9]	L4	I/O Group A Schmitt 12/24 mA	**Keyboard Clock or General Purpose Input.** This pin is the Keyboard interface Clock when internal KBC is enabled. Otherwise, it is a general purpose input.
KBDATA/ GPI[10]	L5	I/O Group A Schmitt 12/24 mA	**Keyboard data or General Purpose Input.** KB interface DATA output when internal KBC is enabled. Otherwise, this pin is a general purpose input.
MSCLK/ GPI[11]	K4	I/O Group A Schmitt 12/24 mA	**Mouse Clock or General Purpose Input.** Mouse clock output when internal PS2 Keyboard is enabled. Otherwise, this pin is a general purpose input.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Miscellaneous Logic :			
MSDATA/ IRQ12I	K5	I/O Group A Schmitt 12/24 mA	**Mouse Data or Interrupt Line 12 Input.** Mouse data output when internal PS2 Keyboard is enabled. Otherwise, this pin is the IRQ12 input.
IRQ12O/ GPO[14]	R19	O-Group A 4/4 mA	**Interrupt Line 12 Output or General Purpose Output.** When both external APIC and internal KBC are enabled, this pin is IRQ12 output. Otherwise, this pin is a general purpose output.
IRQ0/ GPO[15]	R18	O-Group A 4/4 mA	**Interrupt Line 0 Output or General Purpose Output.** This pin is the Interrupt request 0 output when external APIC mode is enabled. Otherwise this pin is a general purpose output.
APICREQJ/ GPI[8]	W19	I -Group A	**APIC Request Input or General Input.** This pin connects to the APIC Chip Request Line when external APIC mode is enabled. Otherwise, this pin is a general purpose input.
APICCSJ/ GPO[16]	R17	O-Group A 4/4 mA	**APIC Chip Select or General Purpose Output.** This pin connects to the APIC Chip Select Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
APICGNTJ/ GPO[17]	R16	O-Group A 4/4 mA	**APIC Grant Output or General Purpose Output.** This pin connects to the APIC Chip Grant Line when external APIC mode is enabled. Otherwise, this pin is a general purpose output.
BIOSA17/ GPO[19]	P16	O-Group A 4/4 mA	**ROM Address 17 or General Purpose Output.** This pin is the ROM A17 control when 2M ROM is used, or it is a general purpose output.
BIOSA16/ GPO[18]	P17	O-Group A 4/4 mA	**ROM Address 17 or General Purpose Output.** This pin is the ROM A16 control when 2M ROM is used, or it is a general purpose output.
PCSJ/ GPO[0]	U20	O-Group A 4/4 mA	**Programmable Chip Select or General Purpose Output.** This pin can be selected as a Programmable Chip Select, or as a general purpose output.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
IDE interface :			
PIDE_DRQ	G16	I-Group D	**Primary IDE DMA Request for IDE Master.** This is the input pin from the Primary Channel IDE DMA request to do the IDE Master Transfer.
SIDE_DRQ	E14	I-Group D	**Secondary IDE DMA Request for IDE Master.** This is the input pin from the Secondary Channel IDE DMA request to do the IDE Master Transfer.
PIDE_AKJ	E17	O-Group D 9.6/9.6 mA	**Primary IDE DACKJ for IDE Master.** This is the output pin to grant the Primary Channel IDE DMA request to begin the IDE Master Transfer.
SIDE_AKJ	A14	O-Group D 9.6/9.6 mA	**Secondary IDE DACKJ for IDE Master.** This is the output pin to grant the Secondary Channel IDE DMA request to begin the IDE Master Transfer.
PIDE_RDY	F17	I-Group D	**Primary IDE Ready.** This is the input pin from the Primary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
SIDE_RDY	B14	I-Group D	**Secondary IDE Ready.** This is the input pin from the Secondary IDE Channel to indicate the IDE device is ready to terminate the IDE command. The IDE device can de-assert this input (logic 0) to expand the IDE command if the device is not ready.
PIDEIORJ	G17	O-Group D 12/12 mA	**Primary IDE IORJ Command.** This is the IORJ command output pin to notify the Primary IDE device to assert the Read Data.
SIDEIORJ	C14	O-Group D 12/12 mA	**Secondary IDE IORJ Command.** This is the IORJ command output pin to notify the Secondary IDE device to assert the Read Data.
PIDEIOWJ	F16	O-Group D 12/12 mA	**Primary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Primary IDE device that the available Write Data is already asserted by M1533.
SIDEIOWJ	D14	O-Group D 12/12 mA	**Secondary IDE IOWJ Command.** This is the IOWJ command output pin to notify the Secondary IDE device that the available Write Data is already asserted by M1533.
PIDECS1J	E18	O-Group D 9.6/9.6 mA	**IDE Chip Select 1 for Secondary Channel 0.** This is the Chip Select 1 command output pin to enable the Primary IDE device to watch the Read/Write Command.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
IDE interface :			
PIDECS3J	E19	O-Group D 9.6/9.6 mA	**IDE Chip Select 3 for Secondary Channel 1.** This is the Chip Select 3 command output pin to enable the Primary IDE device to watch the Read/Write Command.
SIDECS1J	B15	O-Group D 9.6/9.6 mA	**IDE Chip Select 1 for Primary Channel 0.** This is the Chip Select 1 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
SIDECS3J	A15	O-Group D 9.6/9.6 mA	**IDE Chip Select 3 for Primary Channel 1.** This is the Chip Select 3 command output pin to enable the Secondary IDE device to watch the Read/Write Command.
PIDE_A[2:0]	D20, D18, D19	O-Group D 9.6/9.6 mA	**Primary IDE ATA Address Bus.** These are the Address pins connected to Primary Channel.
SIDE_A[2:0]	C15, E15, D15	O-Group D 9.6/9.6 mA	**Secondary IDE ATA Address Bus.** These are the Address pins connected to Secondary Channel.
PIDE_D[15:0]	C19, B20, B18, D17, B17, A17, B16, D16, E16, A16, C16, C17, A18, B19, C18, C20	I/O Group D 9.6/9.6 mA	**Primary IDE ATA Data Bus.** These are the Data pins connected to Primary Channel.
SIDE_D[15:0]	A13, C13, E13, B12, D12, A11, C11, E11, A10, D11, B11, E12, C12, A12, D13, B13	I/O Group D 9.6/9.6 mA	**Secondary IDE ATA Data Bus.** These are the Data pins connected to Secondary Channel.
Power Management Unit :			
RSM_RSTJ	M18	I-Group C Schmitt	**Resume Circuit Initial Reset Input.** This input is used to initialize the resume circuit.
SMIJ	F19	O-Group E 4/4 mA	**SMM Interrupt Output.** This output should be connected to CPU SMM Interrupt input.
STPCLKJ	H17	O-Group E 4/4 mA	**Stop CPU Internal Clock Output.** This output is used to stop the CPU internal clock and should be connected to CPU STPCLKJ input.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Power Management Unit :			
SLEEPJ/ GPO[20]	J17	O-Group E 4/4 mA	**Pentium PRO Sleep State or General Purpose Output.** This output will force Pentium PRO CPU to enter Sleep State, or as a general purpose output.
ZZ/ GPO[1]	J16	O-Group E 4/4 mA	**PBSRAM Power Saving Mode or General Purpose Output.** This output is used to control L2 cache entering power saving mode, or as a general purpose output.
CLKRUNJ	D10	I/O - Group B 12/16 mA	**PCI Clock Stop Message Control.** This pin is used to support PCI Clock Run function.
CPU_STPJ/ GPO[2]	H5	O-Group B 4/4 mA	**Clock Cell CPU Clock Stop or General Purpose Output.** This output is used to stop the CPU Clock of the clock generator, or as a general purpose output.
PCI_STPJ/ GPO[3]	H4	O-Group B 4/4 mA	**Clock Cell PCI Clock Stop or General Purpose Output.** This output is used to stop the PCI Clock of the clock generator, or as a general purpose output.
SUSTAT1J	L17	O-Group C 4/4 mA	**Suspend Status for North Bridge.** This output is used to notice the north bridge to control DRAM suspend refresh circuit.
SLOWDWN/ GPO[4]	G3	O-Group B 4/4 mA	**Slow Down the Clock Generator Output or General Purpose Output.** This output is used to control the Clock Generator to slow down the clock output, or as a general purpose output.
AMSTATJ/ GPO[8]	F2	O-Group B 4/4 mA	**APM State Control.** It is asserted when HALT or STPGNT cycle is detected.
PWRBTNJ	L18	I-Group C Schmitt	**Power Button Input.** This input is used to support the ACPI Power Button function.
PCIREQJ/ GPI[3]	H3	I-Group B	**PCI Bus Request Event Input or General Purpose Input.** This input comes from the North Bridge or external circuit to notice M1533 there is PCI request pending. This pin can also be programmed as a general purpose input.
POSSTA/ GPI[4]	W17	I -Group A	**Force M1533 into Suspend Mode or General Purpose Input.** This input can be used to force M1533 entering suspend mode, or as a general purpose input.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Power Management Unit :			
SQWO/ GPO[9]	T19	O-Group A 4/4 mA	**Square Wave Output or General Purpose Output.** This output can be used to output Square Wave with 1Hz or 2Hz, or as a general purpose output.
OFF_PWR0/ GPO[21]	P20	O-Group C 4/4 mA	**Remove Clock Generator Power Control or General Purpose Output.** This output can be used to remove the Clock Generator Power, or as a general purpose output.
OFF_PWR1/ GPO[22]	P19	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit and External DRAM or General Purpose Output.**
OFF_PWR2/ GPO[23]	P18	O-Group C 4/4 mA	**Remove All Circuit Power Except Internal Suspend Circuit or General Purpose Output.**
RI	H20	I -Group C Schmitt	**Ring-in or General Purpose Input.** This input connects to Modem Ring-in input to support ACPI Ring-in function, or as a general purpose input.
LBJ	M19	I -Group C Schmitt	**First Battery Low Indication Input or General Purpose Input.** This input can be used as the first stage battery low level indication, or as a general purpose input signal.
LLBJ	K16	I -Group C Schmitt	**Last Battery Low Indication Input or General Purpose Input.** This input can be used as the last battery low level indication, or as a general purpose input signal.
EXTSW	Y13	I -Group A Schmitt	**External Switch Event or General Purpose Input.** EXTSW is a triggered input to the M1533 showing that an external device is requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
THRMJ	Y16	I -Group A Schmitt	**Thermal Event Input or General Purpose Input.** THRMJ is a triggered input to the M1533 showing that the external thermal detected circuits are requesting the system to enter power management mode. This signal also can be used optionally as a general purpose input signal.
ACPWR	V16	I - Group A Schmitt	**Detect AC Adapter Plug-in or General Purpose Input.** This is a triggered input showing that the AC adapter is plugged in or plugged out event. This triggered event can be used as a system management (or control) interrupt source. This signal also can be used optionally as a general purpose input signal.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Power Management Unit :			
CRT	Y17	I -Group A Schmitt	**Detect CRT Connector Plug-in or General Purpose Input.** This signal represents whether the external CRT connector is plugged in/ plugged out, or used as a general purpose input.
SETUPJ	W16	I -Group A	**Setup Switch Input or General Purpose Input.** This signal can be used as a setup switch triggered input for generating the power management interrupt event, or as a general purpose input signal.
EJECT	U16	I -Group A	**External Eject SMIJ Trigger or General Purpose Input.** This triggered input is used as an eject (undocking) event indicator, or as a general purpose input signal.
LID	M20	I -Group C	**Cover Switch Input or General Purpose Input.** This signal is used to indicate if the system's lid is open or closed, or as a general purpose input.
HOTKEYJ	M17	I -Group C Schmitt	**Hot Key Press Event Input or General Purpose Input.** This input signal is used to indicate a hot key press event occurred or not, or as a general purpose input.
DOCKJ	K17	I-Group C	**Docking Insert Event Input or General Purpose Input.** This triggered input is used as a docking event indicator, or as a general purpose input signal.
VCSJ/ GPI[5]	Y19	I-Group A	**VGA Activity Event Input or General Purpose Input.** The VGA chip should set this signal to active low when an VGA memory access occurred. This active signal is used by the M1533 to reload the VGA monitor timer or to generate a system management event. This signal also can be used as a general purpose input.
FPVEE/ GPI[6]	V17	I-Group A	**LCD Back Light VEE Input or General Purpose Input.** This signal is used by the M1533 to generate DISPLAY and a programmable CCFT signals. This signal also can be used as a general purpose input.
CCFT/ GPO[5]	U19	O-Group A 4/4 mA	**Back Light Control or General Purpose Output.** This signal can be programmed to be a periodical wave controlled by the FPVEE signal or kept to static low level. This signal also can be used as a general purpose output.
DISPLAY/ GPO[6]	U18	O-Group A 4/4 mA	**LCD Display On/Off Control or General Purpose Output.** This signal can be programmed to be a response controlled by the FPVEE signal, or it can also be used as general purpose output.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Power Management Unit :			
CONTRAST/ GPO[7]	T20	O-Group A 4/4 mA	**LCD Contrast Control or General Purpose Output.** It is a 1KHz signal with programmable duty cycle and can be used to control LCD contrast. It can also be a general purpose output.
GPIORBJ/ GPO[10]	V20	O-Group A 4/4 mA	**Input Event Latching into External Buffers Command or General Purpose Output.** This signal can be used as an external buffer(s) latching command for extended general inputs, or as a normal general purpose output signal.
GPIOWB/ GPO[11]	T17	O-Group A 4/4 mA	**Output Control Signal Latching into External Buffers Command or General Purpose Output.** This signal can be used as an external buffer(s) latching command for extended general outputs, or as a normal general purpose output signal.
GPIO[19:16]	J18, J19, J20, K18	I/O Group C Schmitt 4/4 mA	**General Purpose I/O Pins for Resume from Suspend Mode.** These signals can be programmed as the inputs or outputs for the resume triggered events from the suspend mode.
GPIO[15:12]/ BATSEL[3:0]	K19, K20, L19, L20	I/O Group C Schmitt 4/4 mA	**General Purpose I/O Pins or SM Bus Battery Select.** These signals can be used as the general purpose I/O pins, or as the external SMB battery select control signals.
GPIO[11:8]	U17, V20, V19, V18	I/O Group A Schmitt 4/4 mA	**General Purpose I/O Pins for Wake-up from Stand-by Mode.** These signals can be programmed as the inputs or outputs for the wake-up triggered events from the standby mode.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
USB interface :			
USBP0+ USBP0-	G2 G1	I/O Group B	**Universal Serial Bus Port 0.** These are the serial data pair for USB Port 0.
USBP1+ USBP1-	H2 H1	I/O Group B	**Universal Serial Bus Port 1.** These are the serial data pair for USB Port 1.
OVCRJ[1:0]/ GPI[1:0]	J4, J5	I -Group B	**Over Current Detect Inputs or General Purpose Inputs.** These two pins are used to monitor the USB Power Over Current, or as two general purpose inputs.
SM Bus signal :			
SMBEVENTJ/ GPI[7]	W18	I-Group A Schmitt	**SM Bus Resume Event or General Purpose Input.** This signal can be used as the SM Bus resume event indicator, or as a general purpose input.
SMBCLK	H19	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Clock.** SM Bus clock signal should be combined with SM Bus data to carry information between the devices connected to the SM Bus.
SMBDATA	H18	I/O-Group C Schmitt 9.6/9.6 mA	**SM Bus Data Line.** SM Bus data signal should be combined with SM Bus clock to carry information between the devices connected to the SM Bus.
Power Pins :			
VCC_A	R15, R7, P6	P	**Vcc 3.3V or 5V for Power Group A.** This power is used for ISA interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power connects to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3A	R14	P	**Vcc 3.3V for Power Group A.** This power is used for ISA interface. If Vcc_A is selected as 3.3V, this power pin connects with Vcc_A to 3.3V power plane. If Vcc_A is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_B	F6, G6	P	**Vcc 3.3V for Power Group B.** This power is used for PCI interface. It must be connected to 3.3V. The relative signals will output 3.3V and 5V input tolerance.

Pin Description Table (continued) :

Pin Name	Pin No.	Type	Description
Power Pins :			
VCC_C	P15	P	**Vcc 3.3V or 5V for Power Group C.** This power is used for resume/ suspend control interface signals during normal operation and suspend periods. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_3C	G15	P	**Vcc 3.3V for Power Group C.** This power is used for Resume/Suspend Control interface. If Vcc_C is selected as 3.3V, this power pin connects with Vcc_C to 3.3V power plane. If Vcc_C is selected as 5V, this power pin should connect to 3.3V power plane to save power consumption.
VCC_D	F14	P	**Vcc 3.3V or 5V for Power Group D.** This power is used for IDE interface. If this power is connected to 3.3V, the relative signals will output 3.3V and accept 5V input tolerance. If this power is connected to 5V, the relative signals will output 5V TTL and accept TTL input.
VCC_E	F15	P	**Vcc 3.3V or 2.5V for Power Group E.** This power is used for CPU interface. If this power connects to 3.3V, the relative signals will output 3.3V and accept 3.3V input. If this power connects to 2.5V, the relative signals will output 2.5V and accept 2.5V input.
VDD_5	R6	P	**Vcc 5.0V for core Power.** It supplies the core power for the internal circuit except the suspend circuit.
VDD_5S	N15	P	**Vcc 5.0V for Suspend/Resume Core Power.** It supplies the core power for the internal suspend/resume circuit.
Vss or Gnd	H[8:13], J[8:13], K[8:13], L[8:13], M[8:13], N[8:13]	P	**Ground.**

2.3. ATI 264GT (3D RAGE II+DVD)

The *mach64* 3D RAGE™ (also known as the GT) is a 208-pin VLSI video graphics controller chip with built-in 3D coprocessor, GUI coprocessor, video scaler, color space converter, True Color palette DAC, and dual-clock synthesizer. This controller is 100% register-compatible with the IBM VGA display adapter.

The GT supports synchronous graphics memory chips SDRAM/SGRAM. When combined with the 64-bit memory interface and memory clocks up to 63 MHz, the available bandwidth can reach 800 MB/sec. This increase in memory bandwidth allows for greater display resolutions and uncompromising video playback capabilities. The GT also supports DRAM and EDO DRAM.

Both footprint and pinout of the GT are backward compatible with the ATI-264CT (CT) and ATI-264VT (VT).

2.3.1 Features

2.3.1.1 3D Accelerator

- Complete 3D primitives-Points, Lines, Triangles, Trapezoids, and Rectangles
- Full-screen or window double buffering for smooth animation
- Flat and Gouraud shading
- Dithering down to 8 or 16 bits per pixel (bpp) from 24 bpp 3D engine for smaller memory foot print
- Texture mapping
    - Hardware perspective correction
    - Sub-pixel accuracy
    - Mip-mapping
    - Bi-linear and tri-linear filtering
    - Texture maps up to 1024x1024
    - Non-square texture maps
    - Alpha in texture map
    - Video textures using YUV format
- 3D effects
    - Alpha blending and alpha interpolation
    - Fogging and fog interpolation

- Texture lighting modes

- 3D modes
    - ARGB32 (8:8:8:8)
    - ARGB16 (1:5:5:5)
    - RGB16 (5:6:5)
    - RGB8 (3:3:2)
    - Y8 gray scale
    - ARGB16 (4:4:4:4)
    - YUV444, YUV422

2.3.1.2 2D Accelerator

- Hardware acceleration-Rectangle Fill, Line Draw, BitBlt, Polygon Fill, Panning/Scrolling, Bit Masking, Monochrome Expansion, Scissoring, and full ROP support

- Hardware cursor up to 64 x 64 x 2

- Acceleration provided in 4/8/16/24/32-bpp modes. Packed pixel support (24 bpp) enables true color in IMB configurations

- Game acceleration for Microsoft's DirectDraw-Double Buffering, Virtual Sprites, Transparent Blit, Masked Blit, and Context Chaining

2.3.1.3 Video Accelerator

- Filtered horizontal and vertical scalers for TV-quality, full-screen video playback

- Integrated video line buffers support filtered video scaling

- Color interpolation during scaling for improved high resolution video quality

- YUV to RGB color space conversion with support for both packed and planar

- Graphics and video keying for effective overlay of video and graphics

- AMC supports I2C interface for special applications (i.e., video tuner control)

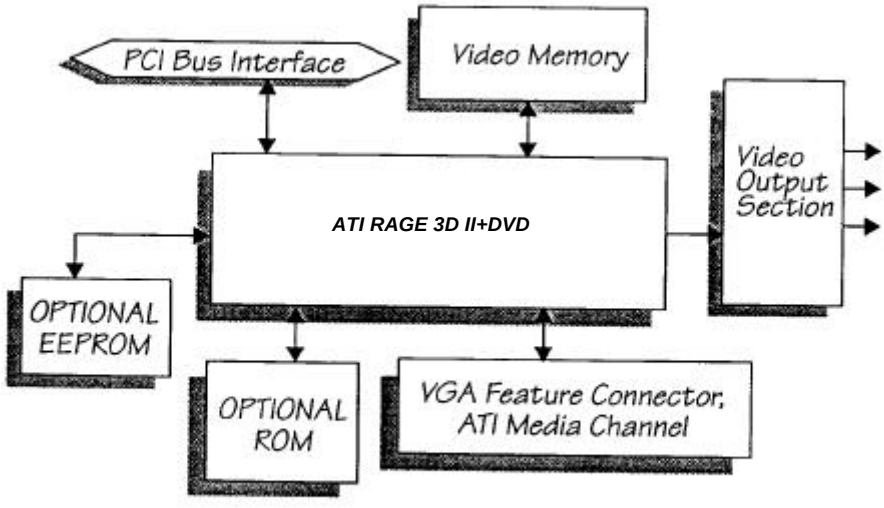
- Supports ATI Media Channel (AMC) 1.0 for additional video expansion capabilities

- Support for 26-pin VESA compatible VGA Feature Connector (VFC) that supports up to 1024 x 768 resolution

2.3.1.4 General Features

- First graphics controller to integrate 3D, 2D, and Video accelerators with palette DAC and dual-clock synthesizer in a single chip
- 24-bit, true-color palette DAC
    - Supports pixel clock rates to 1280 x 1024 resolution at 75-Hz refresh
    - Gamma correction for true WYSIWYG color
    - Full 24-bit palette
- PCI revision 2.0 bus for Plug-and-Play ease of use
- Bi-endian support for compliance on a variety of processor platforms
- 32-level command FIFO assures fast response to host command transfers for maximum CPU/host bus/controller efficiency and concurrent operation
- Software interface including:
    - Programmable flat- or paged-memory model with enhanced host access to a linear frame buffer
    - 32-bit wide read/writable memory mapped registers with optimized organization to reduce instruction overhead and raises performance
- DDCI and DDC2B Plug-and-Play monitor support
- Power management for full-VESA Display Power Management Signaling (DPMS) and EPA Energy Star compliance. Also, register support for controller power reduction and DAC power down
- Optional EEPROM for storing user-selectable configurations
- Single-chip solution in 208-pin PQFP package, 0.511m, mixed 3.3V/5.0V
- supports fast page mode DRAM and EDO DRAM at up to 63MHz memory clock across a 64-bit memory interface
- 3D driver support
    - Microsoft Direct 3D including support for Reality Lab and OpenGL
    - Apple QuickDraw 3D and TinselTown 3D interface
    - ATI 3D RAGE DOS and Windows API
    - Intel 3DR
- Easy-to-use Windows utilities

2.3.2 Block Diagram



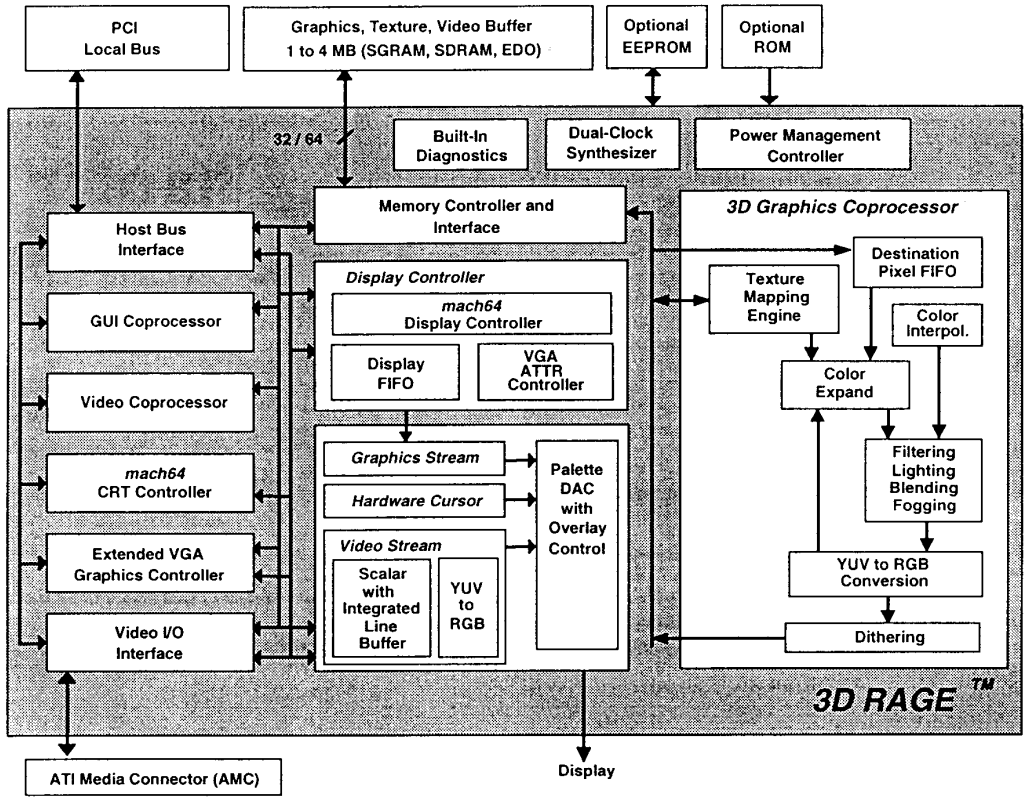


Figure 2-9 264GT Block Diagram

2.3.3 Pin Diagram

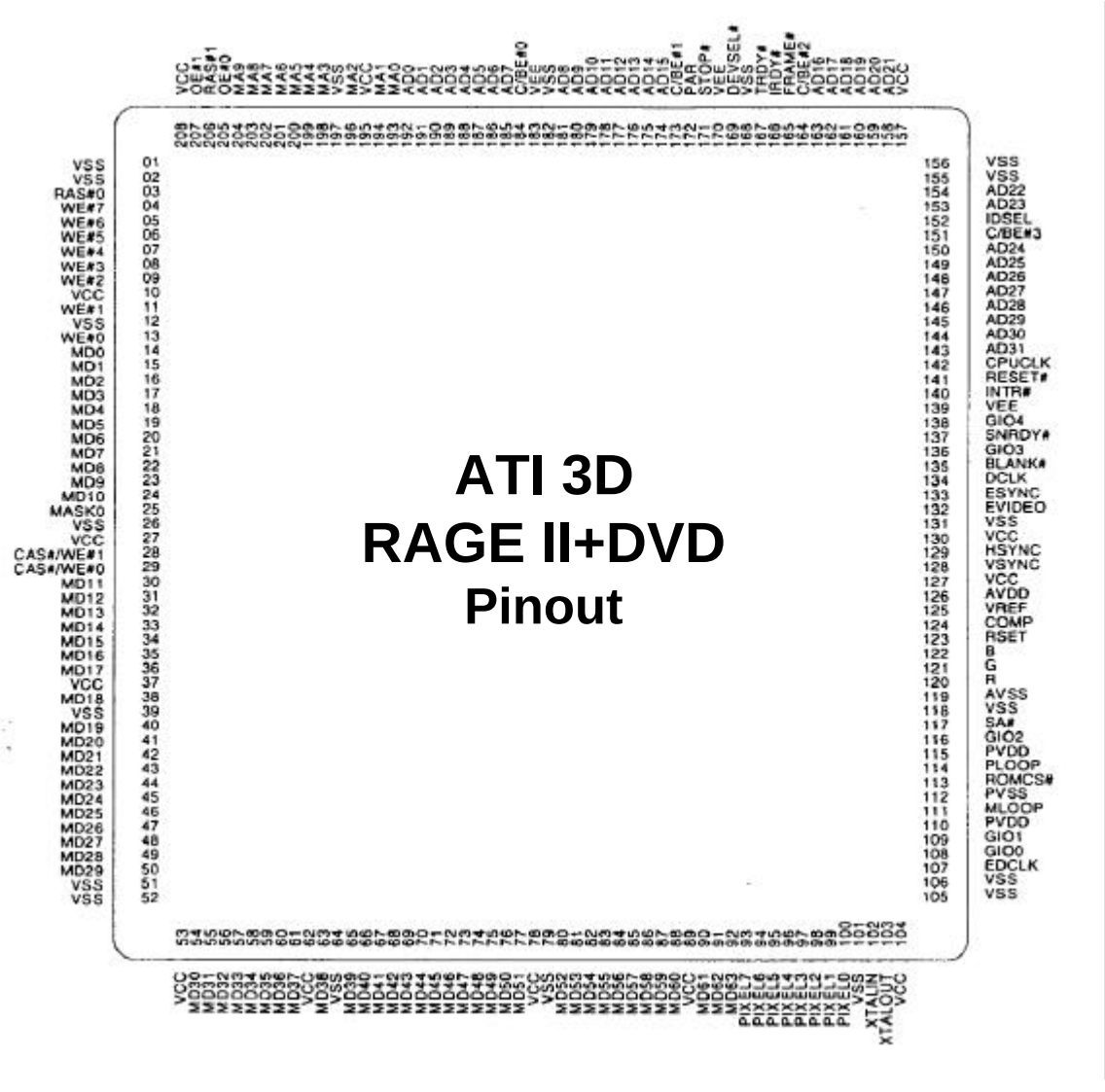


Figure 2-10 264GT Pin Diagram

2.3.4 Signal Descriptions

Table 2-9 264GT Parameter Descriptions

Code	Description
O	Output pin
1/0	Bidirectional pin
Pwr	Power pin
Gnd	Ground pin
A	Analog pins
#	Active-low signal

Table 2-10 264GT Signal Descriptions

Signal	Pin	Type	Description
PCI Bus Interface Implementation (for 5V PCI interface support)			
AD[31 :0]	143:150, 153:154, 158:163, 174:181, 185:192	I/O	Multiplexed-System Address or Data bits [31:0]
C/BE#[3:0]	151,164, 173,184	I	Multiplexed-Bus Command or Byte Enable bits 3:0. (BE# is active low)
CPUCLK	142	I	Bus Clock
DEVSEL#	169	O	Device Select. When driven active, it indicates that the controller has decoded its address.
FRAME#	165	I	Frame is driven by the current bus master to indicate the beginning and duration of an access.
IDSEL	152	I	Initialization Device Select. Used as a chip select during configuration read and write transactions.
INTR#	140	O	Interrupt Request-Level triggered Active low by default
IRDY#	166	I	Initiator Ready - Indicates that the bus master is able to complete the current data phase of the transaction
PAR	172	O	Parity: Even parity used
RESET#	141	I	Bus Reset
STOP#	171	O	Stop. Indicates that the current target is requesting the master to stop the current transaction
TRDY#	167	O	Target Ready. Indicates the the target agent is able to complete the current data phase of the transaction

Table 2-10 264GT Signal Descriptions

Signal	Pin	Type	Description
Memory Interface			
CAS#/WE#0	29	O	Write Strobe of the first and second MB of memory
CS#3/WE#1	28	O	Write Strobe of the third and fourth MB of memory
MA[9:0]	204:198, 196, 194:193	O	Memory Address bits 9:0
MD[31 :0]	55:54, 50:40, 38, 36:30, 24:14,	I/O	Memory Data bits 31:0 of the first and third MB of memory
MD[63:32]	92:90, 88:80, 77:65, 63, 61:56	I/O	Memory Data bits 63:32 of the second and fourth MB of memory
OE#0	205	O	Output Enable of the first and second MB of memory
OE#1	207	O	Output Enable of the third and fourth MB of memory
RAS#0	3	O	Row Address Strobe of the first and second MB of memory
CS#2	206	O	Row Address Strobe of the third and fourth MB of memory
WE#[7:0]	4:9,11, 13	I/O	Column Address Strobe
SDRAM Memory 128KBx16x2, and x32x2			
CAS#/WE# [1 :0]	28,29	O	CAS[1:0]
MA[9:0]	204:198, 196,194, 193	O	MA[9:0]
MD[63:0]	92:90, 88:80, 77:65, 63, 61 :54, 50:40, 38, 36:30, 24:14	I/O	AD[63:0]
OE#1	205	O	WE# Command
OE#0	207	O	MCLK
RAS#[1:0]	3, 206	O	RAS[1:0]
WE#[7:0]	4:9,11, 13	O	DQM[7:0]
DAC and Monitor Interface			
R	120	A	Red analog pixel data output to monitor
G	121	A	Green analog pixel data output to monitor
B	122	A	Blue analog pixel data output to monitor
COMP	124	A	Compensation pin for the DAC
HSYNC	129	O	Horizontal Sync
VSYNC	128	O	Vertical Sync
DAC and Monitor Interface			

Table 2-10 264GT Signal Descriptions

Signal	Pin	Type	Description
RSET	123	A	Current-Setting Resistor for the DAC
VREF	125	A	DAC Reference Voltage
Frequency Synthesizer Interface			
MLOOP	111	A	Memory Clock Loop filter
PLOOP	114	A	Pixel Clock Loop filter
XTALIN*	102	A	14.31818-MHz crystal or TTL oscillator connection
XTALOUT*	103	A	14.31818-MHz crystal connection
Optional ATI Media Channel Interface			
BLANK#	135	0	Blank Signal
DCLK	134	0	Pixel Clock Output
EDCLK	107	I	Enable Pixel Clock
ESYNC	133	I	Enable Sync
EVIDEO	132	I	Enable Pixel Data
PIXEL[7:0]	93:100	0	Pixel Data Output
SA#	117	I/O	Serial I/O, Interrupt Request
137		I/O	Slave Not Ready
MASKO	25	I/O	Pixel Mask
Optional EEPROM Interface			
GI01	109	I/O	EEPROM Clock
GI02	116	I/O	EEPROM Data I/O
GI03	136	0	EEPROM Chip Select
MD [46:32]	72:65, 63, 61:56	I/O	EPROM Address Bus
Optional EEPROM Interface			
MD [63:56]	92:90, 88:84	I/O	EPROM Data Bus
ROMCS#	113	O	ROM Chip Select
Optional EEPROM Interface (Monitor ID for DDC Support)			
GIO0	108	I/O	DDC Serial Data
GI04	138	I/O	DDC Serial Clock

* For designs using an external clock source (instead of a crystal): the input XTALIN is CMOS inverter with Cjn = 0.5pF; XTALOUT is not connected.

Table 2-10 264GT Signal Descriptions

Signal	Pin	Type	Description
Power and Ground Pins			
AVDD	126	PWR	DAC Analog Power
AVSS	119	GND	DAC Analog Ground
PVDD	110, 115	PWR	PLL Power
PVSS	112	GND	PLL Ground
VCC	10,27, 37,53, 62,78, 127,130, 157,195, 208	PWR	3.3V Power
VEE	139,170, 183	PWR	5.0V Power
VSS	1,2,12, 26,39, 51,52, 64,79, 101,105, 106,118, 131,155, 156,168, 182,197	GND	Ground

2.4. CT2510

The Creative ViBRA™ 16X VLSI chip is a high-performance stereo codec 16-bit device that utilizes 2 ADC's and 4 DAC's based on the latest Sigma-Delta. The 2 ADC are used for stereo audio conversion, while the 4 DAC are split into 2 functions: 2 for stereo MIDI synth and 2 for stereo audio conversion. This solution is Sound Blaster™ 16 compatible, Roland MPU401 UART mode compatible and fully compliant with Multimedia PC Level 2 and 3 specifications.

The chip contains the following sub-block functions:

- ISA 8-bit data bus interface
- ISA 16-bit I/O addressing
- Full-duplex DMA allowing 16-bit data for record and playback
- Plug-and-Play support
- Digital audio processor
- High-performance 16-bit Sigma Delta Stereo codec
- Sound Blaster™ 16 compatible mixer
- Music synthesizer (CQM™) with stereo DAC

- Frequency synthesizer utilizing a 14.31818-MHz clock

- Joystick Quad timer

The ViBRA™ 16x, CT2510 bus interface contains the necessary interface circuits between the ISA bus and all the other functional blocks of the chip. This includes 16-bit I/O address decoding; control logic for the Interrupt and DMA string. It also provides MPU401 compatibility, FIFO's for digital audio recording and playback, format conversions for the ADC/DAC, and the logic for providing Full-duplex operation in the following modes: 16-bit/16-bit, 8-bit/8-bit, 16-bit/8-bit for playback and recording.

The Plug-and-Play interface block contains the necessary interface circuits for the protocol communication to the operating system and the ROM that contains the configuration information of the ViBRA™ 16x. This design meets the configuration information of the ViBRA™ 16x and the requirements set forth by PnP Specification. The PnP information is located in ROM inside the part. There is also support for an external EEPROM to provide the configuration information. The external EEPROM is utilized for add-on card applications or for those designs that require resource information different than the internal ROM provides.

2.4.1 Features

- Complete 16-bit audio VLSI single-chip solution

- Sound Blaster™ 16 compatible

- Mixed digital and analog high-performance chip

- Integrated CQMTM

- Integrated frequency synthesizer

- Plug-and-Play support

- Full-duplex DMA allowing 8-bit or 16-bit data for recording and playback

- Stereo-enhancement support

- Advanced Power Management

- Roland MPU401 UART mode compatible

- Fully MPC, MPC II, and MPC III compatible

- 5V operation for both digital and analog portions

- 100-pin TQFP

- Analog
    - Analog mixing of 7 audio sources
        - Digital audio (stereo)
        - CD audio (stereo)
        - Synthesized music (stereo)
        - Line level audio (stereo)
        - Auxiliary level audio (stereo)
        - Microphone level audio (mono)
    - Mono audio (mono)
    - Individual software programmable volume controls
    - Mixer controlled recording and source selection
    - Programmable gain control for microphone level audio
    - Integrated high-performance 16-bit stereo Sigma Delta codec
    - Dynamic filtering for digital audio recording and playback
    - External volume control of master volume
- Digital
    - Built-in micro-controller unit to ensure full compatibility
    - Built-in PnP interface
    - Full-duplex record and playback
    - 8/16-bit stereo/mono digital audio playback and recording
    - FIFO's for digital audio playback and recording for optimum Windows operations
    - Independent block length for 8 and 16-bit DMA transfers
    - Type-F and Demand mode DMA
    - Accepts signed and unsigned integer format for digital audio PCM data
    - Variable sampling rates from 5 KHz to 48 KHz
- Other peripherals
    - Built-in analog joystick quad timer
- Mixer
    - 32-level volume control mixer
- Codec

- 16-bit Sigma Delta Stereo A/D, D/A converter
- Sampling Rate of 5 KHz to 48 KHz

- CQMTM music synthesizer and DAC
  - Creative Music synthesizer
  - 16-bit Sigma Delta Stereo D/A converter

- Stereo enhancement
  - Built-in Creative stereo enhancement
  - Supports enhancement effect on all inputs to the mixer CD audio, Line-in, Auxiliary, VOC, MIDI, Mic, or Mono

- PnP
  - Built-in PnP
  - PnP controlled decoding and enabling functions
  - PnP resource contained in internal ROM
  - External PnP EEPROM used, if pin SROMSEL is pulled low.
  - PnP logical devices are:
    - Logical device 0-SB, MPU-401, Music synthesizer
    - Logical device 1 - Gameport (Programmable IO base - 8 choices of I/O space between 200-20Fh)
  - Supports direct connection to the ISA bus

2.4.2 Pin Diagram

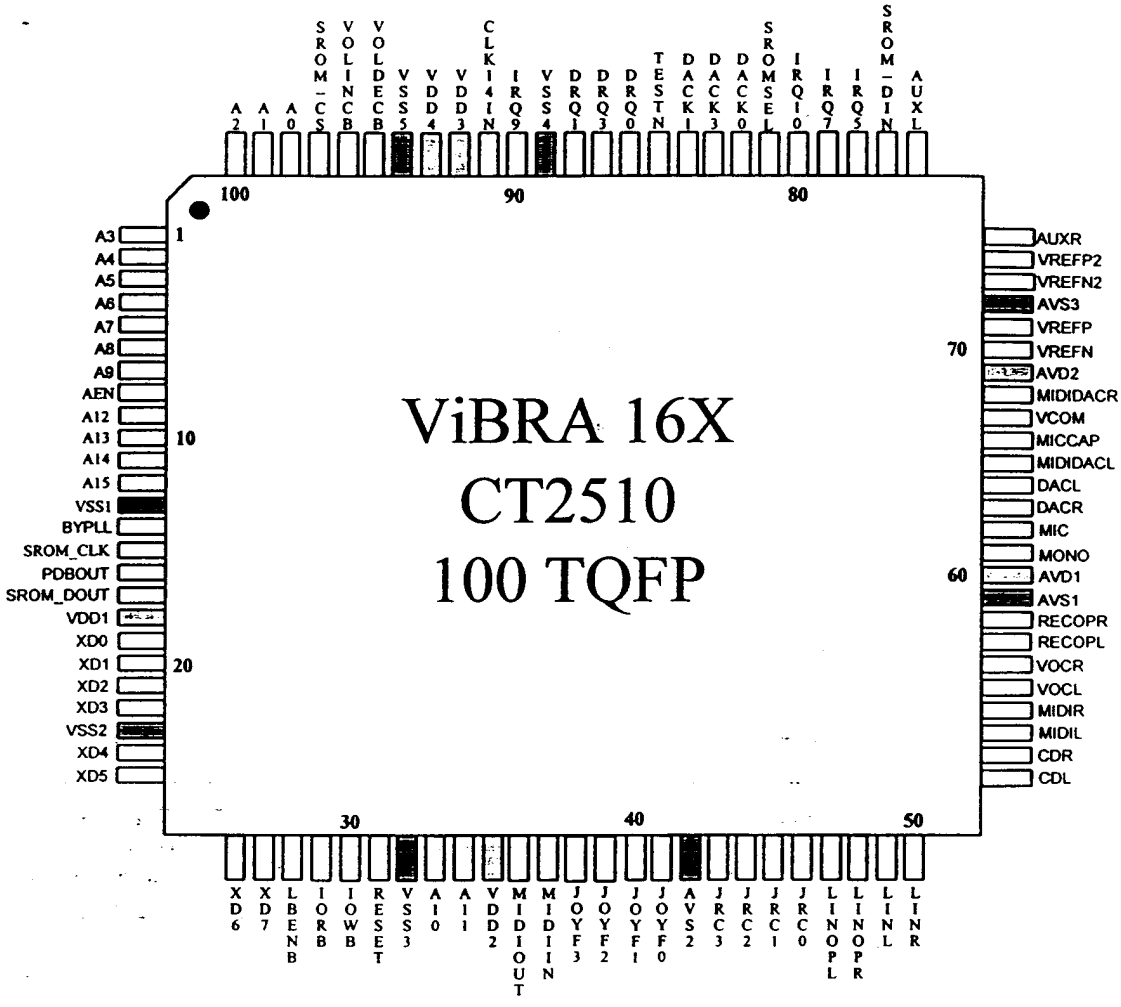


Figure 2-5 CT2510 Pin Diagram

2.4.3 Signal Descriptions

Table 2-6 CT2510 Signal Descriptions

Name	No.	IO	Type	Function	Description
A<3>	1	DI	S	System Address Input	TTL, Schmitt Input
A<4>	2	DI	S	System Address Input	TTL, Schmitt Input
A<5>	3	DI	S	System Address Input	TTL, Schmitt Input
A<6>	4	DI	S	System Address Input	TTL, Schmitt Input
A<7>	5	DI	S	System Address Input	TTL, Schmitt Input
A<8>	6	DI	S	System Address Input	TTL, Schmitt Input
A<9>	7	DI	S	System Address Input	TTL, Schmitt Input
AEN	8	DI			TTL, Schmitt Input
A<12>	9	DI		System Address Input	TTL, Schmitt Input
A<13>	10	DI		System Address Input	TTL, Schmitt Input
A<14>	11	DI		System Address Input	TTL, Schmitt Input
A<15>	12	DI	S	System Address Input	TTL, Schmitt Input
VSS1	13	PWR		Digital Ground	
BYPLL	14	DI		ByPass PLL, active LOW	
SROM_CLK	15	DO		EEPROM CLK	CMOS Output 4mA
PDBOUT	16	DO		Power Down Output, active LOW	TTL, 4mA
SROM_DOUT	17	DI	S	EEPROM DOUT	TTL input schmitt
VDD1	18	PWR		Digital Power	
XD<0>	19	DIO	S	Data Bus	For XD<7:0>
XD<1>	20	DIO	S	Data Bus	TTL I/O
XD<2>	21	DIO	S	Data Bus	TTL Schmitt Input
XD<3>	22	DIO	S	Data Bus	16mA TTL Output
VSS2	23	PWR		Digital Ground	
XD<4>	24	DIO	S	Data Bus	
XD<5>	25	DIO	S	Data Bus	
XD<6>	26	DIO	S	Data Bus	
XD<7>	27	DIO	S	Data Bus	
LBENB	28	DO		XD<7:0>Data buffer enable	CMOS output 4mA
IORB	29	DI	S	System IO read input	TTL schmitt input
IOWB	30	DI	S	System IO write input	TTL schmitt input
RESET	31	DI	S	System Reset input, active HIGH	TTL schmitt input
VSS3	32	PWR		Digital Ground	
A<10>	33	DI	S	System Address Input	TTL, schmitt Input
A<11>	34	DI	S	System Address Input	TTL, Schmitt Input
VDD2	35	PWR		Digital Power	

Table 2-6 CT2510 Signal Descriptions

Name	No.	IO	Type	Function	Description
MIDIOUT	36	DIDO		Serial MIDI Data Output	CMOS output 8mA
MIDIIN	37	DI	S	Serial MIDI Data Input	TTL
JOYF3	38	DI	S	Game-Port Firing Button	TTL
JOYF2	39	DI	S	Game-Port Firing Button	TTL
JOYF1	40	DI	S	Game-Port Firing Button	TTL
JOYF0	41	DI	S	Game-Port Firing Button	TTL
AVS2	42	PWR		Analog Ground	
JRC3	43	AI		Game-Port	For JRC<3:0>
JRC2	44	AI		Game-Port	ext RC
JRC1	45	AI		Game-Port	CMOS comparator in.
JRC0	46	AI		Game-Port	
LINOPL	47	AO		Line Output Left Channel	5 Kohm, 50 pF load
LNOPR	48	AO		Line Output Right Channel	5 Kohm, 50 pF load
LINL	49	AI	PA	Line Left Channel Input	Impedance 20K min
LINR	50	AI	PA	Line Right Channel Input	Impedance 20K min
CDL	51	AI	PA	CD Left Channel Input	Impedance 20K min
CDR	52	AI	PA	CD Right Channel Input	Impedance 20K min
MIDIL	53	AI	PA	MIDI Left Channel Input	Impedance 30K min
MIDIR	54	AI	PA	MIDI Right Channel Input	Impedance 30K min
VOCL	55	AI	PA	VOC Left Channel Input	Impedance 20K min
VOCR	56	AI	PA	VOC Right Channel Input	Impedance 20K min
RECOPL	57	AO		Rec Mixer Left Output	
RECOLR	58	AO		Rec Mixer Right Output	
AVS1	59	PWR		Analog Ground	
AVD1	60	PWR		Analog Power	
Mono	61	AI	PA	Mono Audio Input	Impedance 30K min
MIC	62	AI	PA	Microphone Iinput	Mic input to mixer
DACR	63	AO		CODEC Right Output	
DACL	64	AO		CODEC Left Output	
MIDIDACL	65	AO		MIDI DAC Left Output	
MICCAP	66	AI		MIC cap	
VCOM	67	AI		Analog Common	
MIDIDACR	68	AO		MIDI DAC Left Output	
AVD2	69	PWR		Analog Power	
VREFN	70	AI		Analog Reference	
VREFP	71	AI		Analog Reference	
AVS3	72	AI		Analog GROUND	
VREFN2	73	AI		Extra Reference	

Table 2-6 CT2510 Signal Descriptions

Name	No.	IO	Type	Function	Description
VREFP2	74	AI		Extra Reference	
AUXR	75	AI	PA	AUX Right Channel Input	Impedance 30K min
AUXL	76	AI	PA	AUX Left Channel Input	Impedance 30K min
SROM_DIN	77	DO		FFPROM DIN	CMOS Output 4mA
IRQ5	78	DO		Interrupt Request	TTL tri-state 12mA
IRQ7	79	DO		Interrupt Request	TTL tri-state 12mA
IRQ10	80	DO		Interrupt Request	TTL tri-state 12mA
SROMSEL	81	DI	PH,S	Internal ROM Select	TTL, Schmitt input
DACK0	82	DI	S	DMA Acknowledge	TTL, Schmitt input
DACK3	83	DI	S	DMA Acknowledge	TTL, Schmitt input
DACK1	84	DI	S	DMA Acknowledge	TTL, Schmitt input
TESTN1	85	DI	S	Test Mode Enable, active LOW	TTL, Schmitt input
DRQ0	86	DO		DMA Request	TTL tri-state 12mA
DRQ3	87	DO		DMA Request	TTL tri-state 12mA
DRQ1	88	DO		DMA Request	TTL tri-state 12mA
VSS4	89	PWR		Digital Ground	
IRQ9	90	DO		Interrupt Request 2 or 9	TTL tri-state 12mA
CLK14IN	91	OSC		14.318 MHz Clock Input	TTL, Schmitt input
VDD3	92	PWR		Digital Power	
VDD4	93	PWR		Digital Power	
VSS5	94	PWR		Digital Power	
VOLDECB	95	DI	S	Volume Increment	TTL, Schmitt input
VOLINCB	96	DI	S	Volume Decrement	TTL, Schmitt input
SROM_CS	97	DO		EEPROM Chip Select	CMOS Output 4mA
A<0>	98	DI	S	System Address Input	TTL, Schmitt input
A<1>	99	DI	S	System Address Input	TTL, Schmitt input
A<2>	100	DI	S	System Address Input	TTL, Schmitt input

2.4.4 Pin List

Table 2-7 CT2510 Pin List

No.	Name	Function	Description
4	IRQ5, IRQ7, IRQ9, IRQ10	IRQ	IRQ
3	DRQ0, DRQ1, DRQ3,	DMA	DRQ
3	DACK0, DACK1, DACK3		DACK
4	SROM_CS, SROM_CLK, SROM_DOUT, SROM_DIN	SERIAL	Serial EEPROM
5	LABENB, TESTN, SROMSEL, PDBOUT, BYPLL	MISC	
24	D[7:0, A[15:0]	ISA	Data bus
4	IORB, IOWB, AEN, RESET		Control
2	MIDIOUT, MIDIIN	MIDI	
8	JRC[3:0], JOYF[3:0]	GAMEPORT	
2	VOLINCB, VOLDECB	VOLUME	
11	MIDIL, MIDIR, LINL, LINR, VOCL, VOCR, AUXL, AUXR, CDL, CDR, MONO	ANALOG	Analog input
4	RECOPR, RECOPL, DACR, DACL		Codec related
2	MIC, MICCAP		MIC
2	LINOPL, LINOPR		Output
2	MIDIDACL, MIDIDACR		CQM output
5	VREFN, VREFP, VCOM, VREFN2, VREFP2	ANALOG REF	
1	CLK14IN	CLOCK	14.31818 MHz
4	VDD	POWER	Digital VDD
5	VSS		Digital VSS
2	AVDD		Analog VDD
3	AVSS		Analog VSS
100		TOTAL	

2.5. SMC 37C93xAPM

The SMC 37C93xAPM is an advanced high-performance multi-mode parallel port super I/O floppy disk controller.

2.5.1 Features

- Compatible with ISA Plug-and-Play standard (version 1.0a)
- 8042 keyboard controller
    - 2-K Proqram ROM
    - 256-byte Data RAM
    - Asynchronous access to two data registers and one status register
    - Supports interrupt and pollinq access
    - 8-bit timer counter
- Real time clock
    - MC146818 and DS1287 compatible
    - 256 bytes of battery-backed CMOS in two banks of 128 bytes
    - 128 bytes of CMOS RAM lockable in 4 x 32 byte blocks
    - 12 and 24-hour time format
    - Binary and BCD format
    - <1μa standby current (typ)
- Intelligent auto-power management

- 2.88-MB super I/O floppy disk controller
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - Three DMA options
    - Licensed CMOS 765B floppy disk controller
    - Advanced digital data separator
    - Software and register compatible with SMC's proprietary 82077AA compatible core
    - Sophisticated Power Control Circuitry (PCC) including multiple power-down modes for reduced power consumption
    - Game port select logic
    - Directly supports two floppy drives
    - 24-mA AT bus drivers
    - Low-power CMOS design

- Licensed CMOS 765B floppy disk controller core
    - Supports vertical recording format
    - 16-byte data FIFO
    - 100% IBM compatibility
    - Detects all overrun and underrun conditions
    - 48-mA drivers and Schmitt Trigger inputs
    - DMA enable logic
    - Data rate and drive control registers

- Enhanced digital data separator
    - Low-cost implementation
    - No filter components required
    - 2-Mbps, 1-Mbps, 500-Kbps, 300-Kbps, 250-Kbps data rates
    - Programmable pre-compensation modes

- Serial ports
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - 2 high-speed NS16C550 Compatible UARTs with send/receive 16-byte FIFOs
    - Programmable baud rate generator
    - Modem control circuitry including 230-K and 460-K baud
    - IrDA, HP-SIR, ASK-IR support

- IDE interface
    - Relocatable to 480 different addresses
    - 13 IRQ options
    - 6 DMA options
    - 2-channel/4-drive support
    - On-chip decode and select logic compatible with IBM PC/XT and PC/AT embedded hard disk drives
- Multi-mode parallel port with ChiProtect
    - Relocatable to 480 different addresses

2.5.2 Block Diagram

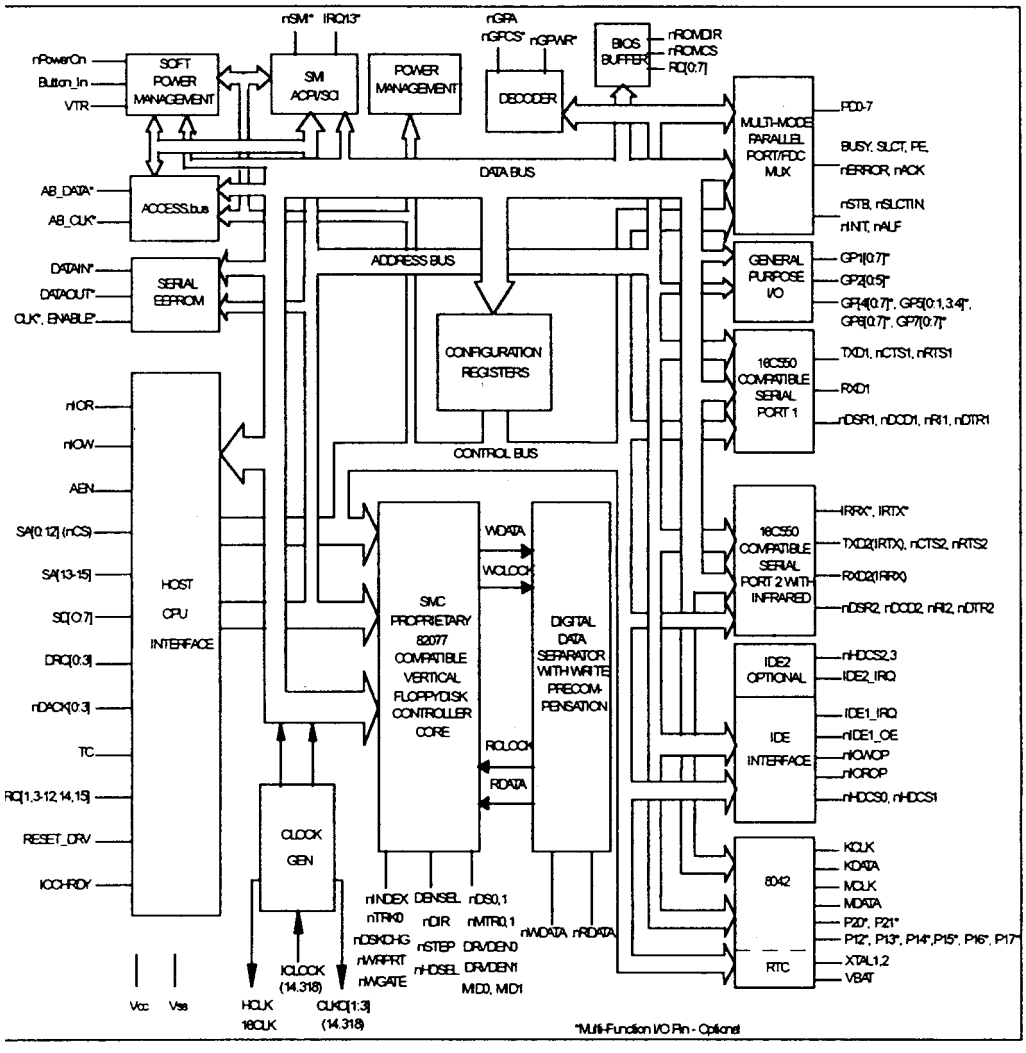


Figure 2-6 SMC 37C93xAPM Block Diagram

2.5.3 Pin Diagram

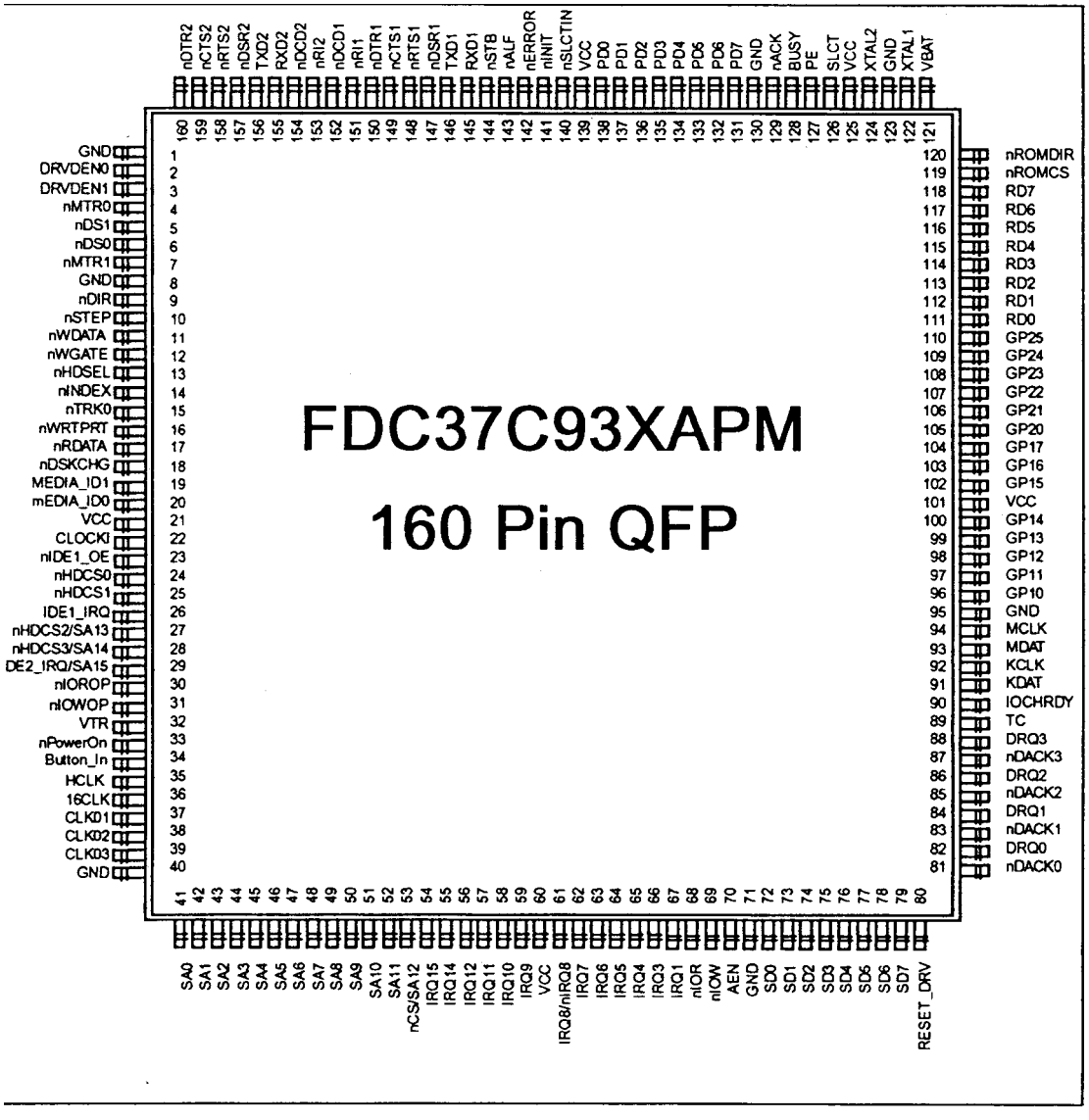


Figure 2-7 SMC 37C93xAPM Pin Diagram

2.5.4 Signal Descriptions

Table 2-8 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
Host Processor Interface			
SD0 - SD7	72:79	I/O24	System Data Bus
SA0 - SA11	41:52	I	System Address Bus
CS#	53	I	Chip Select / SA12
AEN	70	I	Address Enable
IOCHRDY	90	OD24	I/O Channel Ready
RESET_DRV	80	IS	Reset Drive
IRQ[1, 3:12, 14, 15]	67:61, 59:54	OD24	Interrupt Requests
DRQ[0:3]	82,84,86,88	O24	DMA Request
DACK[0:3]#	81, 83, 85, 87	I	DMA Acknowledge
TC	89	I	Terminal Count
IOR#	68	I	I/O Read
IOW#	69	I	I/O Write
16CLK	36	O8SR	16MHz Out
CLOCKI	22	ICLK	14.318MHz Clock Input
CLOCK1	37	O8SR	14.318MHz Clock Output 1
CLOCK2	38	O8SR	14.318MHz Clock Output 2
CLOCK3	39	O8SR	14.318MHz Clock Output 3
Floppy Drive Interface			
RDATA#	17	IS	Read Disk Data
WGATE#	12	OD48	Write Gate
WDATA#	11	OD48	Write Data
HDSEL#	13	OD48	Head Select (1 = side 0)
DIR#	9	OD48	Direction Control (1 = out)
STEP#	10	OD48	Step Pulse
DSKCHG#	18	IS	Disk Change
DS[0:1]#	5,6	OD48	Drive Select 0, 1
MTR[0:1]#	7,4	OD48	Motor on Lines
WPROT#	16	IS	Write Protected
TR0#	15	IS	Track 00
INDEX#	14	IS	Index Pulse Input
DRVDEN[1:0]	3,2	OD48	Drive Density Select [1:0]
MID[1:0]	19,20	IS	Media ID Inputs
Serial Port Interface			
RXD1, RXD2	145, 155	I	Receive Data
TXD1, TXD2	146, 156	O4	Transmit Data
RTS1#, RTS2#	148, 158	O4	Request to Send
Serial Port Interface			

Table 2-8 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
CTS1#, CTS2#	149, 159	I	Clear to Send
DTR1#, DTR2#	150, 160	O4	Data Terminal Ready
DSR1#, DSR2#	147, 157	I	Data Set Ready
DCD1#, DCD2#	152, 154	I	Data Carrier Select
RI1#, RI2#	151, 153	I	Ring Indicator
Parallel Port Interface			
PD0-PD7	138:131	I/OP24	Port Data
SLCTIN#	140	OD24/OP24	Printer Select
INIT#	141	OD24/OP24	Initiate Output
ALF#	143	OD24/OP24	Auto Line Feed
STB#	144	OD24/OP24	Strobe Signal
BUSY	128	I	Busy Signal
ACK#	129	I	Acknowledge Handshake
PE	127	I	Paper End
SLCT	126	I	Printer Selected
ERROR#	142	I	Error at Printer
IDE			
IDE1_OE#	23	O4	IDE1 Enable
HDCS0#	24	O24	IDE1 Chip Select0
HDCS1#	25	O24	IDE1 Chip Select1
IOROP#	30	O24	IOR Output
IOWOP#	31	O24	IOW Output
A[2:0]	32:34	O24	Address [2:0] Output
IDE1_IRQ	26	I	IDE Interrupt Request
HDCS2	27	O24	IDE2 Chip Select 2 / SA13
HDCS3	28	O24	IDE2 Chip Select 3 / SA14
IDE2_IRQ	29	I	IDE2 Interrupt Request / SA15
Real Time Clock			
XTAL1	122	ICLK	32-KHz Crystal Input
XTAL2	124	OCLK	32-KHz Crystal Output
Vbat	121		Battery Voltage
Keyboard / Mouse			
KDAT	91	I/OD16P	Keyboard Data
KCLK	92	I/OD16P	Keyboard Clock
MDAT	93	I/OD16P	Mouse Data
Keyboard / Mouse			
MCLK	94	I/OD16P	Mouse Clock

Table 2-8 SMC 37C93xAPM Signal Descriptions

Signal	Pin	Type	Description
Soft Power Management Interface			
PowerOn#	33	I/O24	Power On
Button_In	34	I/O24	Button Input
General Purpose I/O			
GP10	96	I/O4	IRQ In
GP11	97	I/O4	IRQ In
GP12	98	I/O4	WD Timer Output / IRRX
GP13	99	I/O24	Power LED Output / IRTX
GP14	100	I/O4	GPI/O, General Purpose Read Strobe
GP15	102	I/O4	GPI/O, General Purpose Write Strobe
GP16	103	I/O4	GPI/O, Joystick Read Strobe / JOYCS
GP17	104	I/O4	GPI/O, Joystick Write Strobe
GP20	105	I/O4	GPI/O, IDE2 Output Enable
GP21	106	I/O4	GPI/O, Serial EEPROM Data In
GP22	107	I/O4	GPI/O, Serial EEPROM Data Out
GP23	108	I/O4	GPI/O, Serial EEPROM Clock
GP24	109	I/O4	GPI/O, Serial EEPROM Enable
GP25	110	I/O4	GPI/O, 8042 P21
BIOS Buffers			
RD[0:7]	111:118	I/O4	ROM Bus (I/O to the SD bus)
DOMCS#	119	I	ROM Chip Select (only used for ROM)
ROMOE#	120	I	ROM Output Enable (DIR) (only used for ROM)
Power			
VCC	21, 60, 101, 125, 139		+ 5V Supply Voltage
VTR	32		Trickle Voltage Input
GND↔	1, 8, 40, 71, 95, 123, 130		Ground

2.5.5 Multifunction Pins with GPI/O and Other Alternate Functions

Table 2-9 Multifunction Pins with GPI/O and Other Alternate Functions

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
19	MEDIA_ID1	GPI/O			I/O8	Float	GP4	GP40
20	MEDIA_ID0	GPI/O			I/O8	Float	GP4	GP41
23	IDE1_OE#	GPI/O			I/O4	High	GP4	GP42
24	HDCS0#	GPI/O			I/O24	High	GP4	GP43
25	HDCS1#	GPI/O			I/O24	High	GP4	GP44
26	IDE1_IRQ	GPI/O			I/O8	Float	GP4	GP45
30	IOROP#	GPI/O	Power LED Output	WDT	I/O24	Float	GP4	GP46
31	IOWOP#	GPI/O	SMI#		I/O24	Float	GP4	GP47
33	PowerOn#	GPI/O			I/O24	Active low open collector output	GP5	GP51
34	Button_In	GPI/O			I/O24	Input	GP5	GP50
111	RD0	GPI/O	Power LED Output		I/O4	RD0 (1) (4)	GP6	GP60
112	RD1	GPI/O	WDT		I/O4	RD1 (1) (4)	GP6	GP61
113	RD2	GPI/O	8042-P12		I/O4	RD2 (1) (4)	GP6	GP62
114	RD3	GPI/O	8042-P13		I/O4	RD3 (1) (4)	GP6	GP63
115	RD4	GPI/O	8042-P14		I/O4	RD4 (1) (4)	GP6	GP64
116	RD5	GPI/O	8042-P15		I/O4	RD5 (1) (4)	GP6	GP65
117	RD6	GPI/O	8042-P16		I/O4	RD6 (1) (4)	GP6	GP66
118	RD7	GPI/O	8042-P17		I/O4	RD7 (1) (4)	GP6	GP67
119	ROMCS#	GPI/O			I/O8	ROMCS# (1)	GP5	GP53
120	ROMOE#	GPI/O			I/O8	ROMOE#(1)	GP5	GP54
153	R12#	GPI/O			I/O8	Input (2)	GP7	GP70
154	DCD2#	GPI/O			I/O8	Input (2)	GP7	GP71
155	RXD2	GPI/O			I/O8	Input (2)	GP7	GP72
156	TXD2	GPI/O			I/O8	Input (2) (4)	GP7	GP73
157	DSR2#	GPI/O			I/O8	Input (2)	GP7	GP74
158	RTS2#	GPI/O			I/O8	Input (2) (4)	GP7	GP75
159	CTS2#	GPI/O			I/O8	Input (2)	GP7	GP76
160	DTR2#	GPI/O			I/O8	Input (2) (4)	GP7	GP77

Table 2-9 Multifunction Pins with GPI/O and Other Alternate Functions

Pin No.	Original Function	Alternate Function 1	Alternate Function 2	Alternate Function 3	Buffer Type	Default	Index Register	GPI/O
27	HDCS2#	SA13			I/O24	Float		
28	HDCS3#	SA14			I/O24	Float		
29	IDE2_IRQ	SA15			I	Float		
53	CS/SA 12#				I	Input		
96	GPI/O	IRQ in			I/O4	Input	GP1	GP10
97	GPI/O	IRQ in	IRQ13		I/O4	Input	GP1	GP11
98	GPI/O	WDT Timer Output/IRRX			I/O4	Input	GP1	GP12
99	GPI/O	Power LED Output/IRTX			I/O24	Input	GP1	GP13
100	GPI/O	GP Address Decode			I/O4	Input	GP1	GP14
102	GPI/O	GP Write Strobe			I/O4	Input	GP1	GP15
103	GPI/O	Joy Read Strobe	JOYCS		I/O4	Input	GP1	GP16
104	GPI/O	Joy Write Strobe			I/O4	Input	GP1	GP17
105	GPI/O	IDE2 Output Enable	8042 P20		I/O4	Input	GP2	GP20
106	GPI/O	Serial EEPROM Data In	AB_DATA		I/O8/ OD8 (EN1)	Input	GP2	GP21
107	GPI/O	Serial EEPROM Data Out	AB_CLK		I/O8/ OD8 (EN1)	Input	GP2	GP22
108	GPI/O	Serial EEPROM Clock			I/O4	Input	GP2	GP23
109	GPI/O	Serial EEPROM Enable			I/O4	Input	GP2	GP24
110	GPI/O	8042 P21			I/O4	Input	GP2	GP25

Notes (1): At power-up, RD0-RD7, ROMCS# and ROMOE# function as the XD Bus. To use RD0-RD7 for functions other than the XD Bus, ROMCS# must stay high until the reprogramming of RD0-RD7 is done.

(2): These pins are input (high-z) until they are programmed for second serial port.

(3): This is the trickle voltage input pin for the FDC37C93XAPM.

(4): These pins cannot be programmed as open drain pins in their original function.

(5): No pins in their original function can be programmed as inverted input or inverted output.

2.5.6 Buffer Type Descriptions

Table 2-10 SMC 37C935 Buffer Type Descriptions

Buffer Type	Description
I	Input TTL compatible
IS	Input with Schmitt Trigger
I/OD16P	Input/output, 19-mA sink, 90-uA pull-up
I/O24	Input/output pin. 24-mA sink; 12-mA source
O4	Output, 4-mA sink; 2.0-mA source
O8SR	Output, 8-mA sink; 4.0-mA source with Slew Rate Limiting
O24	Output, 24-mA sink; 12-mA source
OD24	Output, open drain; 24-mA sink
OD48	Output, open drain; 48-mA sink
OD24P	Output, open drain; 24-mA sink, 4-mA source pull up
OP24	Output; 24-mA sink, 12-mA source
OCLK	Clock output
ICLK	Clock input

2.6. Intel 82557

The 82557 is Intel's first highly-integrated 32-bit PCI LAN controller for 10 Mbps or 100 Mbps Fast Ethernet network. It offers a high-performance LAN solution while maintaining low-cost through its high-integration. It contains a 32-bit PCI bus master interface to fully utilize the high bandwidth available (up to 132 Mbs) to masters on the PCI bus. The bus master interface can eliminate the intermediate copy step in Receive (RCV) and Transmit (XMT) frame copies, resulting in faster processing of these frames. Though the 82557 maintains a similar memory structure to the Intel 82596 LAN coprocessor, its' memory structures have been streamlined for better network operating system (NOS) interaction and improved performance.

The 82557 contains two large receive and transmit FlFOs that prevent data overruns or underruns while waiting for access to the PCI bus, as well as enabling back-to-back frame transmission within the minimum 960 ns interframe spacing. Full support for up to 1 MB of Flash enables network management support via Intel FlashWorks utilities, as well as remote boot capability (a BIOS extension stored in the Flash allows a node to boot itself off of a network drive). For 100 Mbps applications, the 82557 contains an IEEE Mll compliant interface to the Intel 82553 serial interface device (or other Mll compliant PHYs) that allows connection to 100 Mbps/10 Mbps network. For 10 Mbps network, the 82557 can be interfaced to a standard ENDEC device (such as the Intel 82503 Serial Interface) while maintaining software compatibility with 100 Mbps solutions.

The 82557 is designed to implement cost-effective, high-performance PCI add-in adapters, PC motherboards, or other interconnect devices such as a hubs or bridges. These make the chip ideal for network.

The 82557 has two interfaces: the host system PCI bus interface and the serial or network interface. The network interface complies to the IEEE standard for 10Base-T, TX, and T4 Ethernet interfaces. The 82557 also complies to the PCI Bus Specification Revision 2.1.

2.6.1 Features

- Glueless 32-bit PCI bus master interface (Direct Drive of Bus), compatible with PCI Bus Specification Revision 2.1
- 82596-like chained memory structure
- Improved dynamic transmit chaining for enhanced performance
- Programmable transmit threshold for improved bus utilization
- Early receive interrupt for concurrent processing of receive data
- Flash support up to 1 MB
- Large on-chip receive and transmit FlFOs
- On-chip counters for network management

- Back-to-back transmission at 100 Mbps, EEPROM support
- Support for both 10 Mbps and 100 Mbps networks
- Interface to MII-compliant PHY devices, including Intel 82553 Physical interface component for 10 Mbps/100 Mbps designs
- IEEE 802.3 100Base-T, TX, and T4 compatible
- Interface to Intel 82503 or other serial device for 10 Mbps designs: IEEE 802.3 10Base-T compatible
- Auto-detect and auto-switching for 10 Mbps or 100 Mbps network speeds
- Full- or half-duplex capabilities at 10 Mbps and 100 Mbps
- 160-lead QFP package

2.6.2 Block Diagram

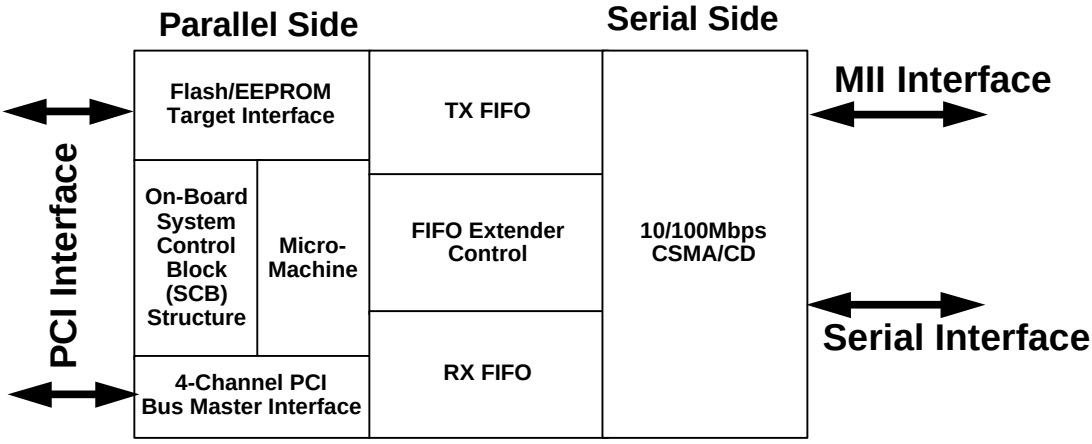


Figure 2-8 82557 Block Diagram

2.6.3 Pin Diagram

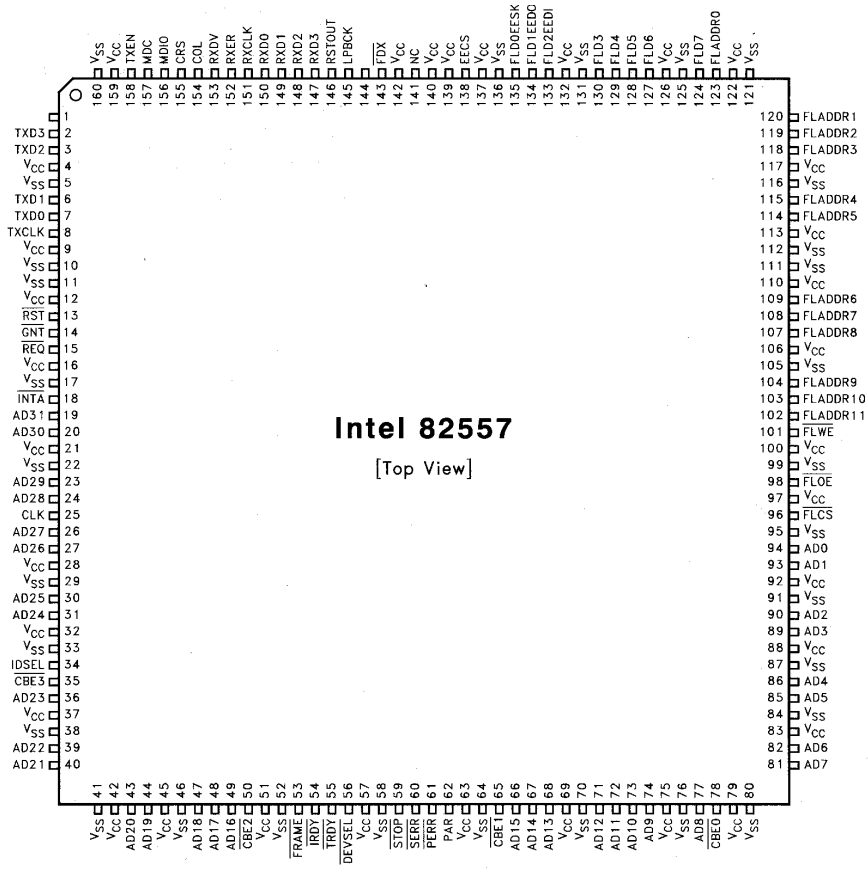


Figure 2-9 82557 Pin Diagram

2.6.4 Signal Descriptions

Table 2-11 82557 Signal Descriptions

Signal	Pin	Type	Description
Address and Data Signals			
ADO AD1 AD2 AD3 AD4 AD5 AD6 AD7 AD8 AD9 AD10 AD11 AD12 |AD13 AD14 AD15 AD16 AD17 AD18 AD19 AD20 AD21 AD22 AD23 AD24 AD25 AD26 AD27 AD28 AD29 AD30 AD31	94 93 90 89 86 85 82 81 77 7473 72 7168 67 66 49 48 47 44 43 40 39 36 31 30 27 26 24 23 20 19	TS	Address and Data are multiplexed on the same PCI pins by the 82557. A bus transaction consists of an address phase followed by one or more data phases. The address phase is the clock cycle in which FRAME# is asserted. During the address phase, AD0-31 contain a physical address (32 bits). For I/O, this is a byte address; for configuration and memory it is a DWORD address. The 82557 used “Little Endian” byte ordering. During data phases AD0-7 contain the least significant byte (LSB) and AD24-31 contain the most significant byte (MSB).
CBE0# CBE1# CBE2# CBE3#	78 65 50 35	TS	Bus Command and Byte Enables are multiplexed on the same PCI pins by the 82557. During the address phase of a transaction, C/BE0-3# define the bus command. During the data phase C/BE0-3# are used as Byte Enables. The Byte Enables are valid for the entire data phase and capable of determining which byte lanes carry meaningful data. The C/BE0# applies to byte 0 (LSB) and C/BE3# applies to byte 3 (MSB).
PAR	62	TS	Parity is the even parity across AD0-31 and C/BE0-3#. PAR is stable and valid one clock after the address phase. For data phases, PAR is stable and valid one clock after either IRDY# is asserted on a write transaction or TRDY# is asserted on a read transaction. Once PAR is valid, it remains valid until one clock after the completion of the current data phase. When the 82557 is a bus master, it drives PAR for address and write data phases. As a slave, it drives PAR for read data phases.
Interface Control Signals			

Table 2-11 82557 Signal Descriptions

Signal	Pin	Type	Description
FRAME#	53	STS	FRAME# is driven by the 82557 to indicate the beginning and duration of an access. FRAME# is asserted to indicate that a bus transaction is beginning. While FRAME# is asserted, data transfers continue. When FRAME# is deasserted, the transaction is in the final data phase.
IRDY#	54	STS	Initiator Ready# indicates the ability of the 82557 (as a bus mastering device) to complete the current data phase of the transaction. IRDY# is used in conjunction with TRDY#. A data phase is completed on any clock in which both IRDY# and TRDY# are sampled asserted. During a write, IRDY# indicates that valid data is present on AD0-31. During a read, it indicates that the master is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82557 drives IRDY# when acting as a master and samples it when acting as a slave.
TRDY#	55	STS	Target Ready# indicates the ability of the 82557 (as a selected device) to complete the current data phase of the transaction. TRDY# is used in conjunction with IRDY#. A data phase is completed on any clock in which both TRDY# and IRDY# are sampled asserted. During a read, TRDY# indicates that valid data is present on AD0-31. During a write, it indicates that the target is prepared to accept data. Wait cycles are inserted until both IRDY# and TRDY# are asserted together. The 82557 drives TRDY# when acting as a slave and samples it when acting as a master.
STOP#	59	STS	STOP# indicates the current target is requesting the master to stop the current transaction. As a slave, the 82557 drives STOP# to inform the bus master to stop the current transaction. As a bus master, the 82557 receives STOP# from the slave and stops the current transaction.
IDSEL	34	IN	Initialization Device Select is used by the 82557 as a chip select during configuration read and write transactions.
DEVSEL#	56	STS	Device Select#, when actively driven by the 82557 as a slave, indicates to the bus master that it has decoded its address as the target of the current access. As an input, DEVSEL# indicates whether any device on the bus has been selected.
Error Reporting Signals			
SERR#	60	OD	System Error# is used by the 82557 to report address parity errors. SERR# is open drain and is actively driven for a single PCI clock when reporting the error.
PERR	61	STS	Parity Error# is used by the 82557 for reporting data parity errors during all PCI transactions except a Special Cycle. The PERR# pin is sustained tri-state and must be driven active by the 82557 receiving data two clocks following the data when a data parity error is detected. The minimum duration of PERR# is one clock for each data phase that a data parity error is detected.

Table 2-11 82557 Signal Descriptions

Signal	Pin	Type	Description
Interrupt Signal			
INTA#	18	OD	Interrupt A# is used to request an interrupt by the 82557. This is an active low, level-triggered interrupt signal.
Arbitration Signals			
REQ#	15	TS	Request# indicates to the arbiter that the 82557 desires use of the bus. This is a point-to-point signal. Every master has its own REQ.
GNT#	14	IN	Grant indicates to the 82557 that access to the bus has been granted. This is a point-to-point signal.
System Signals			
CLK	25	IN	Clock provides timing for all transactions on the PCI bus and is an input to the 82557. All other PCI signals, except RST and the INT lines are sampled on the rising edge of CLK and all other timing parameters are defined with respect to this edge.
RST#	13	IN	Reset# is used to bring PCI-specific registers, sequencers and signals to a consistent state. Anytime RST# is asserted, all PCI output signals must be driven to their benign state. In general, this means they must be tri-stated and SERR# (open drain) is floated. To prevent AD, C/BE# and PAR signals from floating during reset, the central device may drive these lines during reset (bus parking). But to a logic low-level, these signals may not be driven high.
Local Memory Interface			
EECS	138	OUT	The EEPROM Chip Select is an active high signal used to assert Chip Select to the Serial EEPROM.
FLD0EESK	135	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 0 input/output. During EEPROM access, it acts as EEPROM SHIFT CLOCK output to shift data into and out of the serial EEPROM.
FLD1EEDO	134	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 1 input/output. During EEPROM access, it acts as the input EEPROM DATA OUT.
FLD2EEDI	133	TS	Multiplexed pin. During flash access, this signal acts as Flash Data 2 input/output. During EEPROM access, it acts as the output EEPROM DATA IN.
FLD3 FLD4 FLD5 FLD6 FLD7	130 129 128 127 124	TS	Flash Data 7 to 3 input/outputs

Table 2-11 82557 Signal Descriptions

Signal	Pin	Type	Description
Interrupt Signal			
FLADDR0 FLADDR1 FLADDR2 FLADDR3 FLADDR4 FLADDR5 FLADDR6 FLADDR7 FLADDR8 FLADDR9 FLADDR10 FLADDR11	123 120 119 118 115 114 109 108 107 1041 0310 2	OUT	Flash Address 11 to 0. These signals work in conjunction with an external 8-bit Address Latch to control the Flash addressing up to 1 MB. The 8 most significant Flash address pins (FLADDR11 to 4) should be connected to both the Address Latch and to Address Pins 11 to 4 of the Flash. The Address Latch provides the upper 8 bits, 19 to 12, of address to the Flash and is loaded by assertion of the FLCS# pin.
FLCS#	96	OUT	Flash CS is normally high to disable access to the Flash. Whenever a Flash high address is to be latched, FLCS# goes low; thus, latching the data in the latch and enabling the Flash. FLCS# should be connected to both the ENABLE pin on the external address latch and the CE# pin on the Flash.
FLOE#	98	OUT	This output provides the active low Output Enable control to the Flash.
FLWE#	101	OUT	This output provides the active low Write Enable control to the Flash.
MII/Serial Interface Signals			
RXCLK	151	IN	Receive Clock input operates at either 25 MHz, 2.5 MHz (Mll Mode), or 10 MHz (10 Mbps-only mode).
RXD0 RXD1 RXD2 RXD3	150 149 148 147	IN	Receive Data signals are the nibble wide receive data inputs in MII mode. In 10 Mbps-only mode, RXD0 is the serial receive data input.
RXDV	153	IN	Receive Data Valid indicates that valid data is present on the RXD lines. This is used for Mll mode only. When this signal is inactive (low), receive data is not sampled by the 82557.
RXER	152	IN	Receive Data Error indicates that an invalid symbol has been detected inside a receive packet (Mll mode only).
Reserved	1	-	No connection
CRS	155	IN	Carrier Sense signal indicates traffic on the wire.
TXCLK	8	IN	Transmit Clock input that operates at either 25 MHz, 2.5 MHz (Mll Mode), or 10 MHz (10 Mbps-only mode).
TXD0 TXD1 TXD2 TXD3	7 6 3 2	OUT	Transmit Data signals are the nibble wide transmit data outputs in MII mode. However, in 10 Mbps mode, only the TXD0 is the serial transmit data output signal.
RTS/TXEN	158	OUT	Request To Send signal indicates that the 82557 has a frame pending for transmission (10 Mbps-only mode). Transmit Enable signal indicates that the 82557 is transferring data to the PHY (Mll mode).
MII/Serial Interface Signals			

Table 2-11 82557 Signal Descriptions

Signal	Pin	Type	Description
COL	154	IN	Collision Detect signal indicates that a collision has been detected on the wire. In Full Duplex mode, assertion of COL indicates a Congestion condition has occurred.
Reserved	144	IN	Ties high with a 3.3-Kohm pull-up resistor
RSTOUT	146	OUT	This is the Reset Out signal to the PHY. This signal is driven high during H/W reset of the 82557.
LPBCK	145	OUT	Loopback controls the PHY into loopback mode
FDX#	143	IN	Full Duplex is an input from the physical layer component that indicates if it has switched into or out of full duplex mode. FDX# is active low.
FULHAL	6	OUT	When active, this signal indicates that 82557 is in Full Duplex mode. This is multiplexed with the TXD1 pin and operates only when in 10 Mbps mode.
MII/Serial Interface Signals			
MDIO	156	TS	Management Data Input / Output is the bidirectional signal between the 82557 and an Mll-compatible PHY. It is used to transfer control information and status between the 82557 and the PHY. Control information is driven by the 82557 on the MDIO synchronously to MDC and sampled synchronously by PHY. The status information is driven synchronously by PHY and sampled synchronously by 82557.
MDC	157	OUT	Management Data Clock is the timing reference for transfer of control information and status on the MDIO signal. The frequency of this clock is up to 2.5 MHz.

Signal	Pin	Type	Description
Power and Ground			
V_{CC}	4, 9, 12, 16, 21, 28, 32, 37, 42, 45, 51, 63, 69, 75, 79, 83, 88, 92, 97, 100, 110, 113, 117, 122, 126, 132, 137, 159	IN	Power: +5v +-5%
V_{SS}	5, 10, 11, 17, 22, 29, 33, 38, 41, 46, 52, 58, 64, 70, 76, 80, 84, 87, 91, 95, 99, 105, 111, 112, 116, 121, 125, 131, 136	IN	Ground: 0V

BIOS Setup Information

Most systems are already configured by the manufacturer or the dealer. There is no need to run Setup when starting the computer unless you get a Run Setup message.

The Setup program loads configuration values into the battery-backed nonvolatile memory called CMOS RAM. This memory area is not part of the system RAM.

If you repeatedly receive Run Setup messages, the battery may be bad. In this case, the system cannot retain configuration values in CMOS. Ask a qualified technician for assistance.

Before running Setup, have the following information ready:

- **Floppy drive type** The standard type is either a 5.25-inch, 1.2-MB or a 3.5-inch, 1.44/2.88-MB floppy drive.

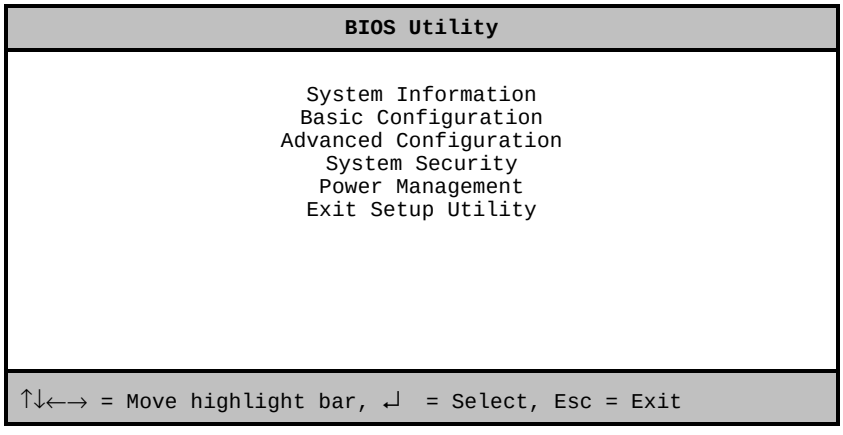
- **IDE hard disk drive type** The drive information is on the label pasted on your IDE drive or in the documentation supplied by the vendor.

3.1. Entering Setup

To enter Setup, press the key combination CTRL+ALT+ESC.

You must press CTRL+ALT+ESC while the system is booting. This key combination does not work during any other time.

The BIOS Utility Main menu then appears:

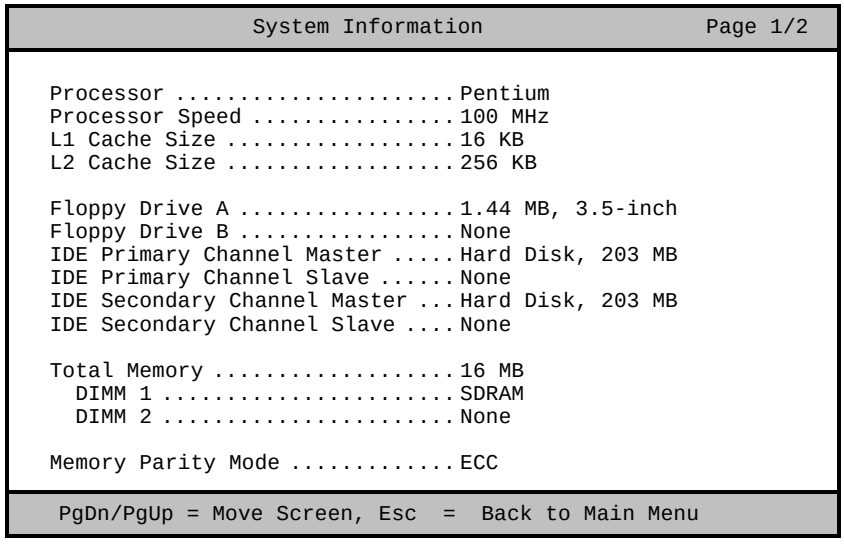


The parameters on the screens show default values. These values may not be the same as those in your system.

The grayed items on the screens have fixed settings and are not user-configurable.

3.2. System Information

The following screen appears if you select the System Information from the Main menu.



The System Information menu shows the current basic configuration of your system.

The command line at the bottom of the menu tells you how to move from one screen to another and return to the Main menu.

Press PGDN to move to the next page or PGUP to return to the previous page.

Press ESC to return to the Main menu.

The following screen shows page 2 of the System Information menu.

```
                System Information                  Page 2/2

   Serial Port 1 ..................... 3F8h, IRQ 4
   Serial Port 2 ..................... Disabled
   Parallel Port  .................... 378h, IRQ 7
   PS/2 Mouse ........................ Installed

   System BIOS Version ............... V.x.x
   System BIOS ID .................... xx-xx  xx  xx


                               INTA   INTB   INTC   INTD
   PCI Slot 1 ................. [--]   [--]   [--]   [--]
   PCI Slot 2 ................. [--]   [--]   [--]   [--]
   PCI Slot 3 ................. [--]   [--]   [--]   [--]
   PCI Slot 4 ................. [--]   [--]   [--]   [--]




   PgDn/PgUp = Move Screen, Esc  =  Back to Main Menu
```

The following sections explain the parameters.

3.2.1 Processor

The Processor parameter specifies the type of processor currently installed in your system. The system can support Intel Pentium P54C/P55C, Cyrix M1/M2 and AMD K5/K6 processors.

3.2.2 Processor Speed

The Processor Speed parameter specifies the speed of the CPU currently installed in your system. The system can support CPUs running at 120, 133, 150, 166, and 200 MHz.

3.2.3 L1 Cache Size

This parameter specifies the first-level or the internal memory (i.e., the memory integrated into the CPU) size.

3.2.4 L2 Cache Size

This parameter specifies the external cache memory size currently supported by the system.

3.2.5 Floppy Drive A

This parameter specifies the system's current floppy drive A settings. For information on how to configure the floppy drives, see section 3.3.2.

3.2.6 Floppy Drive B

This parameter specifies the system's current floppy drive B settings. For information on how to configure the floppy drives, see section 3.3.2.

3.2.7 IDE Primary Channel Master

This parameter specifies the current configuration of the IDE device connected to the master port of the primary IDE channel. For information on how to configure the IDE devices drives, see section 3.3.3.

3.2.8 IDE Primary Channel Slave

This parameter specifies the current configuration of the IDE device connected to the slave port of the primary IDE channel. For information on how to configure the IDE devices drives, see section 3.3.3.

3.2.9 IDE Secondary Channel Master

This parameter specifies the current configuration of the IDE device connected to the master port of the secondary IDE channel. For information on how to configure the IDE devices drives, see section 3.3.3.

3.2.10 IDE Secondary Channel Slave

This parameter specifies the current configuration of the IDE device connected to the slave port of the secondary IDE channel. For information on how to configure the IDE devices drives, see section 3.3.3.

3.2.11 Total Memory

This parameter specifies the total amount of onboard memory. The memory size is automatically detected by BIOS during the POST. If you install additional memory, the system automatically adjusts this parameter to display the new memory size.

3.2.11.1 DIMM 1

This parameter indicates the type of DRAM installed in DIMM 1. The **None** setting indicates that there is no DRAM installed. For the location of DIMM 1, refer to Figure 1-7.

3.2.11.2 DIMM 2

This parameter indicates the type of DRAM installed in DIMM 2. The **None** setting indicates that there is no DRAM installed. For the location of DIMM 2, refer to Figure 1-7.

3.2.12 Memory Parity Mode

This parameter specifies if the ECC or the parity check features are enabled or disabled. The parity check feature enables BIOS to detect data errors. The ECC feature enables BIOS not only to detect, but as well as correct data errors.

3.2.13 Serial Port 1

This parameter shows the serial port 1 address and IRQ settings.

3.2.14 Serial Port 2

This parameter shows the serial port 2 address and IRQ settings.

3.2.15 Parallel Port

This parameter shows the parallel port address and IRQ settings.

3.2.16 PS/2 Mouse

The BIOS utility automatically detects if there is a mouse connected to your system. If there is, this parameter displays the **`Installed`** setting. Otherwise, this is set to **`None.`**

3.2.17 Onboard USB

This parameter specifies whether the onboard USB controller is enabled or not.

3.2.18 System BIOS Version

This parameter specifies the version of the BIOS utility.

3.2.19 System BIOS ID

This parameter specifies the identification number of the BIOS utility.

3.2.20 PCI Slot 1/2/3/4

These parameters specify the auto-assigned interrupt for each of the PCI devices.

3.3. Basic System Configuration

Select Basic System Configuration to input configuration values such as date, time, and disk types.

The following screen shows the Basic System Configuration menu.

```
                Basic System Configuration          Page 1/1

  Date ..................... [MM/DD/YY]
  Time ..................... [HH:MM:SS]

  Floppy Drive A ........... [xx-MB     xx-inch]
  Floppy Drive B ........... [xx-MB     xx-inch]

                                    Cylinder   Head    Sector

  IDE Primary Channel
     Master................. [Auto]    xx        xx      xx
     Slave
  IDE Secondary Channel
     Master................. [Auto]    xx        xx      xx
     Slave ................. [Auto]    xx        xx      xx

  Enhanced IDE Feature
  Boot Options

  ↑↓ = Move Highlight Bar,  → ← = Change Setting, F1 = Help
```

3.3.1 Date and Time

The real-time clock keeps the system date and time. After setting the date and time, you do not need to enter them every time you turn on the system. As long as the internal battery remains good (approximately seven years) and connected, the clock continues to keep the date and time accurately even when the power is off.

3.3.1.1 Date

Highlight the items on the Date parameter and press → or ← to set the date following the month-day-year format.

Valid values for month, day, and year are:

- Month **1** to **12**
- Day **1** to **31**
- Year **00** to **99**

3.3.1.2 Time

Highlight the items on the Time parameter and press → or ← to set the time following the hour-minute-second format.

Valid values for hour, minute, and second are:

- Hour **00** to **23**
- Minute **00** to **59**
- Second **00** to **59**

3.3.2 Floppy Drives

To enter the configuration value for the first floppy drive (drive A), highlight the Floppy Drive A parameter. Press → or ← key to view the options and select the appropriate value.

Possible settings for the Floppy Drive parameters:

- **[None]**
- **[360 KB, 5.25-inch]**
- **[1.2 MB, 5.25-inch]**
- **[720 KB, 3.5-inch]**
- **[1.44 MB, 3.5-inch]**

Follow the same procedure for Floppy Drive B. Choose **None** if you do not have a second floppy drive.

3.3.3 IDE Drives

Move the highlight bar to the Master parameter under IDE Primary Channel to configure the first IDE drive (drive C). Press → or ← to display the IDE drive types with their respective values. Select the type that corresponds to your IDE hard disk drive. If you do not know the exact type of your IDE hard disk drive, select the option **Auto.**

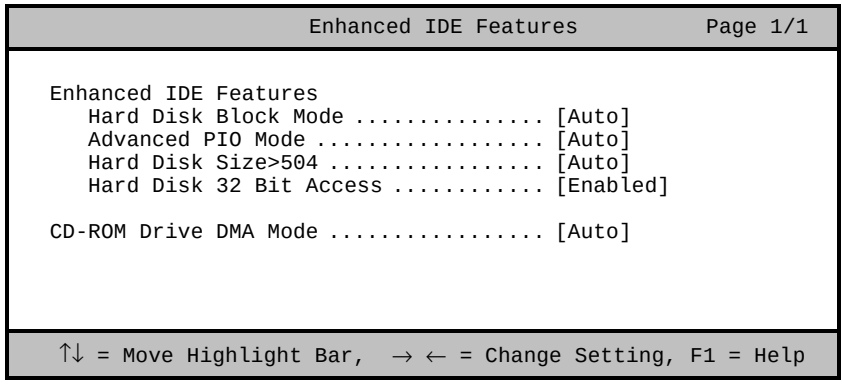
To configure the other IDE drive connected to the slave port of the primary channel, move the highlight bar to Slave and follow the same procedure.

To configure the other IDE drives installed, highlight the Master parameter under the IDE Secondary Channel if the drive is connected to the master connector of the IDE secondary channel, or Slave parameter if it is connected to the slave connector.

For IDE drives other than hard disk and CD-ROM, choose **None**.

3.3.4 Enhanced IDE Feature

The following screen appears if you select Enhanced IDE Feature from the Basic Configuration menu.



This option lets you enable or disable the enhanced IDE features.

3.3.4.1 Hard Disk Block Mode

This function enhances disk performance depending on the hard disk in use. If you set this parameter to **Auto**, the BIOS utility automatically detects if the installed hard disk drive supports the Block Mode function. If supported, it allows data transfer in block (multiple sectors) at a rate of 256 bytes per cycle. To disregard the feature, change the setting to **Disabled.**

3.3.4.2 Advanced PIO Mode

When set to **Auto**, the BIOS utility automatically detects if the installed hard disk supports the function. If supported, it allows for faster data recovery and read/write timing that reduces hard disk activity time. This results to better hard disk performance. To disregard the feature, change the setting to **Disabled.**

3.3.4.3 Hard Disk Size > 504 MB

When set to **Auto**, the BIOS utility automatically detects if the installed hard disk supports the function. If supported, it allows you to use a hard disk with a capacity of more than 504 MB. This is made possible through the Logical Block Address (LBA) mode translation. However, enhanced IDE feature works only under DOS and Windows 3.x, 95 environment. Other operating systems require this parameter to be set to **Disabled**.

3.3.4.4 Hard Disk 32-bit Access

Enabling this parameter improves system performance by allowing the use of the 32-bit hard disk access. This enhanced IDE feature works only under DOS, Windows 3.x, 95, and Novell NetWare. If your software or hard disk does not support this function, set this parameter to **Disabled** .

3.3.4.5 CD-ROM Drive DMA Mode

Set this parameter to **Auto** to enable the DMA mode for the CD-ROM drive. This improves the system performance since it allows direct memory access to the CD-ROM. To deactivate the function, set the parameter to **Disabled** .

3.3.5 Boot Options

This option allows you to specify your preferred setting for bootup.

The following screen appears if you select Boot Options from the Basic Configuration menu:

```
                Boot Options                          Page 1/1

   Fast Boot ..............................[Auto ]

   Silent Boot ............................[Enabled ]
   Num Lock After Boot ....................[Enabled ]
   Memory Test ............................[Disabled]

   System Boot Drive ......................[Drive A Then C]
   Boot From CD-ROM .......................[Disabled]




  ↑↓ = Move Highlight Bar,  → ← = Change Setting, F1 = Help
```

3.3.5.1 Fast Boot

This parameter allows the system to boot faster by skipping some POST routines. The default setting is **Auto**.

3.3.5.2 Silent Boot

This parameter enables or disables the Silent Boot function. When set to **Enabled**, BIOS is in graphical mode and displays only an identification logo during POST and while booting. After which the screen displays the operating system prompt (such as DOS) or logo (such as Windows 95). If any error occurred while booting, the system automatically switches to the text mode.

Even if your setting is **Enabled**, you may also switch to the text mode while booting by pressing F3 after you hear a beep that indicates the activation of the keyboard.

When set to **Disabled**, BIOS is in the conventional text mode where you see the system initialization details on the screen.

3.3.5.3 Num Lock After Boot

This parameter allows you to activate the Num Lock function upon booting. The default setting is **Enabled**.

3.3.5.4 Memory Test

When set to **Enabled**, this parameter allows the system to perform a RAM test during the POST routine. When set to **Disabled**, the system detects only the memory size and bypasses the test routine. The default setting is **Disabled.**

3.3.5.5 System Boot Drive

This parameter allows you to specify the system search sequence. The selections are:

- **Drive A then C:** The system checks drive A first. If there is a diskette in the drive, the system boots from drive A. Otherwise, it boots from drive C.
- **Drive C then A:** The system checks drive C first. If there is a hard disk (drive C) installed, the system boots from drive C. Otherwise, it boots from drive A.
- **C:** The system always boots from drive C.
- **A:** The system always boots from drive A.

3.3.5.6 Boot from CD-ROM

When set to **Enabled**, the system checks for a bootable CD in the CD-ROM drive. If a CD is present, the system boots from the CD-ROM; otherwise, it boots from the drive specified in the System Boot Drive parameter.

When set to **Disabled**, the system boots from the drive specified in the System Boot Drive parameter.

3.4. Advanced Configuration

The Advanced Configuration option allows you to configure the advanced system memory functions.

Do not change any settings in the Advanced Configuration if you are not a qualified technician to avoid damaging the system.

The following screen shows the Advanced Configuration parameters.

```
              Advanced Configuration                Page 1/1

   Memory at 15MB-16MB Reserved for  ... [System]

   PCI IRQ Sharing ..................... [Yes]
   VGA Palette Snoop ................... [Disabled]

   Plug and Play OS .................... [Yes]


   Onboard Peripheral Configuration

   ↑↓ = Move Highlight Bar,  → ← = Change Setting, F1 = Help
```

3.4.1 Memory at 15MB-16MB Reserved For

To prevent memory address conflicts between the system and expansion boards, reserve this memory range for the use of either the system or an expansion board.

3.4.2 PCI IRQ Sharing

Setting this parameter to **Yes** allows you to assign the same IRQ to two different devices. To disable the feature, select **No**.

If there are no IRQs available to assign for the remaining device function, we recommend that you enable this parameter.

3.4.3 VGA Palette Snoop

This parameter permits you to use the palette snooping feature if you installed more than one VGA card in the system.

The VGA palette snoop function allows the control palette register (CPR) to manage and update the VGA RAM DAC (Digital Analog Converter, a color data storage) of each VGA card installed in the system. The snooping process lets the CPR send a signal to all the VGA cards so that they can update their individual RAM DACs. The signal goes through the cards continuously until all RAM DAC data have been updated. This allows display of multiple images on the screen.

Some VGA cards have required settings for this feature. Check your VGA card manual before setting this parameter.

3.4.4 Plug and Play OS

When this parameter is set to **Yes**, BIOS initializes only PnP boot devices such as SCSI cards. When set to **No**, BIOS initializes all PnP boot and non-boot devices such as sound cards.

Set this parameter to **Yes** *only if your operating system is Windows 95.*

3.4.5 Onboard Peripheral Configuration

The Onboard Peripheral Configuration allows you to configure the onboard communication ports and the onboard devices. Selecting this option from the Advanced menu displays the following screen:

```
                Onboard Devices Configuration      Page 1/1

   Serial Port 1 ......................[Enabled ]
      Base Address ....................[378h]
      IRQ .............................[ 4 ]
   Serial Port 2 ......................[Disabled]
      Base Address ....................[----]
      IRQ .............................[----]
   Parallel Port ......................[Enabled ]
      Base Address ....................[378h]
      IRQ .............................[ 7 ]
      Operation Mode ..................[Bidirectional]
      ECP DMA Channel .................[ - ]

   Floppy Disk Controller .............[Enabled]
   IDE Controller .....................[Both]
   Onboard PS/2 Mouse (IRQ 12) ........[Enabled]
   USB Host Controller ................[Enabled]
      USB Legacy Mode .................[Disabled]


  ↑↓ = Move Highlight Bar,  → ← = Change Setting, F1 = Help
```

3.4.5.1 Serial Port 1

This parameter allows you to enable or disable the serial port 1.

3.4.5.1.1 BASE ADDRESS

This function lets you set a logical base address for serial port 1. The options are:

- **3F8h**
- **2F8h**
- **3E8h**
- **2E8h**

3.4.5.1.2 IRQ

This function lets you assign an interrupt for serial port 1. The options are IRQ **3** and **4**.

The Base Address and IRQ parameters are configurable only if Serial Port 1 is enabled.

3.4.5.2 Serial Port 2

This parameter allows you to enable or disable the serial port 2.

3.4.5.2.1 BASE ADDRESS

This function lets you set a logical base address for serial port 2. The options are:

- **3F8h**
- **2F8h**
- **3E8h**
- **2E8h**

3.4.5.2.2 IRQ

This function lets you assign an interrupt for serial port 2. The options are IRQ **3** and **4**.

The Base Address and IRQ parameters are configurable only if Serial Port 2 is enabled.

If you assign 3F8h to serial port 1, you may only assign 2F8h or 2E8h to serial port 2.

If you assign 2F8h to serial port 1, you may only assign 3F8h or 3E8h to serial port 2.

3.4.5.3 Parallel Port

This parameter allows you to enable or disable the parallel port.

3.4.5.3.1 BASE ADDRESS

This function lets you set a logical base address for the parallel port. The options are:

- **3BCh**
- **378h**
- **278h**

3.4.5.3.2 IRQ

This function lets you assign an interrupt for the parallel port. The options are IRQ **5** and **7**.

The Base Address and IRQ parameters are configurable only if Parallel Port is enabled.

If you install an add-on card that has a parallel port whose address conflicts with the parallel port onboard, the system automatically disables the onboard functions.

Check the parallel port address on the add-on card and change the address to one that does not conflict

3.4.5.3.3 OPERATION MODE

This item allows you to set the operation mode of the parallel port. Table 3-1 lists the different operation modes.

Table 3-1 Parallel Port Operation Mode Settings

Setting	Function
Standard Parallel Port (SPP)	Allows normal speed one-way operation
Standard and Bidirectional	Allows normal speed operation in a two-way mode
Enhanced Parallel Port (EPP)	Allows bidirectional parallel port operation at maximum speed
Extended Capabilities Port (ECP)	Allows parallel port to operate in bidirectional mode and at a speed higher than the maximum data transfer rate

3.4.5.3.4 ECP DMA CHANNEL

This item becomes active only if you select **`Extended Capabilities Port (ECP)`** as the operation mode. It allows you to assign DMA channel 1 or DMA channel 3 for the ECP parallel port function (as required in Windows 95).

3.4.5.4 Floppy Disk Controller

This parameter lets you enable or disable the onboard floppy disk controller.

3.4.5.5 Onboard IDE Controller

This parameter lets you enable or disable the IDE controller on board.

3.4.5.6 Onboard PS/2 Mouse (IRQ 12)

This parameter enables or disables the onboard PS/2 mouse. When enabled, it allows you to use the onboard PS/2 mouse assigned with IRQ12. When disabled, it deactivates the mouse and makes IRQ12 available for use of other devices.

3.4.5.7 USB Host Controller

This parameter lets you enable or disable the USB controller on board. When enabled, it activates the USB function of the system. When disabled, it also deactivates the function.

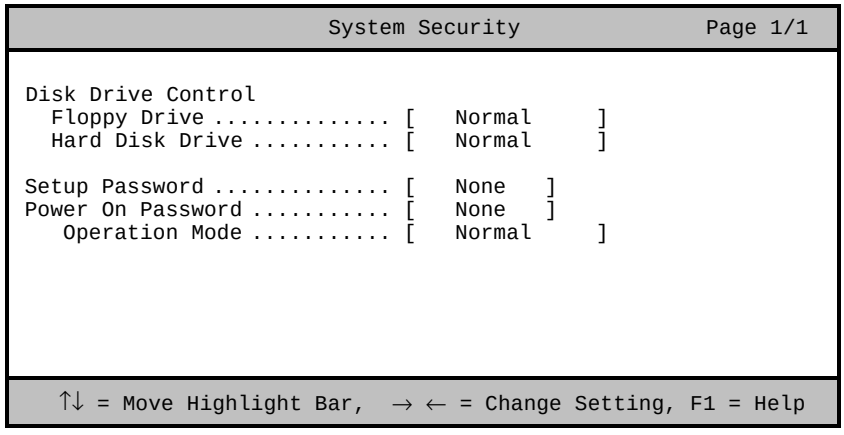
3.4.5.7.1 USB LEGACY MODE

This function, when enabled, lets you use a USB keyboard in DOS environment. Set this to **Disabled** to deactivate the USB keyboard function in DOS environment.

3.5. System Security Setup

The Setup program has a number of security features to prevent unauthorized access to the system and its data.

The following screen appears if you select System Security from the Main menu:



3.5.1 Disk Drive Control

The disk drive control features allow you to control the floppy drive or the hard disk drive boot function to prevent loading operating systems or other programs from a certain drive while the other drives are operational.

Table 3-2 lists the drive control settings and their corresponding functions.

Table 3-2 Drive Control Settings

Floppy Drive	
Setting	**Description**
Normal	Floppy drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all floppy drive functions
Hard Disk Drive	
Setting	**Description**
Normal	Hard disk drive functions normally
Write Protect All Sectors	Disables the write function on all sectors
Write Protect Boot Sector	Disables the write function only on the boot sector
Disabled	Disables all hard disk functions

3.5.2 Setup Password

The Setup Password prevents unauthorized access to the BIOS utility.

3.5.2.1 Setting a Password

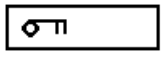
1. Make sure that switch 1 of S1 is set to **On** (bypass password).

   You cannot enter the BIOS utility if a Setup password does not exist and switch 1 of S1 is set to **Off** *(password check enabled).*

   By default, switch 1 of S1 is set to **On** *(bypass password).*

2. Enter BIOS utility and select System Security.

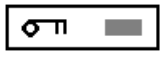
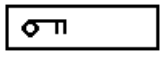
3. Highlight the Setup Password parameter and press the ↑ or ↓ key. The password prompt appears:



4. Type a password. The password may consist of up to seven characters.

   Be very careful when typing your password because the characters do not appear on the screen.

5. Press ENTER. A prompt asks you to retype the password to verify your first entry.

6. Retype the password then press ENTER.

   After setting the password, the system automatically sets the Setup Password parameter to **Present**.

7. Press ESC to exit the System Security screen and return to the Main menu.

8. Press ESC to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.

9. Select **Yes** to save the changes and reboot the system.

10. While rebooting, turn off the system then open the housing.

11. Set switch 1 of S1 to **Off** to enable the password function.

The next time you want to enter the BIOS utility, you must key-in your Setup password.

3.5.2.2 Changing or Removing the Setup Password

Should you want to change your setup password, do the following:

1. Enter the BIOS utility and select System Security.

2. Highlight the Setup Password parameter.

3. Press ← or → to display the password prompt and key-in a new password.

   or

   Press ← or → and select **None** to remove the existing password.

4. Press ESC to exit the System Security screen and return to the Main menu.

5. Press ESC to exit the BIOS utility. A dialog box appears asking if you want to save the CMOS data.

6. Select **Yes** to save the changes.

3.5.2.3 Bypassing the Setup Password

If you forget your setup password, you can bypass the password security feature by hardware. Follow these steps to bypass the password:

1. Turn off and unplug the system.

2. Open the system housing and switch 1 of S1 is set to **On** to bypass the password function.

3. Turn on the system and enter the BIOS utility. This time, the system does not require you to type in a password.

You can either change the existing Setup password or remove it by selecting **None***. Refer to the previous section for the procedure.*

3.5.3 Power On Password

The Power On Password secures your system against unauthorized use. Once you set this password, you have to type it whenever you boot the system. To set this password, enter the BIOS utility, select System Security, then highlight the Power On Password parameter. Follow the same procedure as in setting the Setup password.

Make sure to set switch 1 of S1 to **`Off`** *to enable the Power On password.*

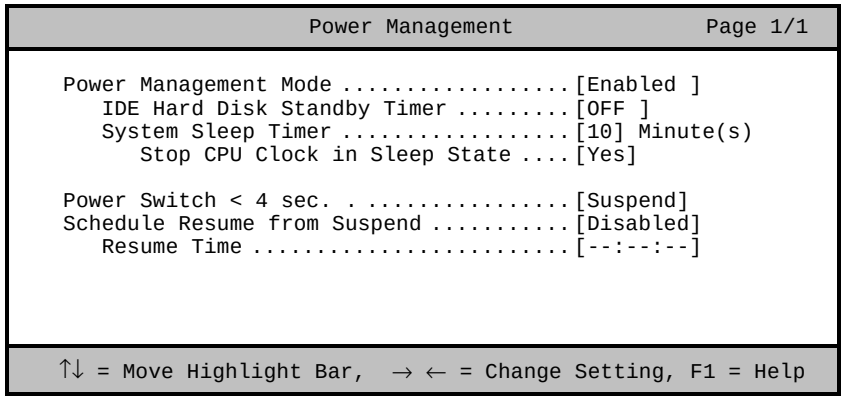
3.5.3.1 Operation Mode

This function lets you enable or disable the password prompt display. When set to **`Normal`**, the password prompt appears before system boot. When set to **`Network`**, the password prompt do not appear; however, the keyboard will be locked after system boot and will remain locked until the correct password is entered.

3.6. Power Management

The Power Management menu lets you configure the system power-management feature.

The following screen shows the Power Management parameters and their default settings:



3.6.1 Power Management Mode

This parameter allows you to reduce power consumption. When this parameter is set to **Enabled**, you can configure the IDE hard disk and system timers. Setting to **Disabled** deactivates the power-management feature and all the timers.

3.6.1.1 IDE Hard Disk Standby Timer

This parameter allows the hard disk to enter standby mode after inactivity of 1 to 15 minutes, depending on your setting. When you access the hard disk again, allow 3 to 5 seconds (depending on the hard disk) for the disk to return to normal speed. Set this parameter to **OFF** if your hard disk does not support this function.

3.6.1.2 System Sleep Timer

This parameter sets the system to the lowest power-saving mode. It automatically enters the sleep or the suspend mode after a specified period of inactivity. Any keyboard or mouse action detected resume system operation.

3.6.1.2.1 STOP CPU CLOCK IN SLEEP STATE

If you want to stop the CPU clock when the system enters the sleep or suspend mode, set this parameter to **Yes**. If not, then select **No**.

3.6.2 Power Switch < 4 sec.

When set to **Power-off,** the system automatically turns off when the power switch is pressed for less than 4 seconds. When set to **Suspend**, the system enters the suspend mode.

3.6.3 Schedule Resume from Suspend

This option lets you enable or disable the automatic system resume function. This function allows you to specify the time when to resume the system from suspend mode. You can specify the time in the Resume Time parameter.

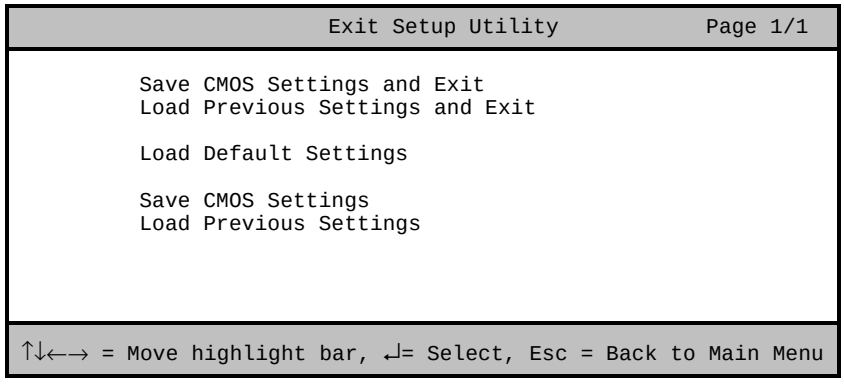
3.6.4 Resume Time

This parameter lets you specify the time when to resume the system from suspend mode to normal mode. The time setting is in hour-minute-second format.

This parameter is configurable only when the Schedule Resume function is enabled.

3.7. Exit Setup Utility

To exit the BIOS utility, select Exit Setup Utility from the Main menu. The following screen appears:



3.7.1 Save CMOS Settings and Exit

Select this option if you want to save the current CMOS settings and exit the BIOS utility.

3.7.2 Load Previous Settings and Exit

Select this option to cancel the current changes made to the BIOS settings, reload the previous settings and exit the BIOS utility after reload.

3.7.3 Load Default Settings

This option loads the default settings for the optimized system configuration. After loading the settings, you return to the Main menu. Press ESC to leave the BIOS utility.

3.7.4 Save CMOS Settings

Select this option to save the current BIOS settings, including your recent modifications. After saving, you return to the Main menu. Press ESC to leave the BIOS utility.

3.7.5 Load Previous Settings

This option cancels all modifications that you have made in the system configuration and reloads your previous settings. After reload, you return to the Main menu. Press ESC to leave the BIOS utility.

Model Number Definition

(1) Trade Mark: Acer

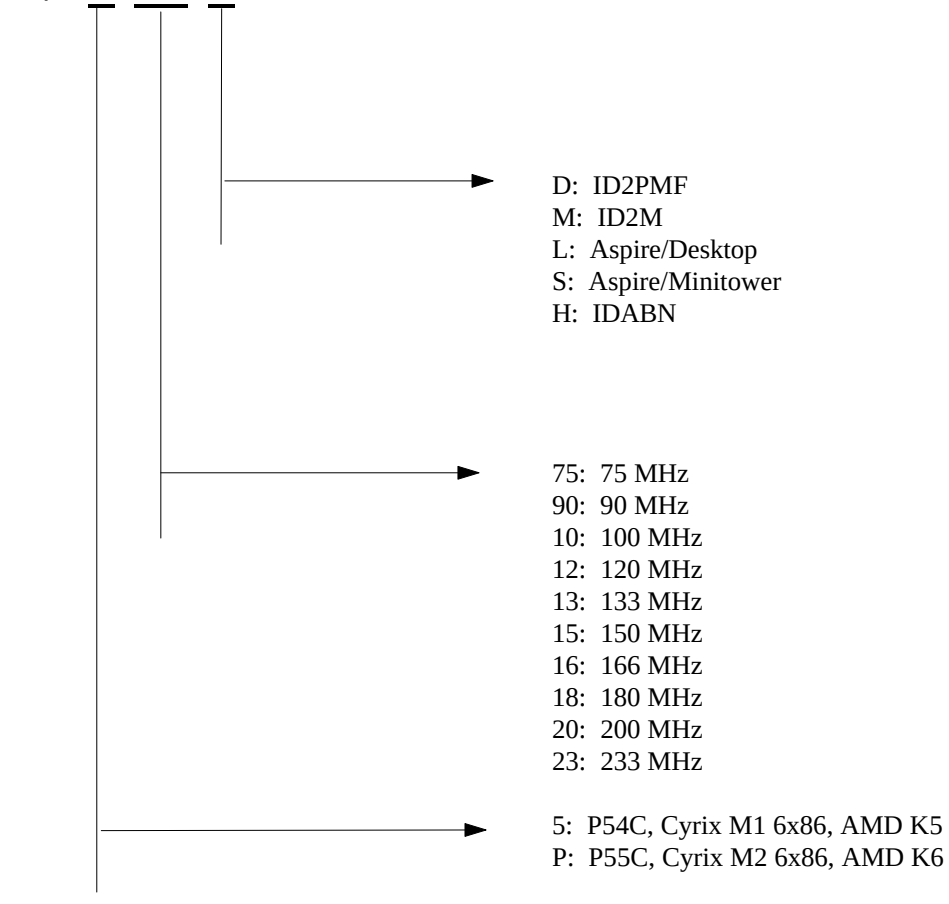
(2) Brand Name: AcerPower

(3) Product Name: 64-bit Computer System

(4) Description:

(5) Model No.:

VKX XX X



Spare Parts List

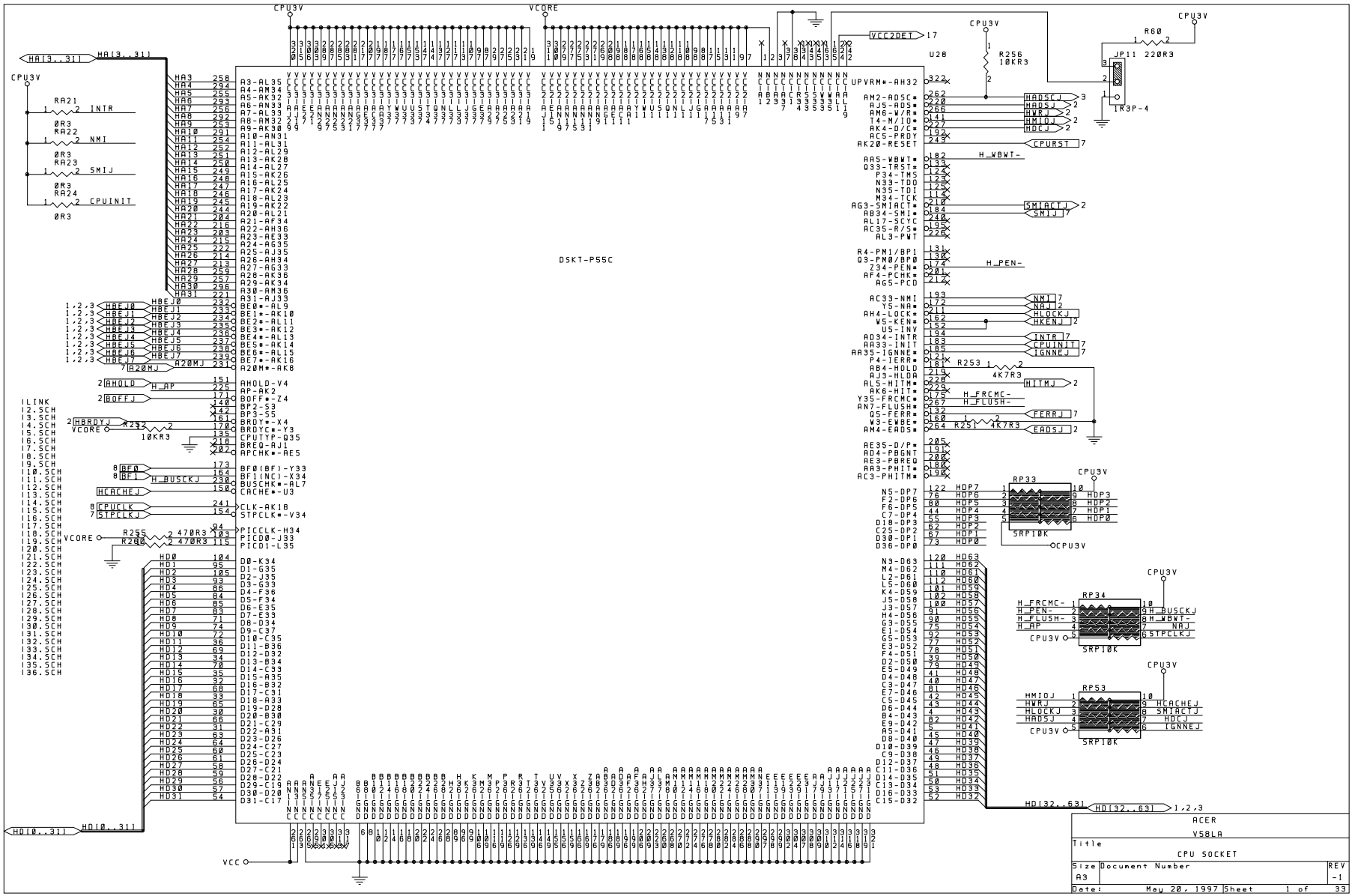
This appendix lists the spare parts for the system board with their part numbers.

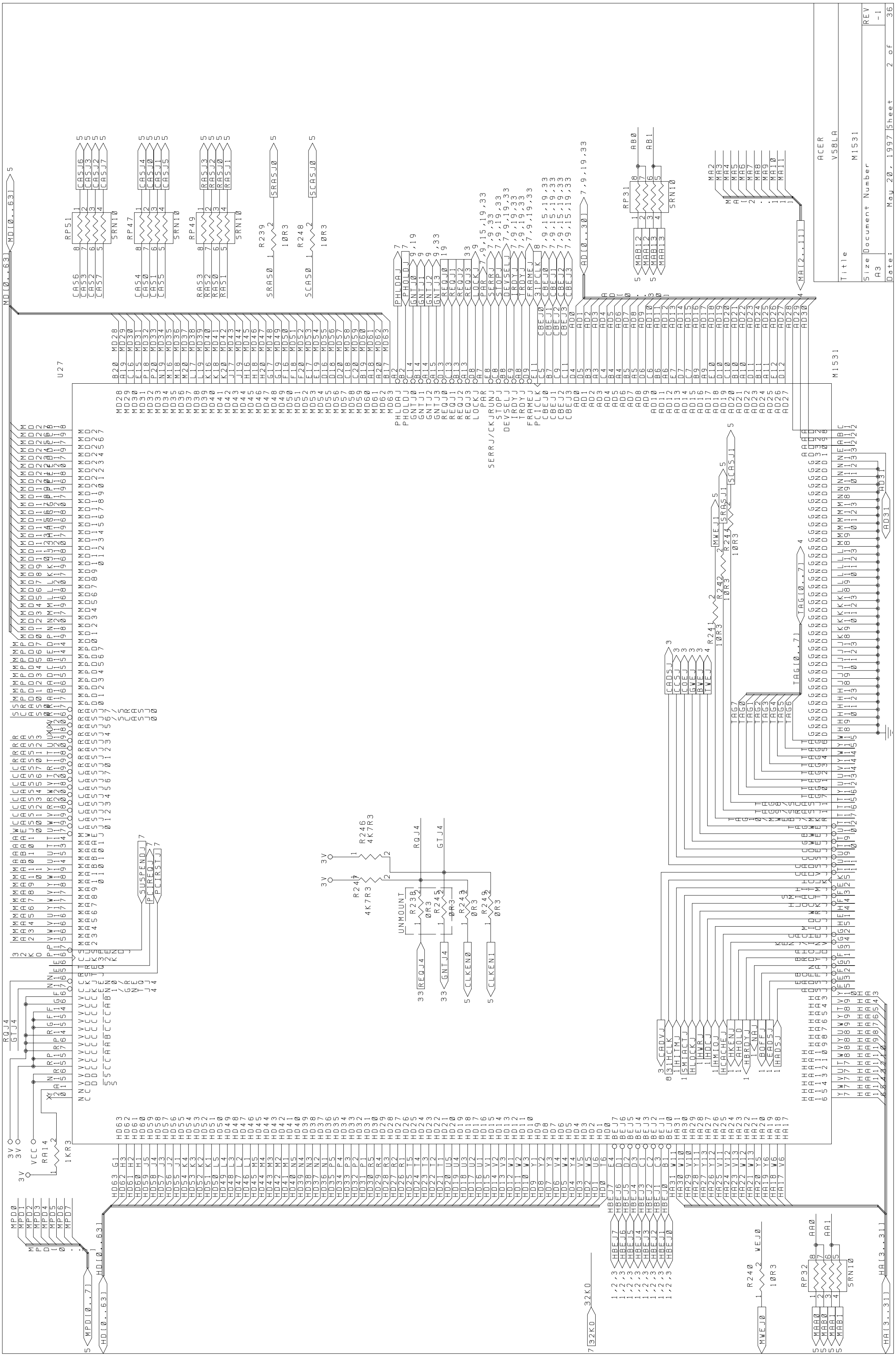
Table B-1 Spare Parts List

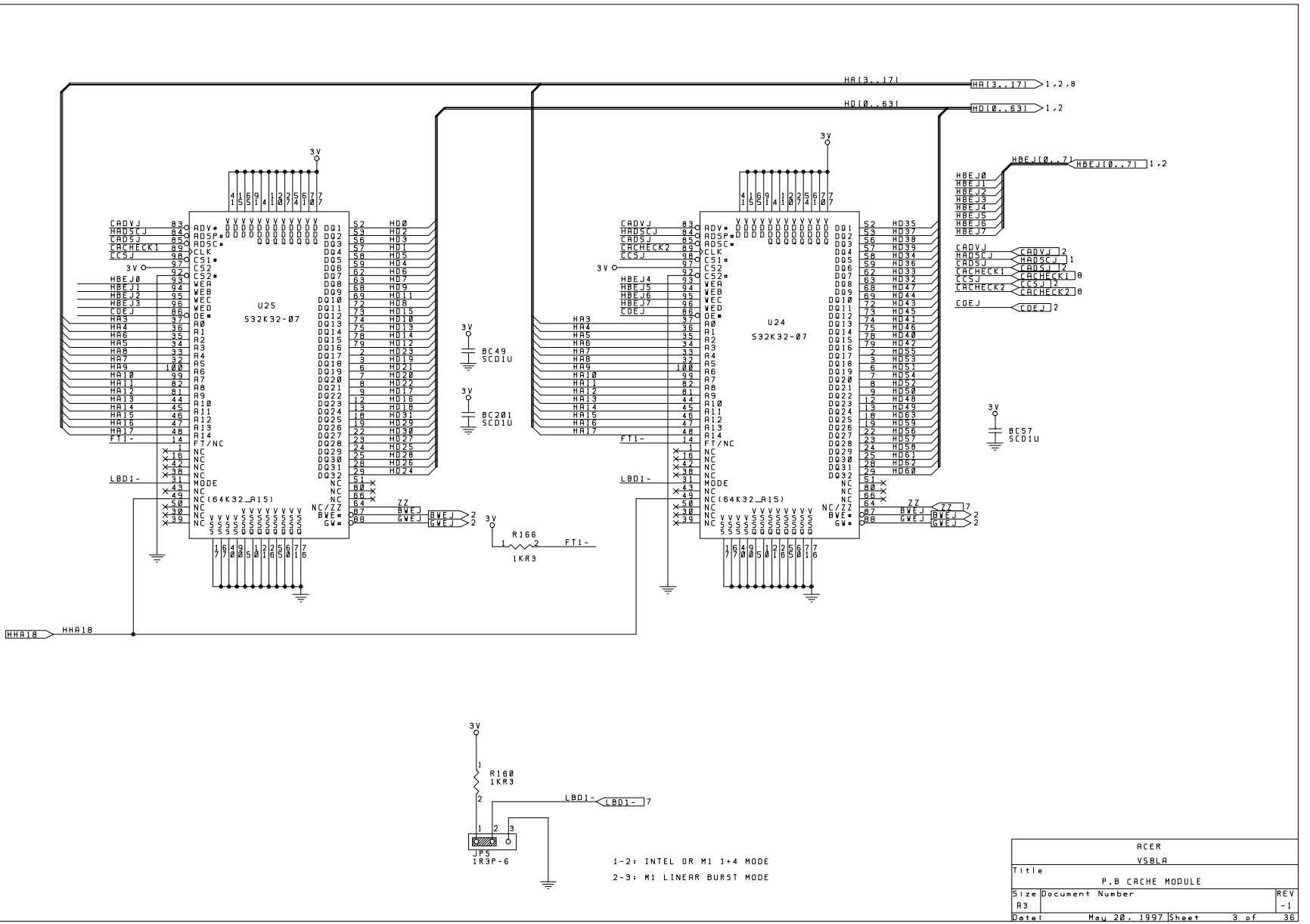
Part Name	Part No.	Comment/Location	Min. Qty.
IC EEPRM 29EE020-150 256K*8 5V	02.29020.060	U23	1
IC EEPROM HY93C46 64*16 DIP 8P	02.93C46.000	73.03244.C0B	10
IC V.R EZ1082CT TO-220 3P	04.01082.030	U29	10
IC A.R LX8383A-00CP TO-220 3P	04.08383.03A	U30	10
SKT IC DIP 8P D7.62MM	22.10001.008	U8	50
SKT IC DIP 32P D15.24MM	22.10002.032	U23	50
SKT DIMM 168P ST 71736-0011	22.10220.168	DIM2 DIM1	50
BATTERY LI 3V CR2032 200MAH	23.20023.001	BT1	50
XTAL 32.768KHZ 12.5PF D3*8L	23.30030.011	X2 X1	50
XTAL 14.31818MHZ 32P 30PPM H5	23.31001.001	X3 X4	50
OSC 25MHZ HALF CMOS	24.30016.011	OSC1	50
V58LA MB 0MB GT 4MB 256K S L	55.53201.001		1
TRANSFORMER PE-68515 SMD	68.00087.301	U1	10
IC G.A MAGPACK PLCC 44P	71.00MAG.00C	U7	10
IC CLK GEN CY2273 SSOP 48P	71.02273.00I	U41	10
IC VGA CHIP ATI264GT B2U3 PQFP	71.264GT.B3E	U37	1
IC PNP CTRL FDC37C935APM V.C	71.37935.C0E	U20	10
IC INTF. 82555 B3 MQFP 100P	71.82555.B09	U2	1
IC FAST ETHERNET 82557 V.C QFP	71.82557.C1E	U21	1
IC M1533 A0-D	71.M1533.D0U	U38	10
IC SRAM W25P022AF-6 64K*32WINB	72.25022.005	U24 U25	10
IC SGRAM 481850-100M 128K*32*2	72.48185.A05	U33 U34	10
IC SRAM 61L256BS-12 32K*8 SOJ	72.61256.28B	U26	10
IC CMOS QS3125 QSOP 16P	73.03125.0BC	U6	50
IC BUS SW 74CBT3244 TSSOP 20P	73.03244.C0B	U5	10

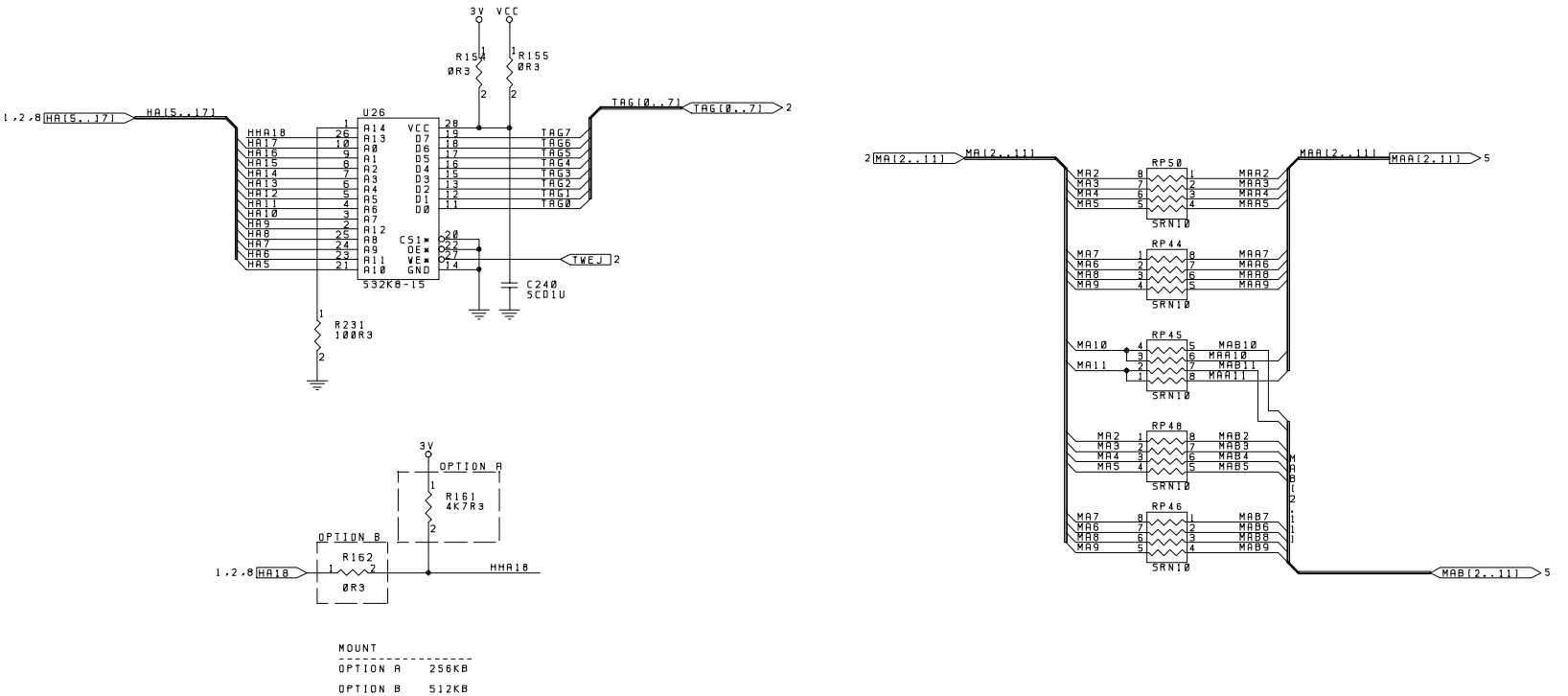
A p p e n d i x C

Schematics

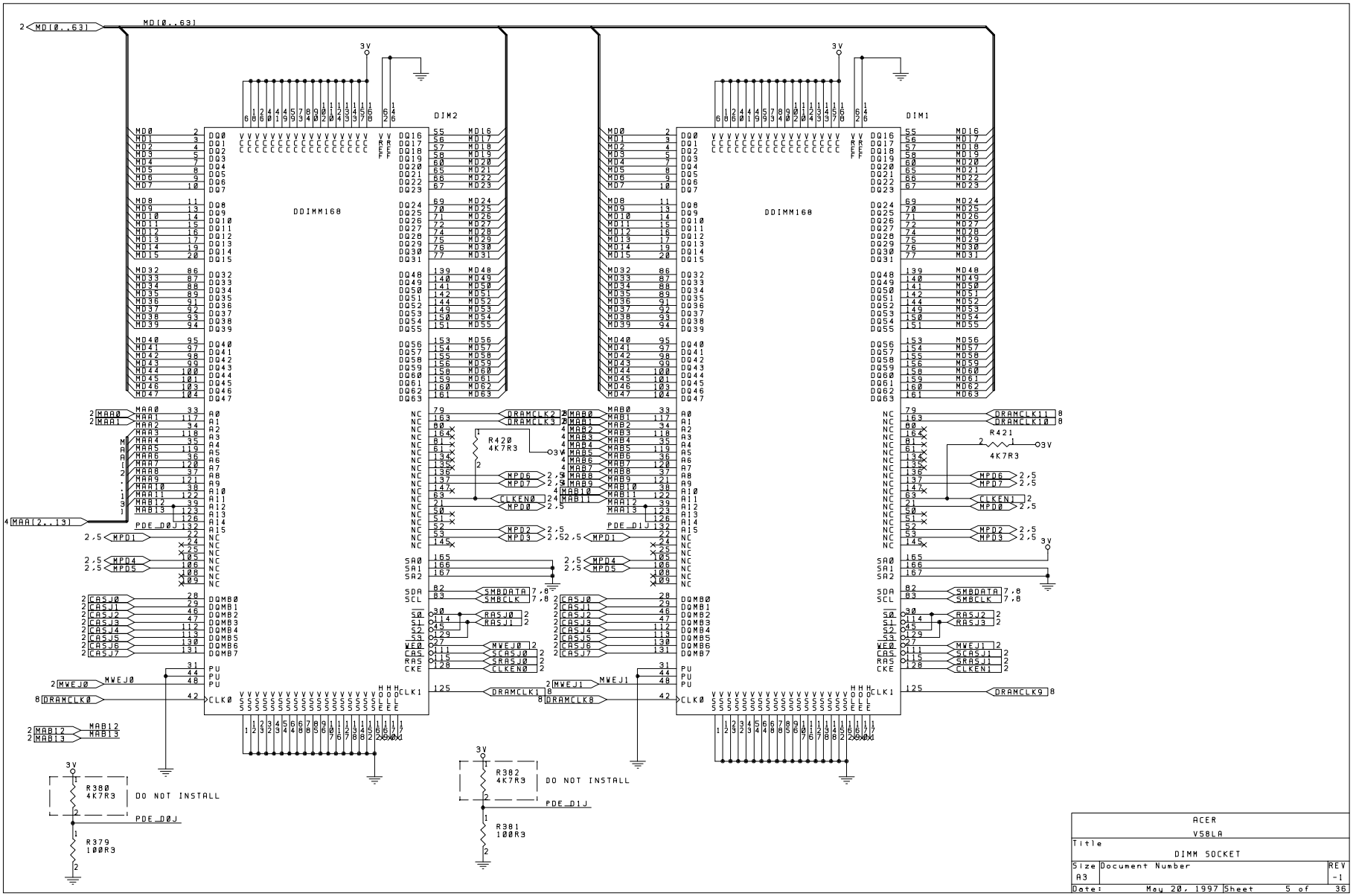

CPU3V
VCORE
VCC2DET
U28
DSKT-P55C
R256 10KR3
R60
JP11 220R3
JP1 1R3P-4
RA21 INTR
RA22 NMI
RA23 SMIJ
RA24 CPUINIT
ØR3
HA[3..31]
HD[0..31]
HD[32..63]
H_WBWT-
H_PEN-
H_FRCMC-
H_FLUSH-
H_AP
H_BUSCKJ
HCACHEJ
A20MJ
R253 4K7R3
R251 4K7R3
R255 470R3
R260 470R3
R252 10KR3
RP33
RP34
RP53
SRP10K
ACER
VS8LA
CPU SOCKET
Size A3
Document Number
REV -1
Date: May 20, 1997
Sheet 1 of 33

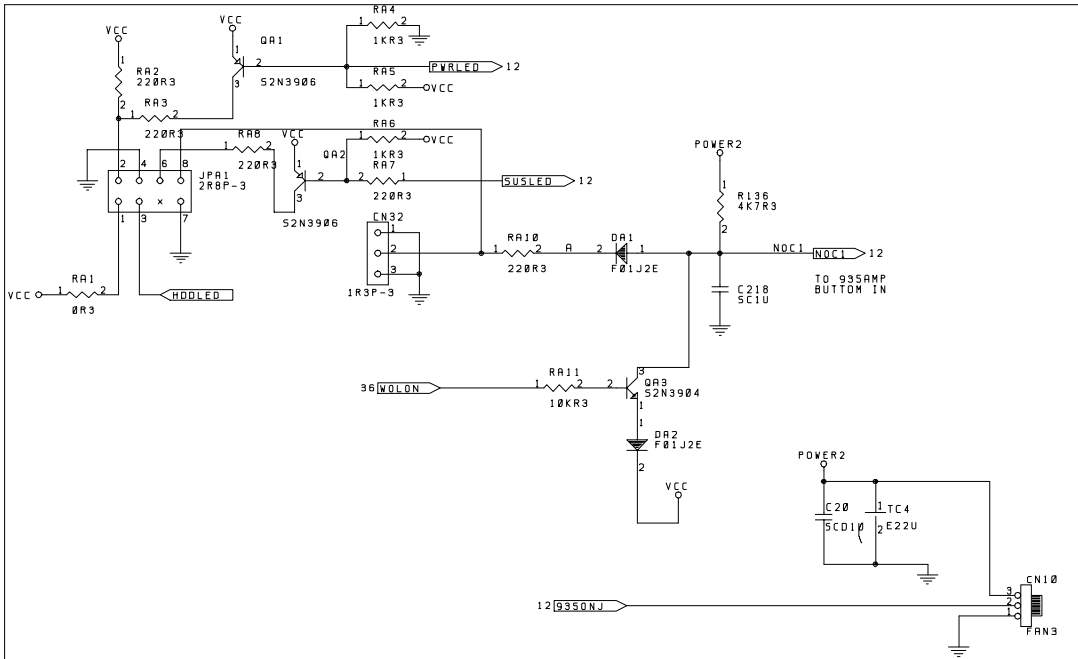

ACER
V58LA
M1531
Title
Size Document Number
A3
Date: May 20, 1997 Sheet 2 of 36
REV
-1


HA[3..17]
HA[3..17] 1,2,8
HD[0..63]
HD[0..63] 1,2
HBEJ[0..7]
HBEJ[0..7] 1,2
U25
532K32-07
U24
532K32-07
3V
BC49
SCD1U
BC201
SCD1U
BC57
SCD1U
R166
1KR3
FT1-
R160
1KR3
LBD1-
LBD1- 7
HHA18
HHA18
JP5
1R3P-6
1-2: INTEL OR M1 1+4 MODE
2-3: M1 LINEAR BURST MODE
ACER
V58LA
Title
P.B CACHE MODULE
Size
A3
Document Number
REV
-1
Date: May 20, 1997
Sheet 3 of 36

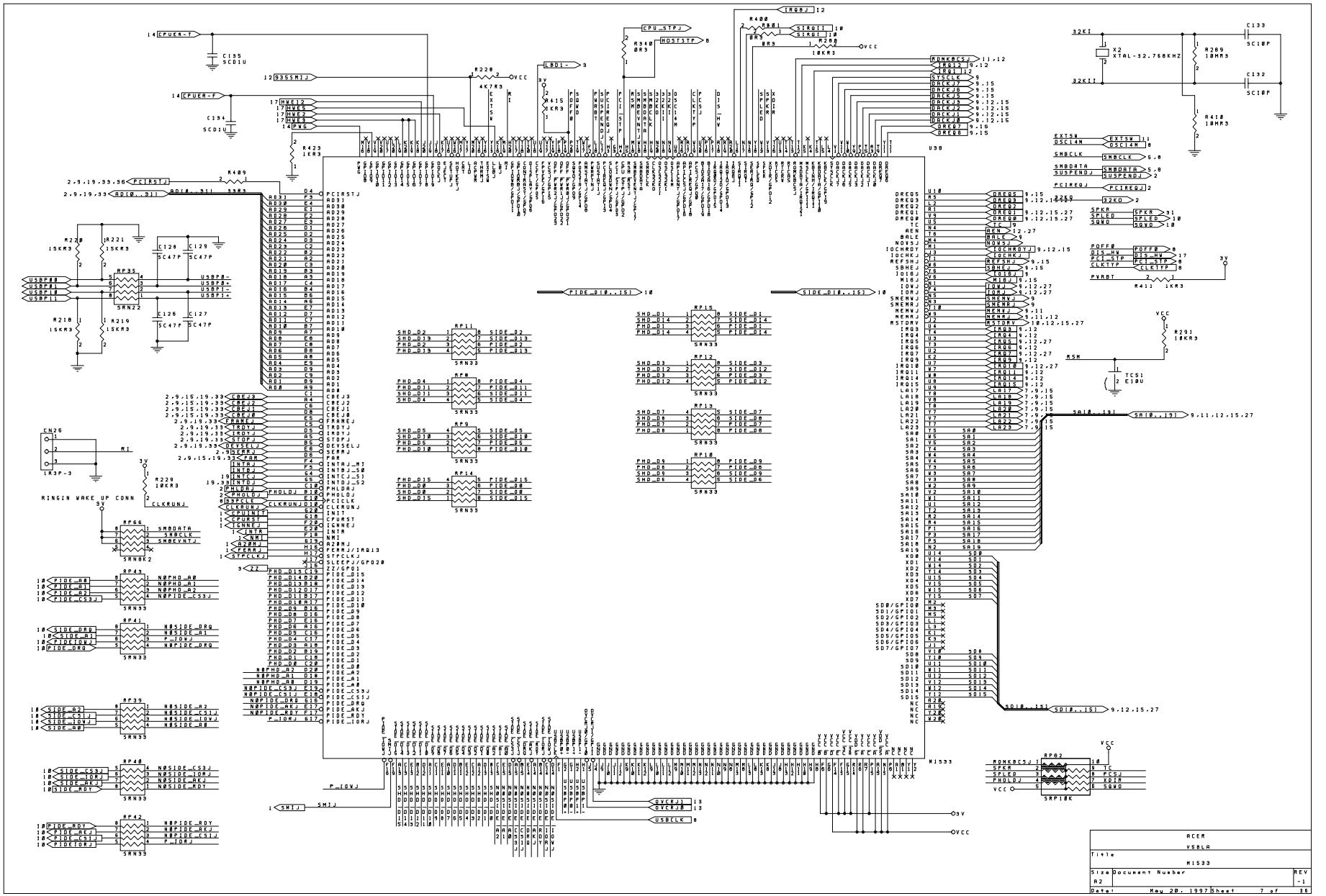


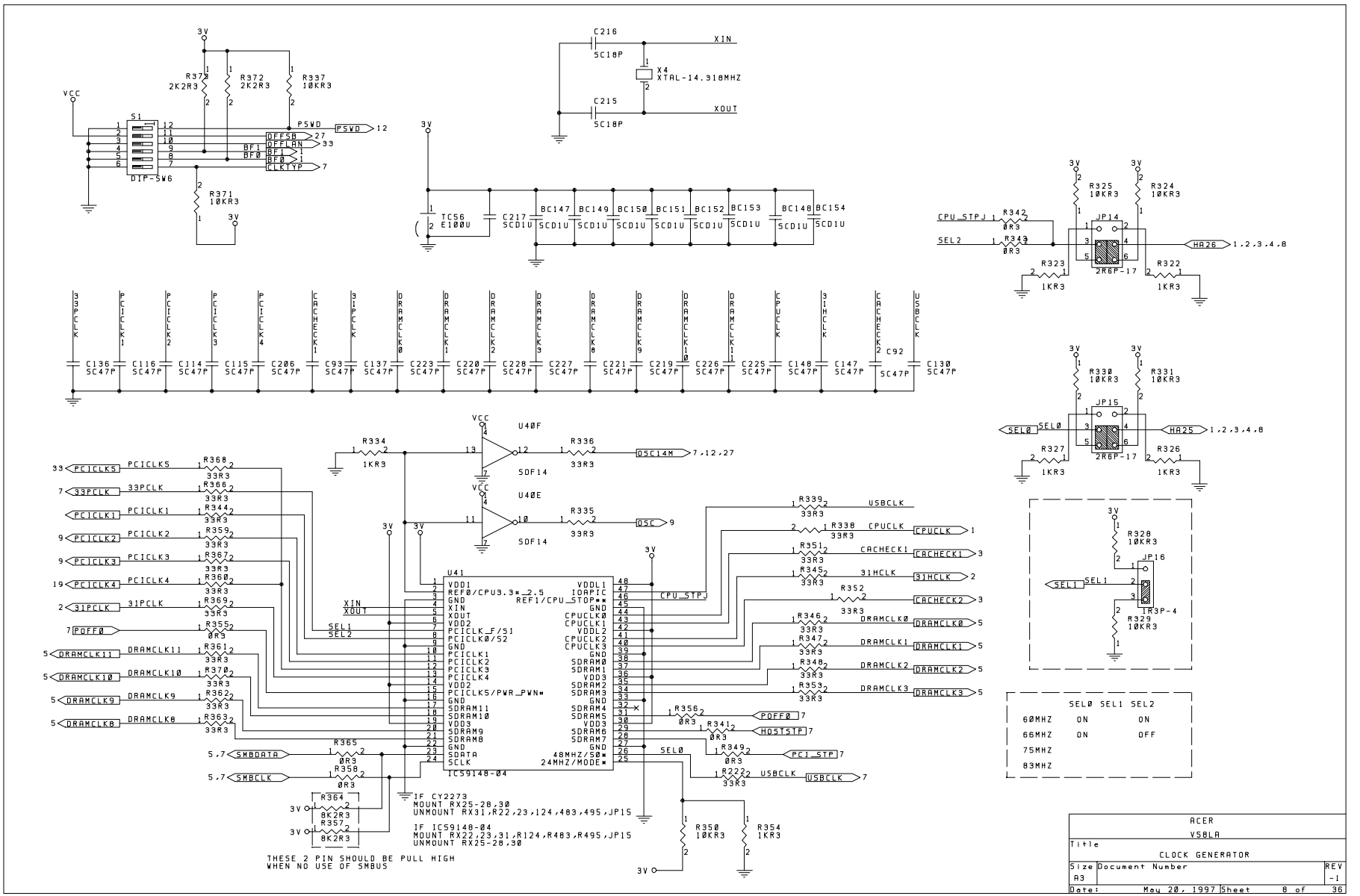
ACER		
V58LA		
Title	TAG SRAM	
Size A3	Document Number	REV -1
Date: May 20, 1997	Sheet 4 of 36	

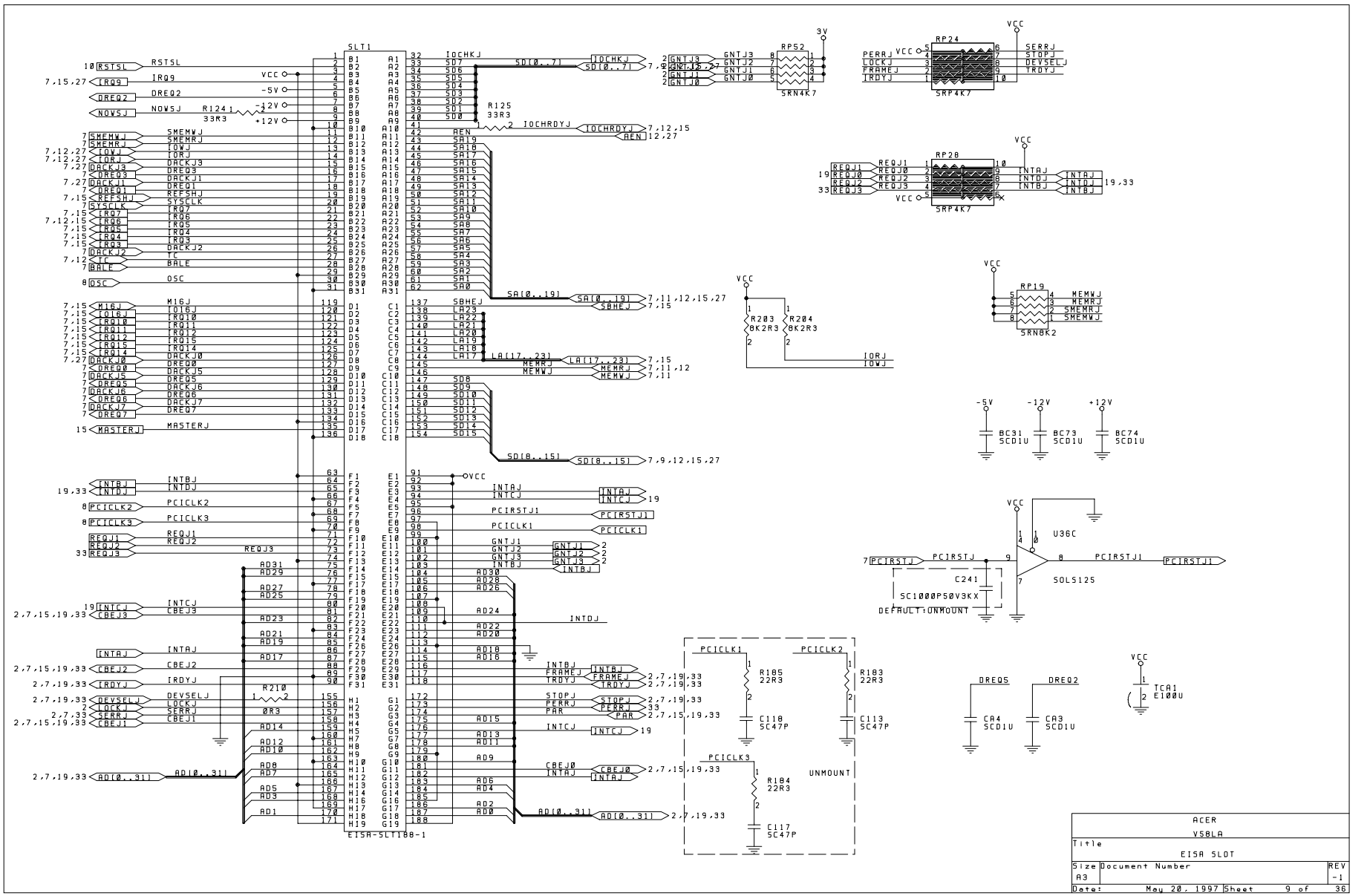

MD[0..63]
DIM2
DIM1
DDIMM168
3V
DO NOT INSTALL
R380 4K7R3
R379 100R3
R382 4K7R3
R381 100R3
R420 4K7R3
R421 4K7R3
PDE_D0J
PDE_D1J
ACER
V58LA
DIMM SOCKET
Size A3
Document Number
REV -1
Date: May 20, 1997
Sheet 5 of 36

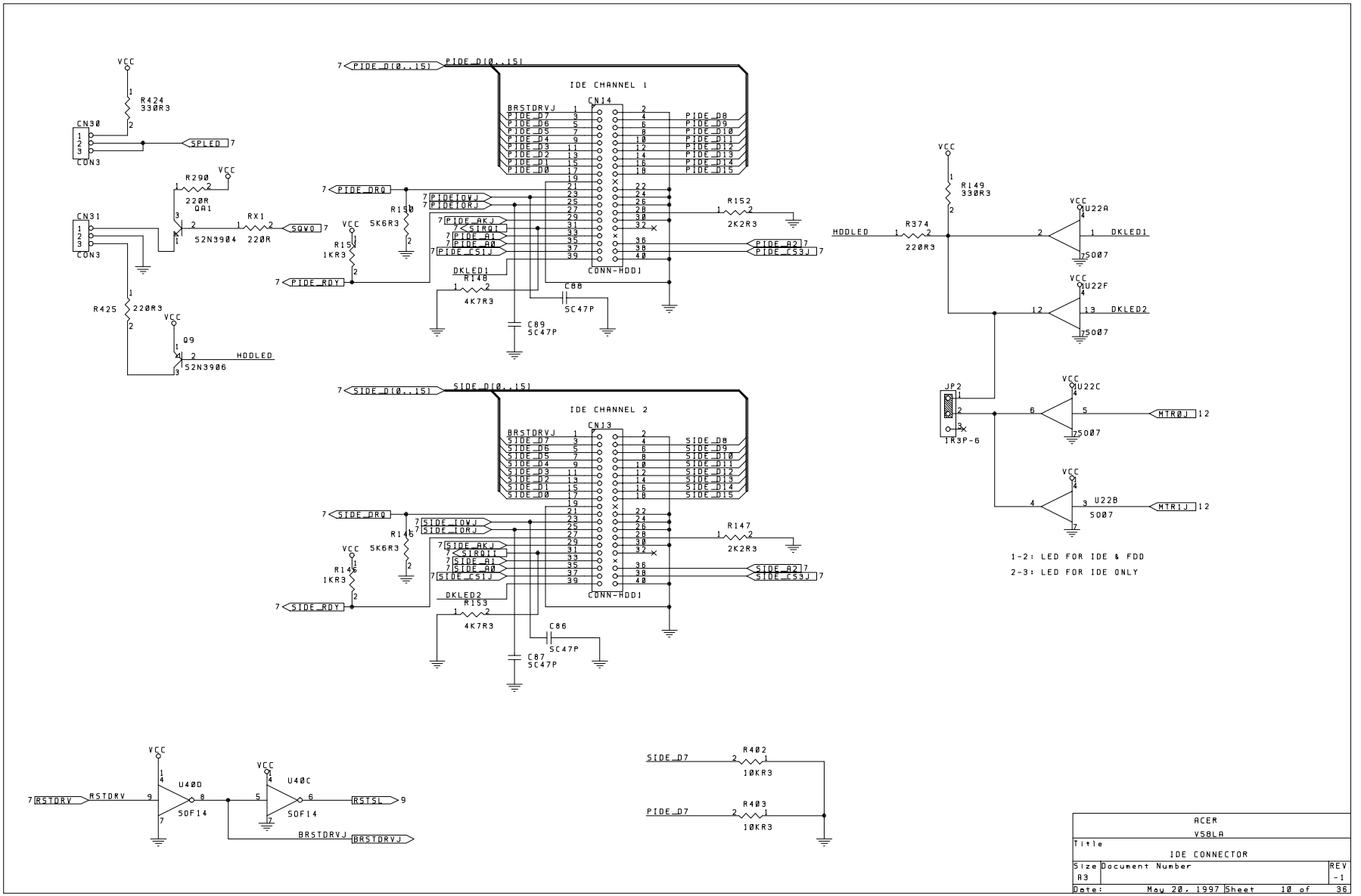


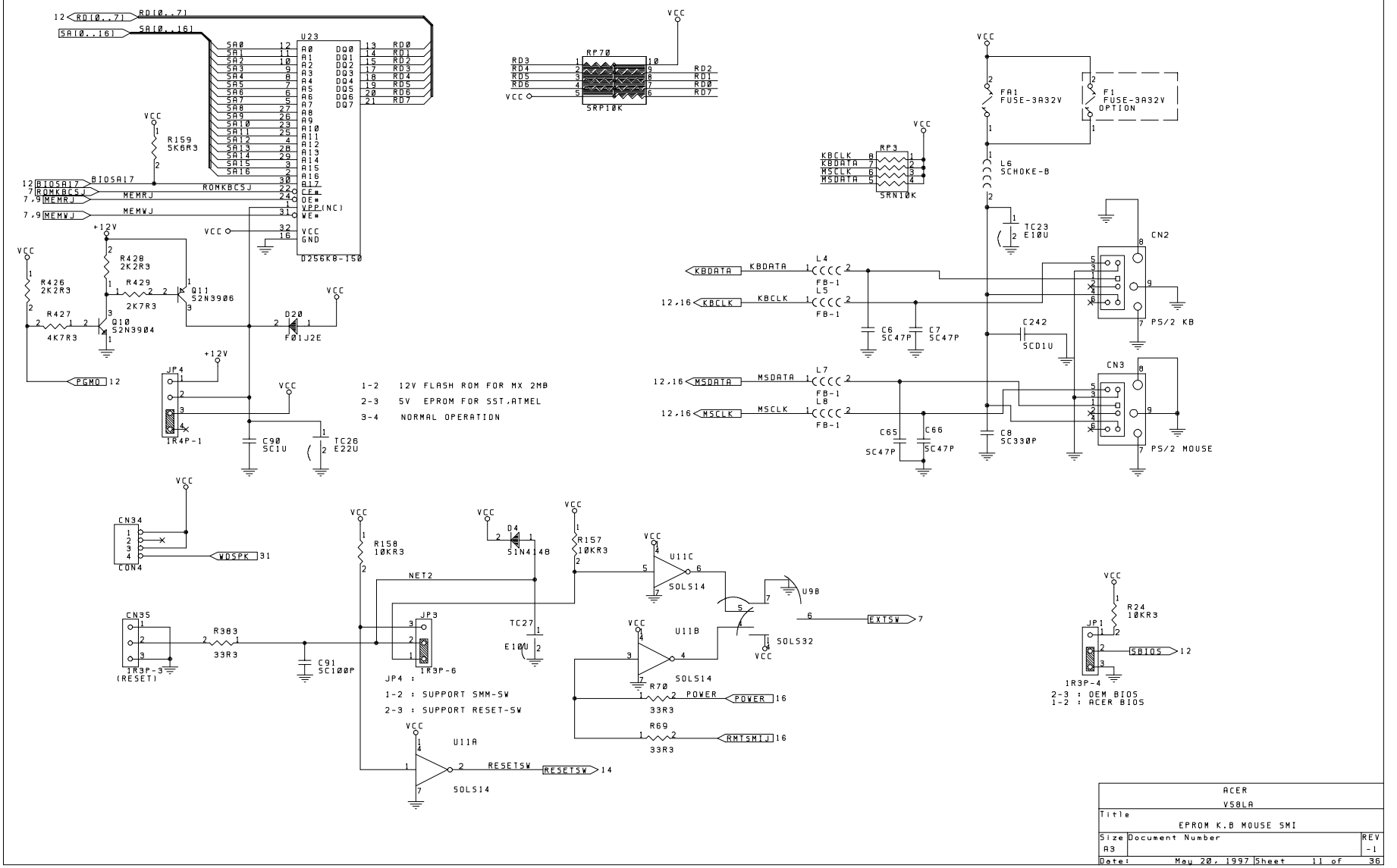
ACER		
V58LA		
Title: POWER ON/OFF ROUTING		
Size: A3	Document Number	REV: -1
Date: May 20, 1997	Sheet 6 of 36	

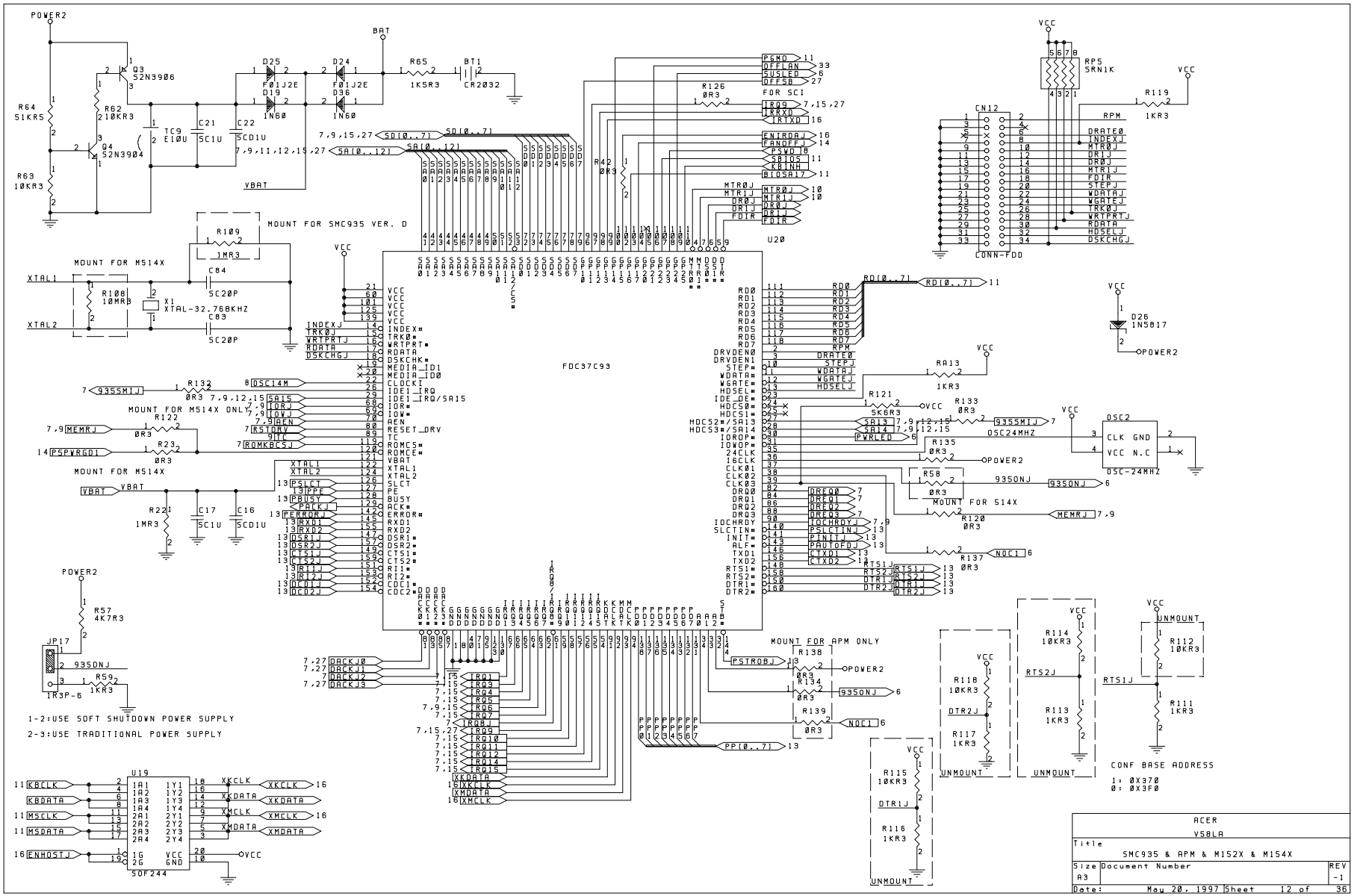

ACER
VSBLA
Title
M1533
Size Document Number
REV
A2
-1
Date: May 20, 1997 Sheet 7 of 36

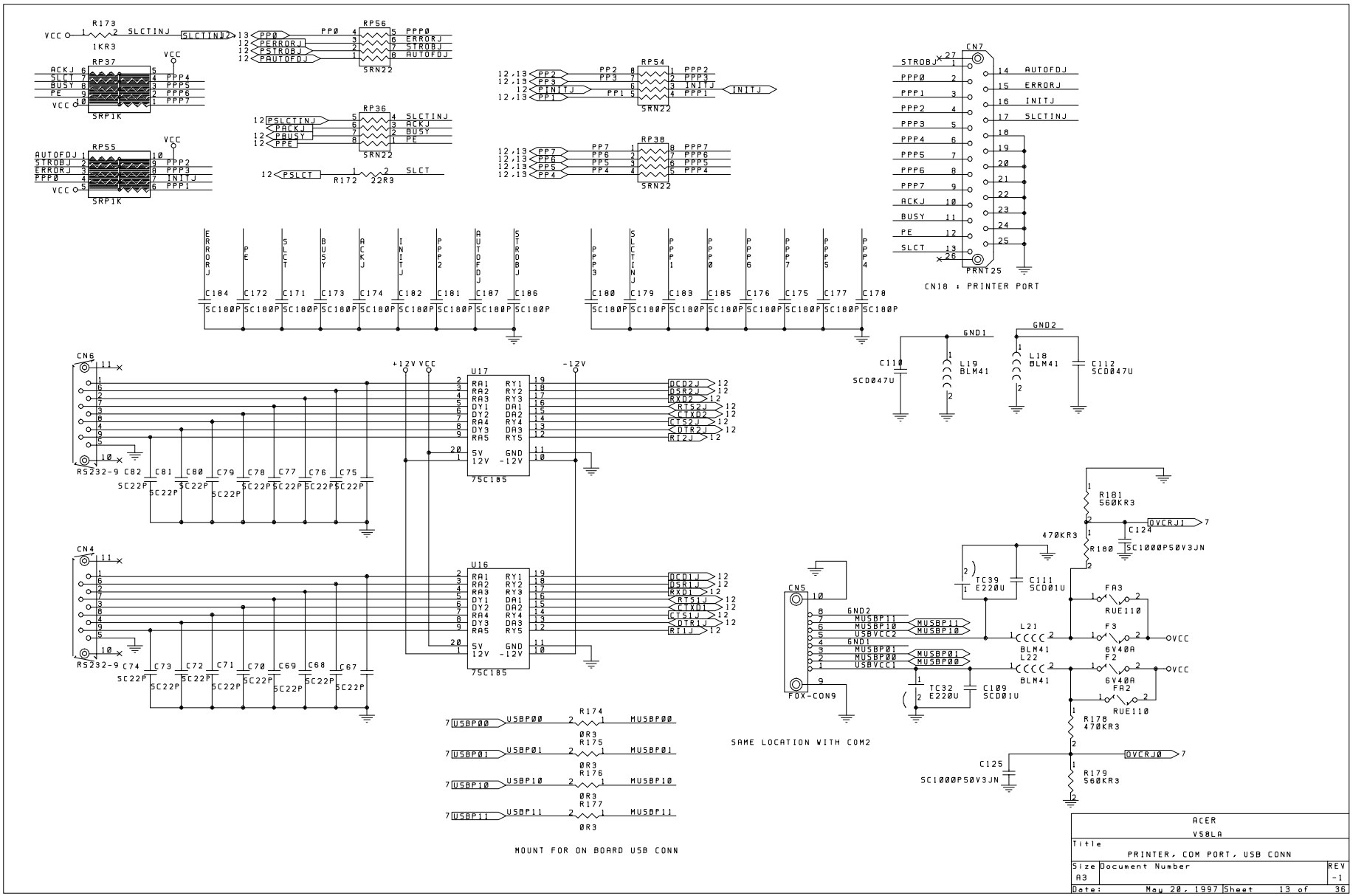

U41
IC59148-04
U40F
U40E
SOF14
DIP-SW6
TC56 E100U
XTAL-14.318MHZ
ACER
V50LA
CLOCK GENERATOR
Size A3
Document Number
REV -1
Date: May 20, 1997 Sheet 8 of 36
SEL0 SEL1 SEL2
60MHZ ON ON
66MHZ ON OFF
75MHZ
83MHZ
THESE 2 PIN SHOULD BE PULL HIGH WHEN NO USE OF SMBUS

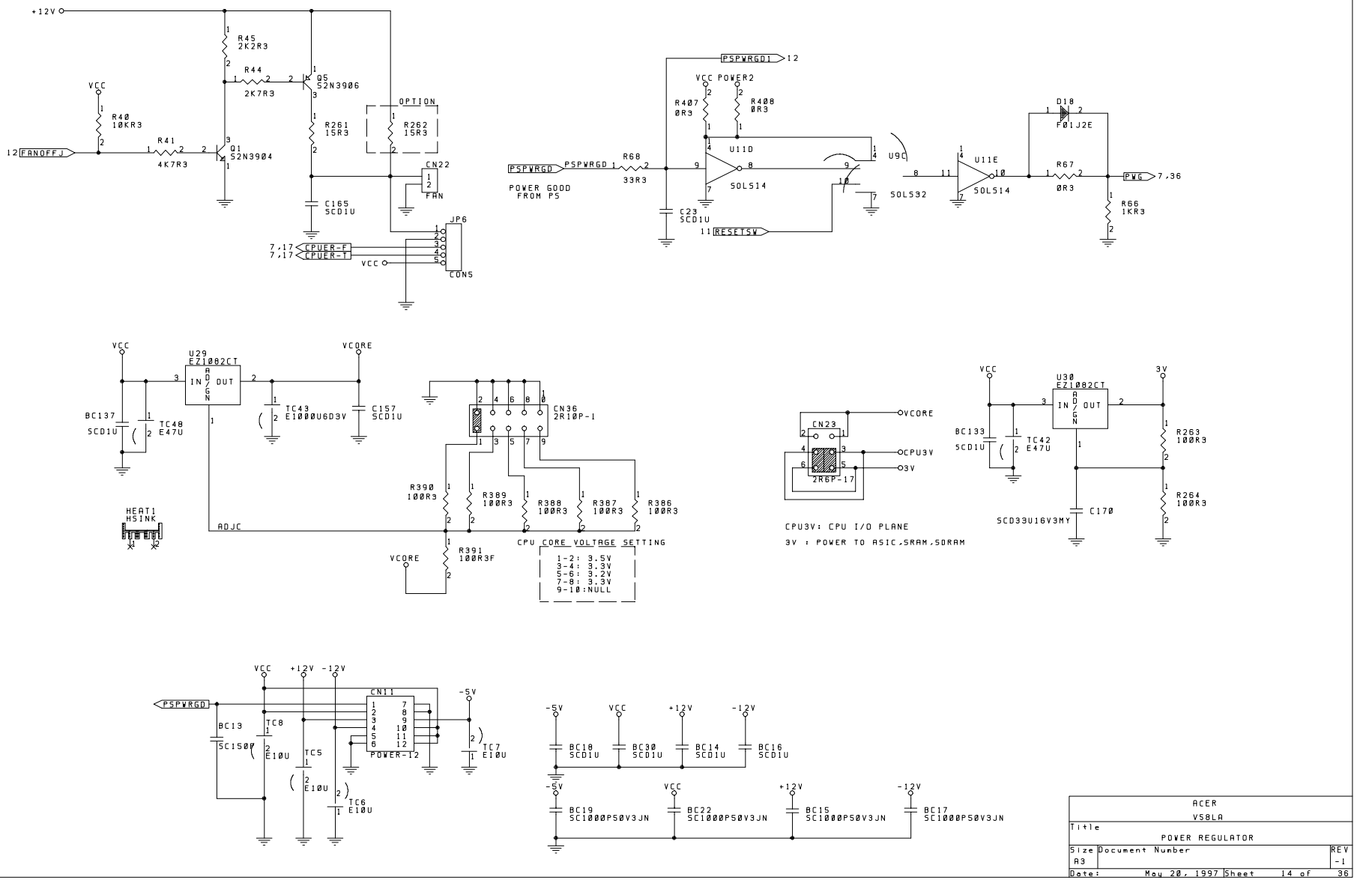

SLT1
EISA-SLT188-1
RP52
SRN4K7
RP24
SRP4K7
RP28
SRP4K7
RP19
SRN8K2
R210
0R3
R125
33R3
R1241
33R3
R203
8K2R3
R204
8K2R3
U36C
SOLS125
C241
SC1000P50V3KX
DEFAULT:UNMOUNT
C118
SC47P
C113
SC47P
C117
SC47P
R185
22R3
R183
22R3
R184
22R3
UNMOUNT
BC31
SCD1U
BC73
SCD1U
BC74
SCD1U
CA4
SCD1U
CA3
SCD1U
TCA1
E100U
-5V
-12V
+12V
3V
VCC
SD[0..7]
SA[0..19]
SD[8..15]
LA[17..23]
AD[0..31]
IOCHKJ
IOCHRDYJ
AEN
SBHEJ
MEMRJ
MEMWJ
IORJ
IOWJ
INTAJ
INTBJ
INTCJ
INTDJ
PCIRSTJ
PCIRSTJ1
PCICLK1
PCICLK2
GNTJ1
GNTJ2
GNTJ3
GNTJ0
REQJ1
REQJ2
REQJ3
REQJ0
FRAMEJ
IRDYJ
TRDYJ
STOPJ
DEVSELJ
PERRJ
SERRJ
PAR
LOCKJ
CBEJ0
CBEJ1
CBEJ2
CBEJ3
MASTERJ
ACER
VS8LA
Title
EISA SLOT
Size
A3
Document Number
REV
-1
Date: May 20, 1997
Sheet 9 of 36


IDE CHANNEL 1
IDE CHANNEL 2
CONN-HDD1
R424 330R3
R149 330R3
R290 220R
R425 220R3
R148 4K7R3
R153 4K7R3
R150 5K6R3
R151 1KR3
R152 2K2R3
R147 2K2R3
R374 220R3
R402 10KR3
R403 10KR3
C88 SC47P
C89 SC47P
C86 SC47P
C87 SC47P
Q1 S2N3904
Q9 S2N3906
U40D SOF14
U40C SOF14
U22A S007
U22F S007
U22C S007
U22B S007
JP2 TR3P-6
1-2: LED FOR IDE & FDD
2-3: LED FOR IDE ONLY
ACER
V58LA
IDE CONNECTOR
Size A3
Document Number
REV -1
Date: May 20, 1997 Sheet 10 of 36

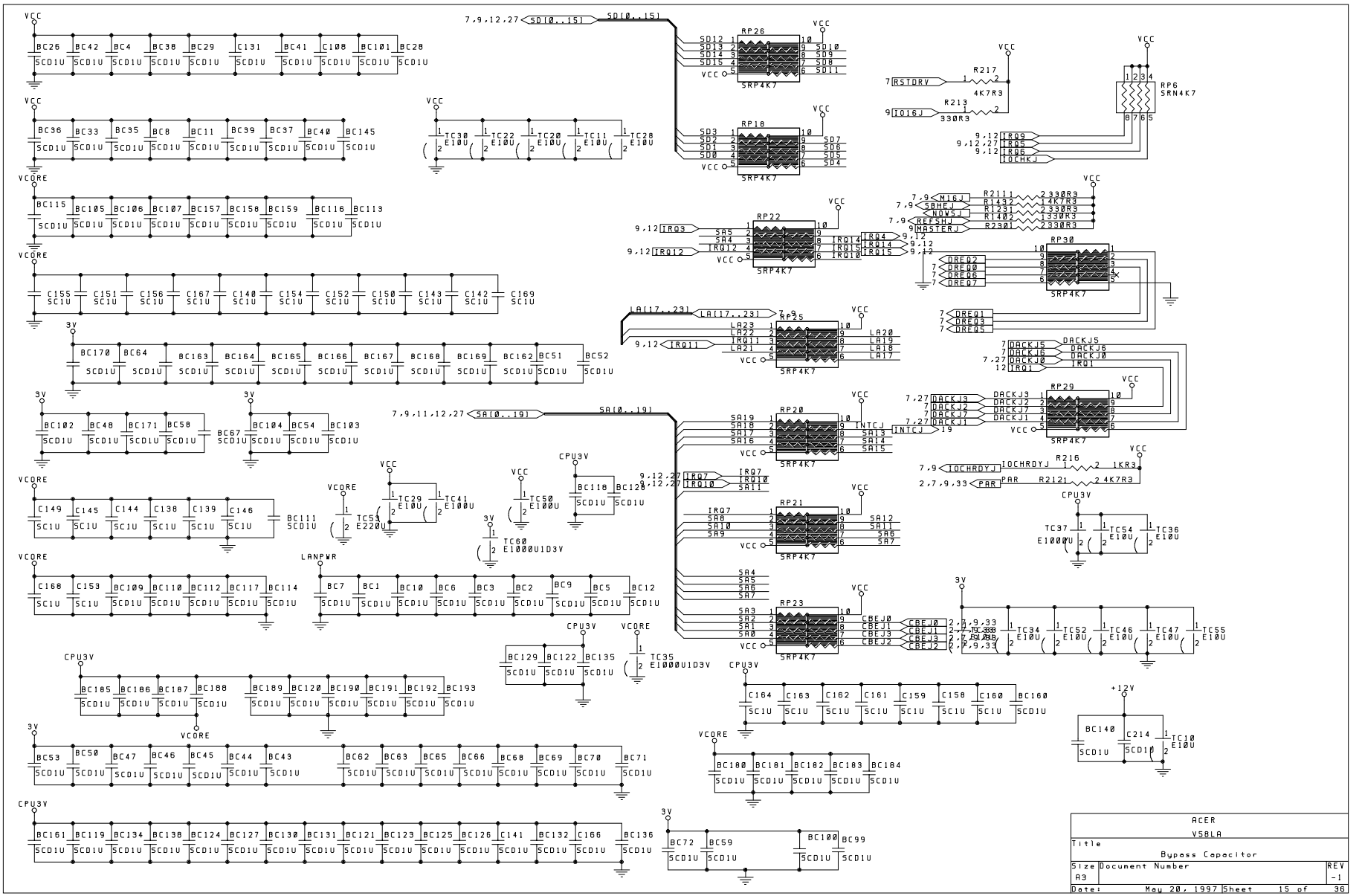

U23
D256K8-150
RP70
SRP10K
RP3
SRN10K
FA1 FUSE-3A32V
F1 FUSE-3A32V OPTION
L6 SCHOKE-B
CN2
PS/2 KB
CN3
PS/2 MOUSE
JP4
1R4P-1
1-2 12V FLASH ROM FOR MX 2MB
2-3 5V EPROM FOR SST,ATMEL
3-4 NORMAL OPERATION
CN34
CON4
CN35
1R3P-3
(RESET)
JP3
1R3P-6
JP4 :
1-2 : SUPPORT SMM-SW
2-3 : SUPPORT RESET-SW
U11A
U11B
U11C
SOLS14
SOLS32
JP1
1R3P-4
2-3 : OEM BIOS
1-2 : ACER BIOS
ACER
V58LA
EPROM K.B MOUSE SMI
Size A3
Document Number
REV -1
Date: May 20, 1997 Sheet 11 of 36

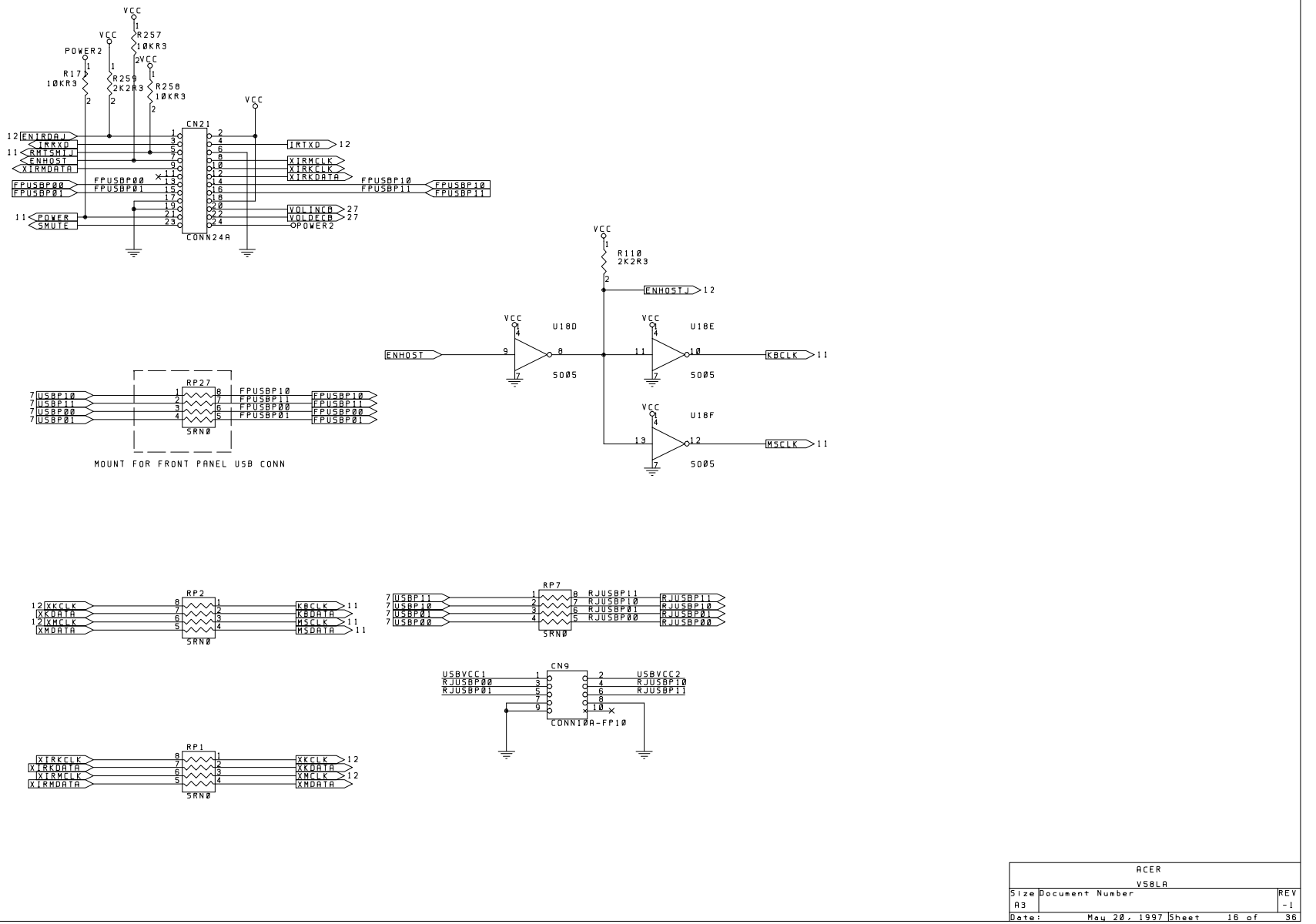

POWER2
BAT
Q3 S2N3906
Q4 S2N3904
R64 51KR5
R62 210KR3
R63 10KR3
TC9 E10U
C21 SC1U
C22 SCD1U
D25 F01J2E
D24 F01J2E
D19 1N60
D36 1N60
R65 1K5R3
BT1 CR2032
VBAT
MOUNT FOR SMC935 VER. D
R109 1MR3
MOUNT FOR M514X
XTAL1
XTAL2
R108 10MRB
X1 XTAL-32.768KHZ
C84 SC20P
C83 SC20P
MOUNT FOR M514X ONLY
R122 0R3
R23 0R3
MOUNT FOR M514X
R221 1MR3
C17 SC1U
C16 SCD1U
R57 4K7R3
JP17
R59 1K3R3
1R3P-6
1-2:USE SOFT SHUTDOWN POWER SUPPLY
2-3:USE TRADITIONAL POWER SUPPLY
U19
SOF244
R126 0R3
FOR SCI
R42 0R3
U20
FDC37C93
MOUNT FOR APM ONLY
R138 0R3
R134 0R3
R139 0R3
RP5 SRN1K
R119 1K3R3
CN12
CONN-FDD
RPM
R133 0R3
OSC24MHZ
OSC2
OSC-24MHZ
D26 1N5817
RA13 1K3R3
R121 5K6R3
R135 0R3
R58 0R3
MOUNT FOR S14X
R120 0R3
R137 0R3
R118 10KR3
R117 1K3R3
R114 10KR3
R113 1K3R3
R115 10KR3
R116 1K3R3
R112 10KR3
R111 1K3R3
UNMOUNT
CONF BASE ADDRESS
1: 0X370
0: 0X3F0
ACER
V58LA
Title
SMC935 & APM & M152X & M154X
Size A3
Document Number
REV -1
Date: May 20, 1997
Sheet 12 of 36


R173
SLCTINJ
1KR3
RP37
RP56
RP54
RP36
RP55
RP38
SRP1K
SRN22
CN7
CN18 : PRINTER PORT
CN6
CN4
CN5
U17
U16
75C185
RS232-9
FOX-CON9
R174
R175
R176
R177
0R3
MOUNT FOR ON BOARD USB CONN
SAME LOCATION WITH COM2
R181
560KR3
470KR3
R180
R178
R179
C124
C125
C109
C110
C111
C112
L18
L19
L21
L22
BLM41
RUE110
6V40A
GND1
GND2
+12V
-12V
VCC
ACER
VS8LA
PRINTER, COM PORT, USB CONN
A3
May 20, 1997
Sheet 13 of 36
REV -1

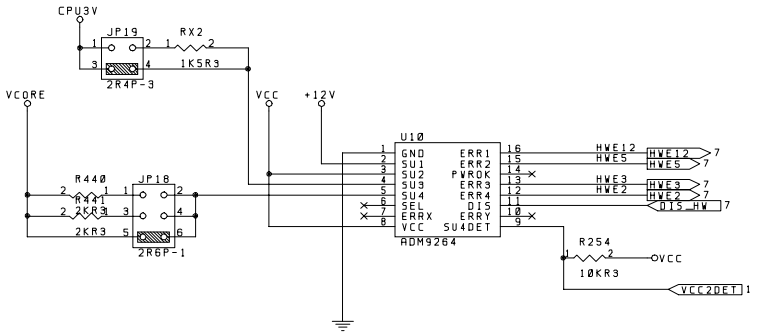


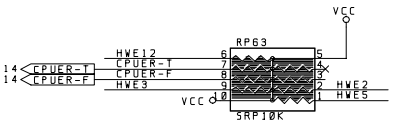
ACER		
VS8LA		
Title		
POWER REGULATOR		
Size: A3	Document Number	REV: -1
Date: May 20, 1997	Sheet 14 of	36


ACER
V58LA
Title
Bypass Capacitor
Size A3
Document Number
REV -1
Date: May 20, 1997 Sheet 15 of 36



ACER		
V58LA		
Size: A3	Document Number	REV: -1
Date: May 20, 1997	Sheet 16 of 36	





1-2: Hardware Monitoring support VCORE 3.2V

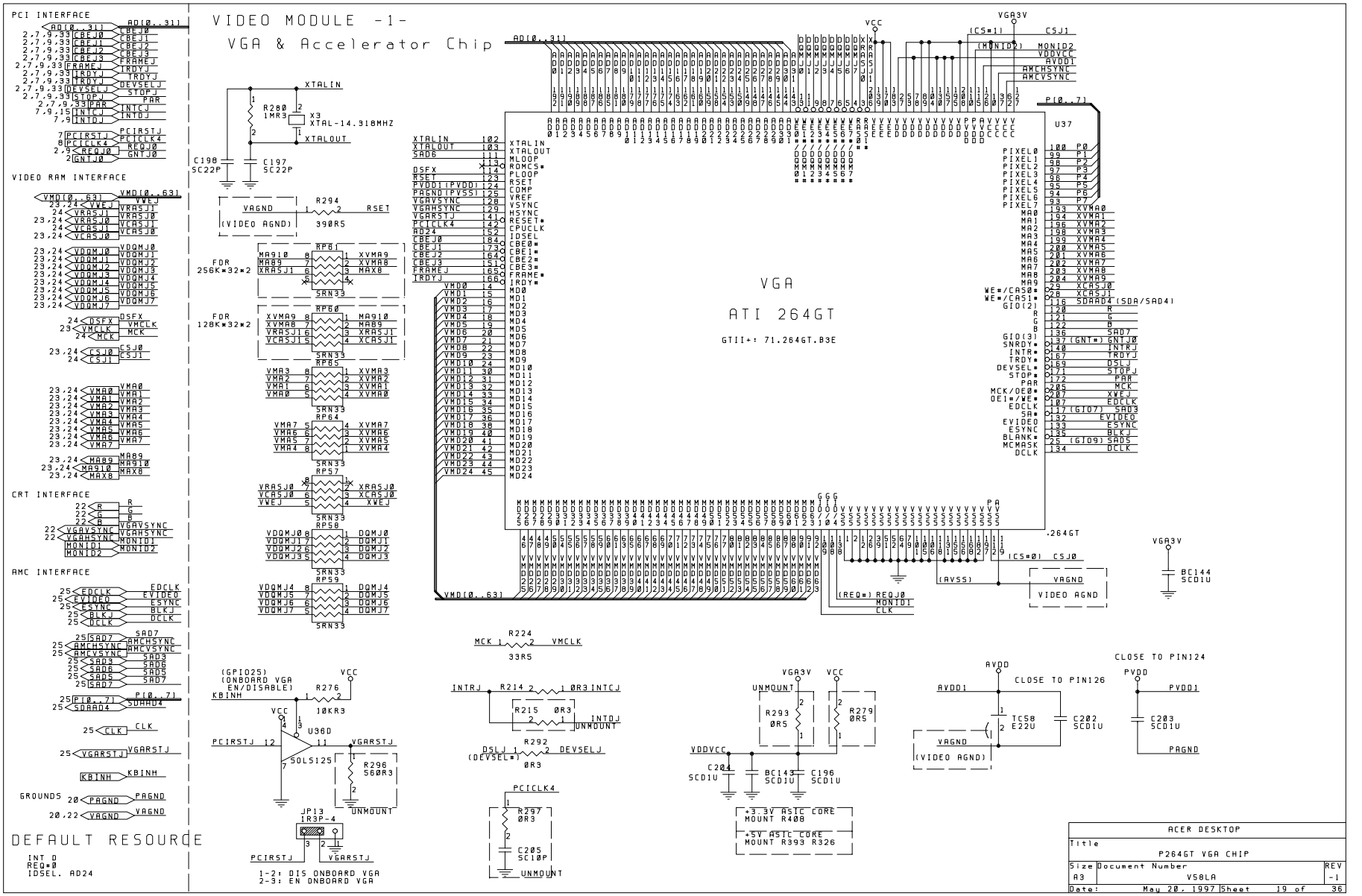
2-3: Hardware Monitoring support VCORE 2.8V (Default)

ACER		
V58LA		
Title: H/W MONITOR		
Size: A3	Document Number	REV: -1
Date: May 20, 1997	Sheet 17 of 36	

VEDIO MODULE

19. VGA CHIP: ATI P264GT
20. REFERENCE
21. VGA CHIP BYPASS, HARDWARE SETTING
22. CRT CONNECTOR
23. SGRAM
24. SGRAM EXTENSION CONNECTOR
25. AMC CONNECTOR

ACER DESKTOP		
Title: VEDIO COVERSHEET		
Size: A3	Document Number: V58LA	REV: 5A
Date: December 16, 1996	Sheet 18 of 36	


VIDEO MODULE -1-
VGA & Accelerator Chip
PCI INTERFACE
VIDEO RAM INTERFACE
CRT INTERFACE
AMC INTERFACE
GROUNDS
DEFAULT RESOURCE
INT D
REQ#0
IDSEL. AD24
VGA
ATI 264GT
GTII+: 71.264GT.B3E
.264GT
U37
U36D
50LS125
JP13
1-2: DIS ONBOARD VGA
2-3: EN ONBOARD VGA
+3.3V ASIC CORE
MOUNT R408
+5V ASIC CORE
MOUNT R393 R326
CLOSE TO PIN126
CLOSE TO PIN124
ACER DESKTOP
P264GT VGA CHIP
V58LA
May 20, 1997
19 of 36

VIDOE MODULE - 2 -
Power Distribution

VCC: DIGITAL 5V FROM POWER SUPPLY
3V: DIGITAL 3.3V FROM SYSTEM REGULATOR
+12V: DIGITAL 12V FROM POWER SUPPLY
PVDD: ANALOG 5V TO PLL
AVDD: ANALOG 5V TO VIDEO
PAGND: PLL ANALOG GROUND
VAGND: VIDEO ANALOG GROUND

VIDEO AGND
19,22 VAGND VAGND

PLL VIDEO
19 PAGND PAGND

(3.3V FROM REG/SYSTEM) (POWER OUTPUT)
VGA3V L16 5CHOKE-B UNMOUNT AVDD (ANALOG 5V FOR B+)
VCC L17 5CHOKE-B UNMOUNT (5V FROM SYSTEM)

VCC
VGA3V U35 ADJ/GND OUT IN EZ1085CM-3
TC49 E100U TC57 E100U

AVDD R295 PVDD 0R5

R298 PAGND 0R3

R300 VAGND 0R3

(CLEAN 5V FOR B+)
(PLL POWER)
U39 NJM78M05DLA-I GND IN OUT

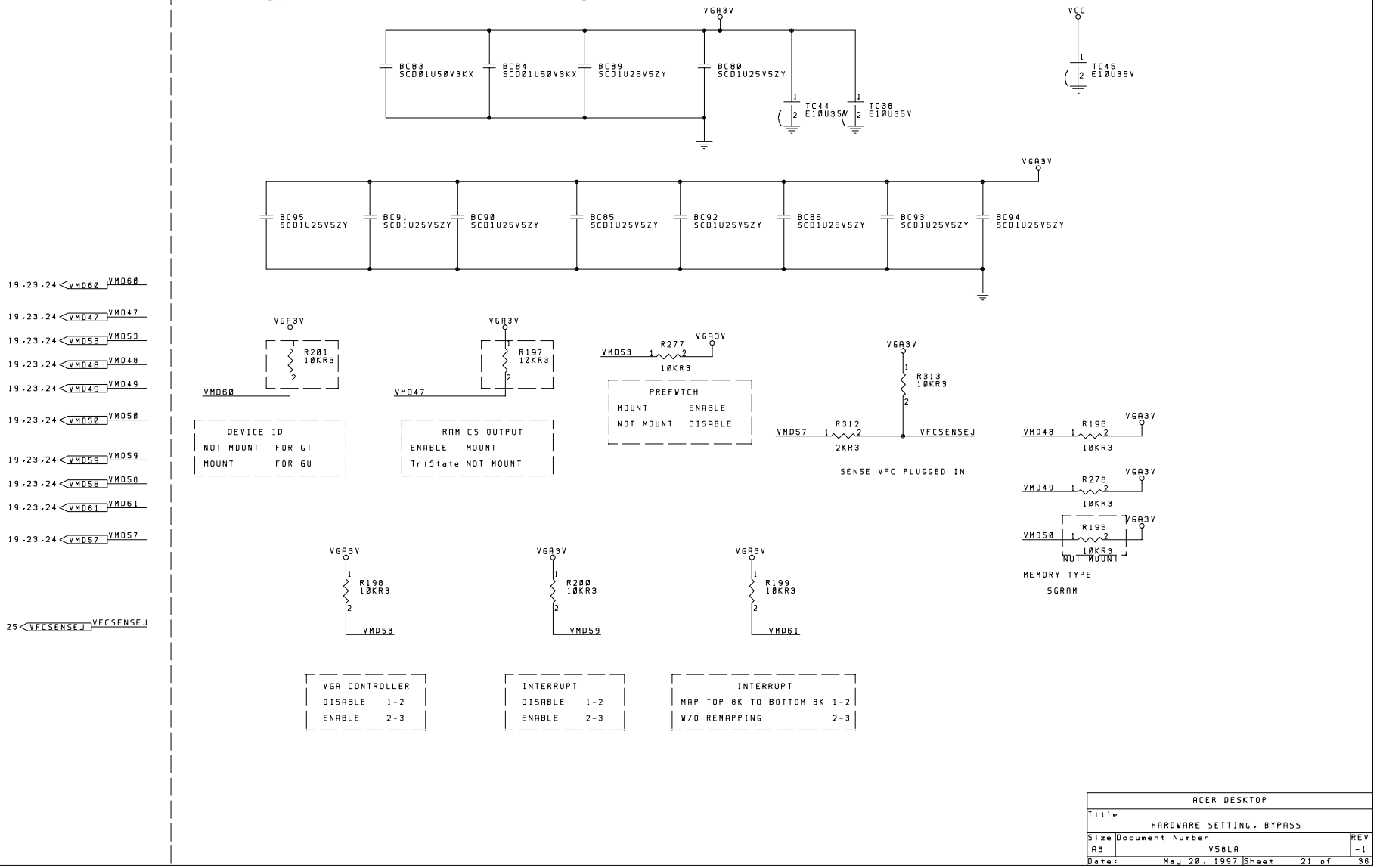
OPTION 5B
+12V C207 5CD01U
PVDD C212 5CD01U TC59 E10U PAGND
(RECOMMENDATED)

OPTION 5A
UNMOUNT
PVDD R299 0R3 VCC
(5V FROM SYSTEM)
(DIGITAL POWER)

ACER DESKTOP		
Title: Power and Ground		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 20 of 36	

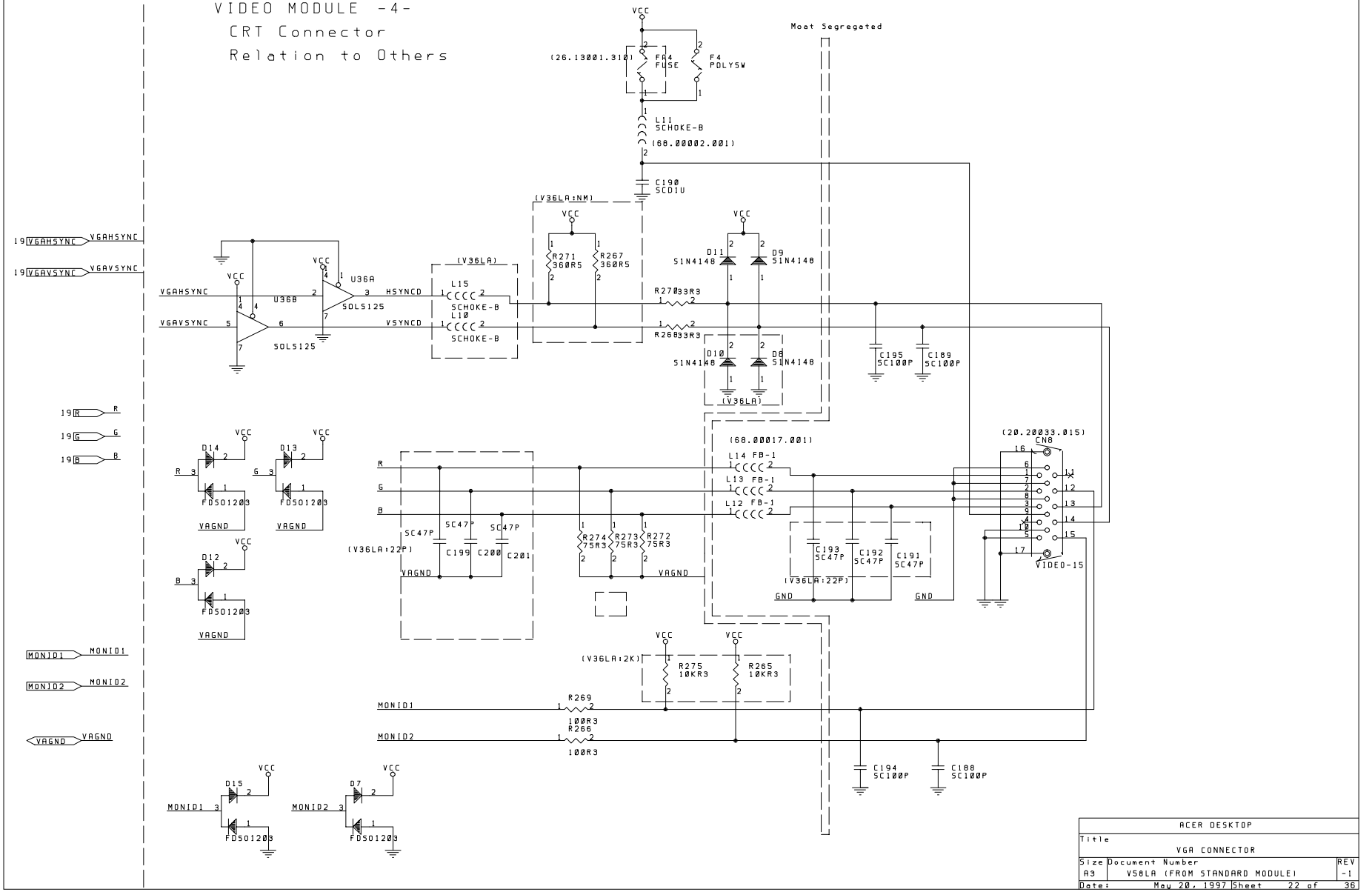
VIDEO MODULE -3-

VGA Bypass and Hardware setting

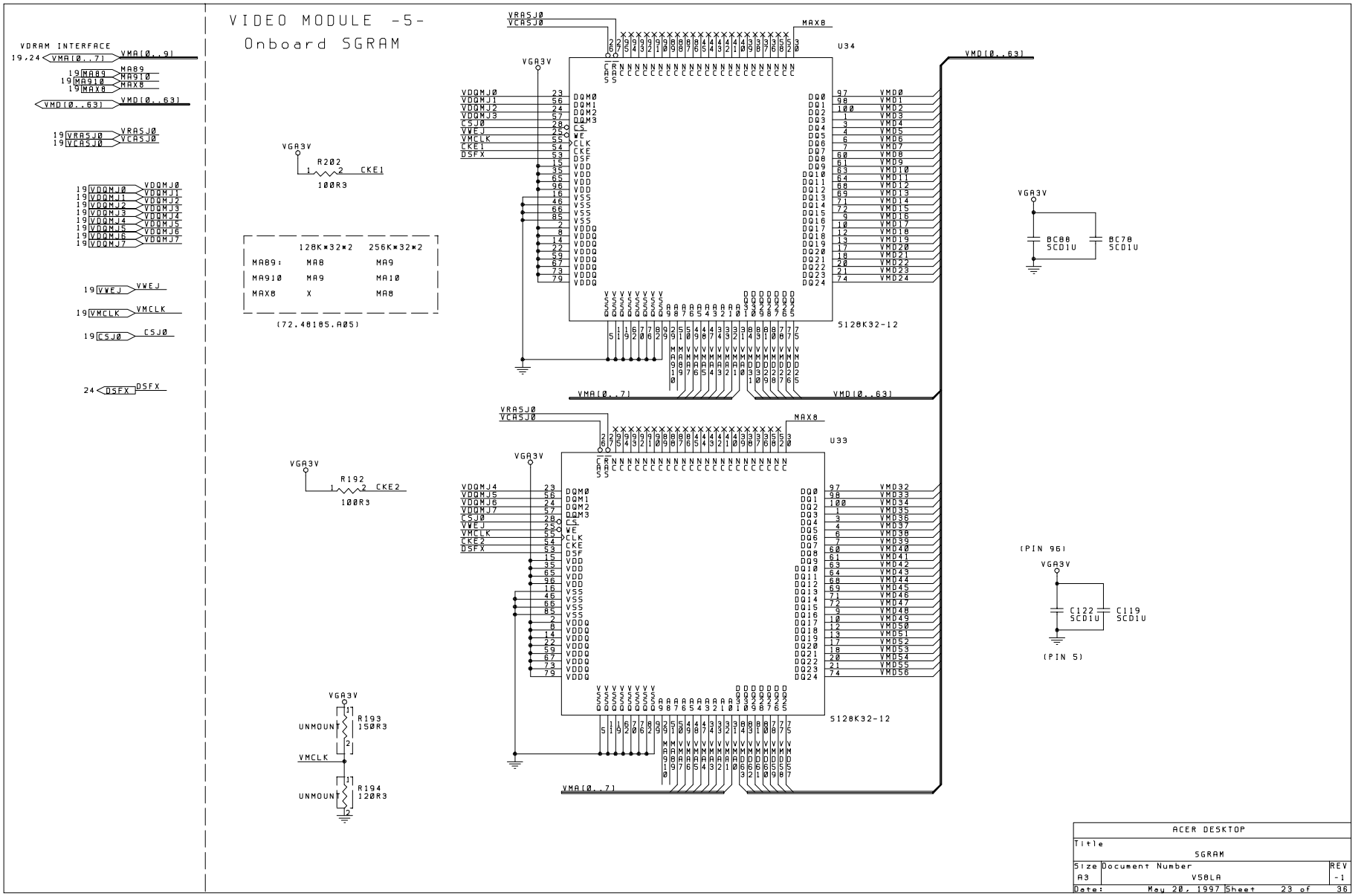


ACER DESKTOP		
Title: HARDWARE SETTING, BYPASS		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 21 of 36	

VIDEO MODULE -4-
CRT Connector
Relation to Others

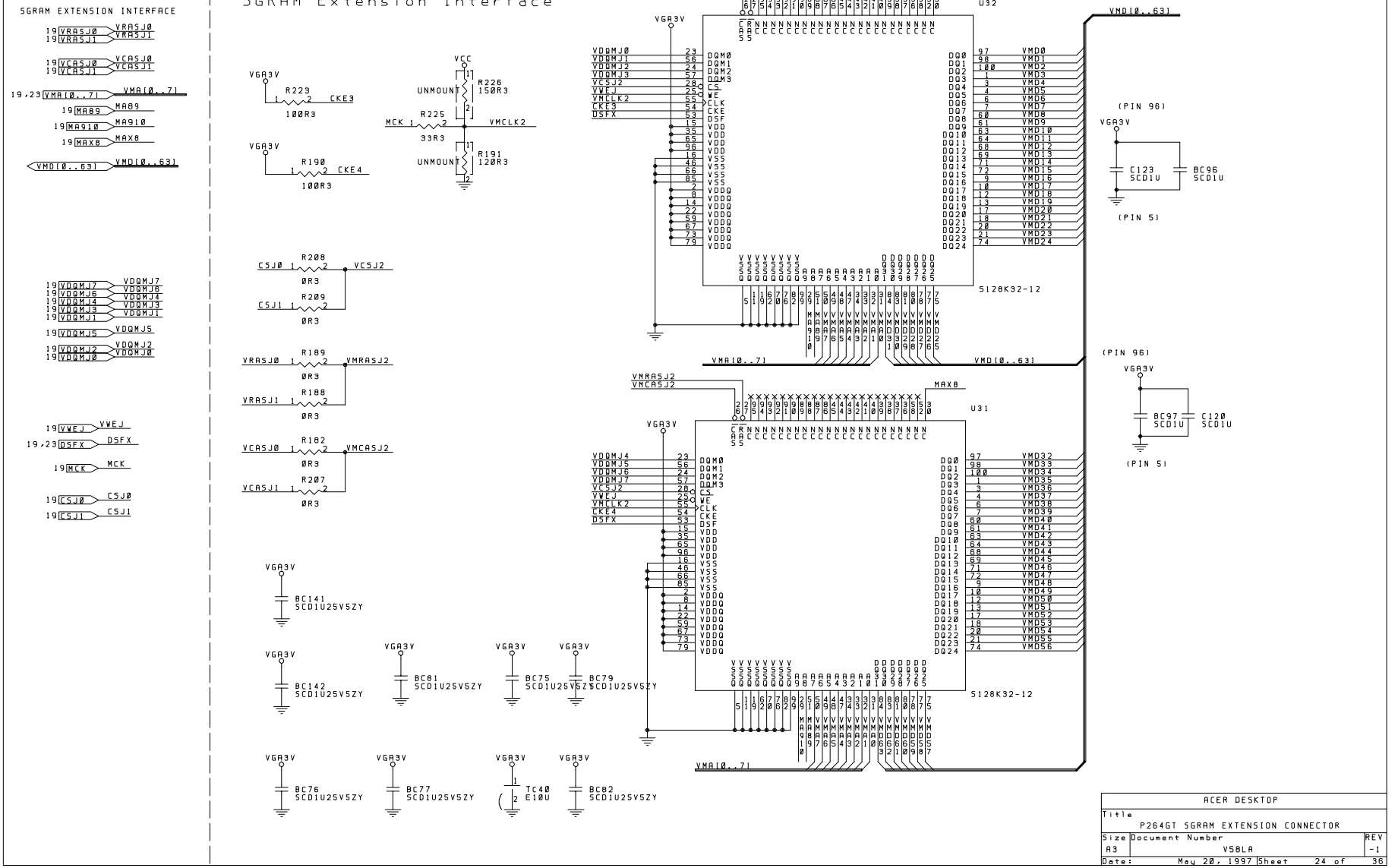


ACER DESKTOP		
Title: VGA CONNECTOR		
Size: A3	Document Number: V50LA (FROM STANDARD MODULE)	REV: -1
Date: May 20, 1997	Sheet 22 of 36	


VIDEO MODULE -5-
Onboard SGRAM
VDRAM INTERFACE
VMA[0..9]
VMD[0..63]
VRASJ0
VCASJ0
VDQMJ0
VDQMJ1
VDQMJ2
VDQMJ3
VDQMJ4
VDQMJ5
VDQMJ6
VDQMJ7
VWEJ
VMCLK
CSJ0
DSFX
MA89
MA910
MAX8
VGA3V
R202
100R3
CKE1
R192
CKE2
R193
150R3
R194
120R3
UNMOUN
128K*32*2
256K*32*2
MA89: MA8 MA9
MA910 MA9 MA10
MAX8 X MA8
(72,48185,A05)
U34
U33
5128K32-12
BC88
SCD1U
BC78
SCD1U
C122
SCD1U
C119
SCD1U
(PIN 96)
(PIN 5)
ACER DESKTOP
Title
SGRAM
Size
A3
Document Number
VS8LA
REV
-1
Date: May 20, 1997 Sheet 23 of 36

VIDEO MODULE -6-

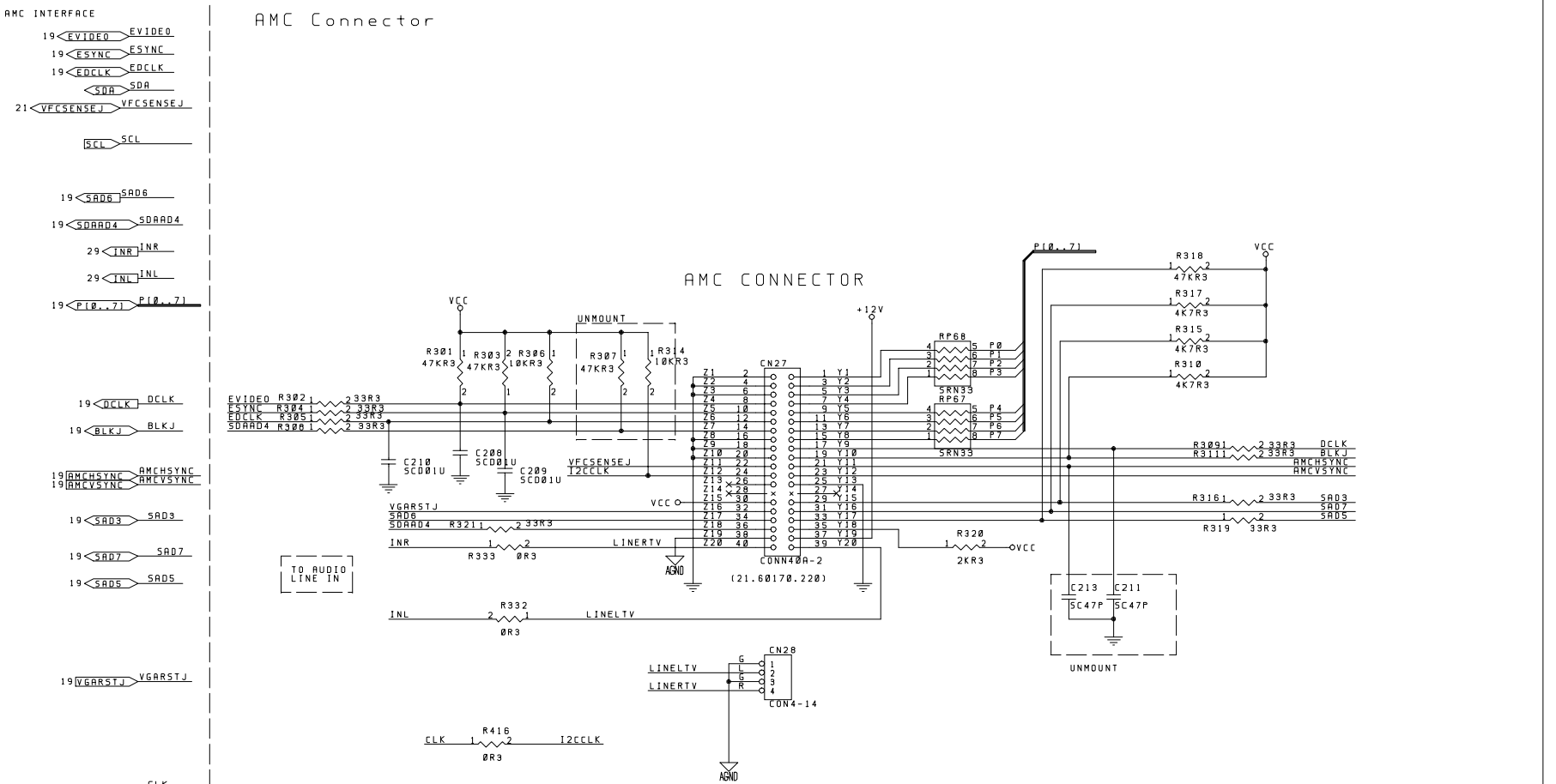
SGRAM Extension Interface



ACER DESKTOP		
Title: P264GT SGRAM EXTENSION CONNECTOR		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 24 of 36	

VIDEO MODULE -7-

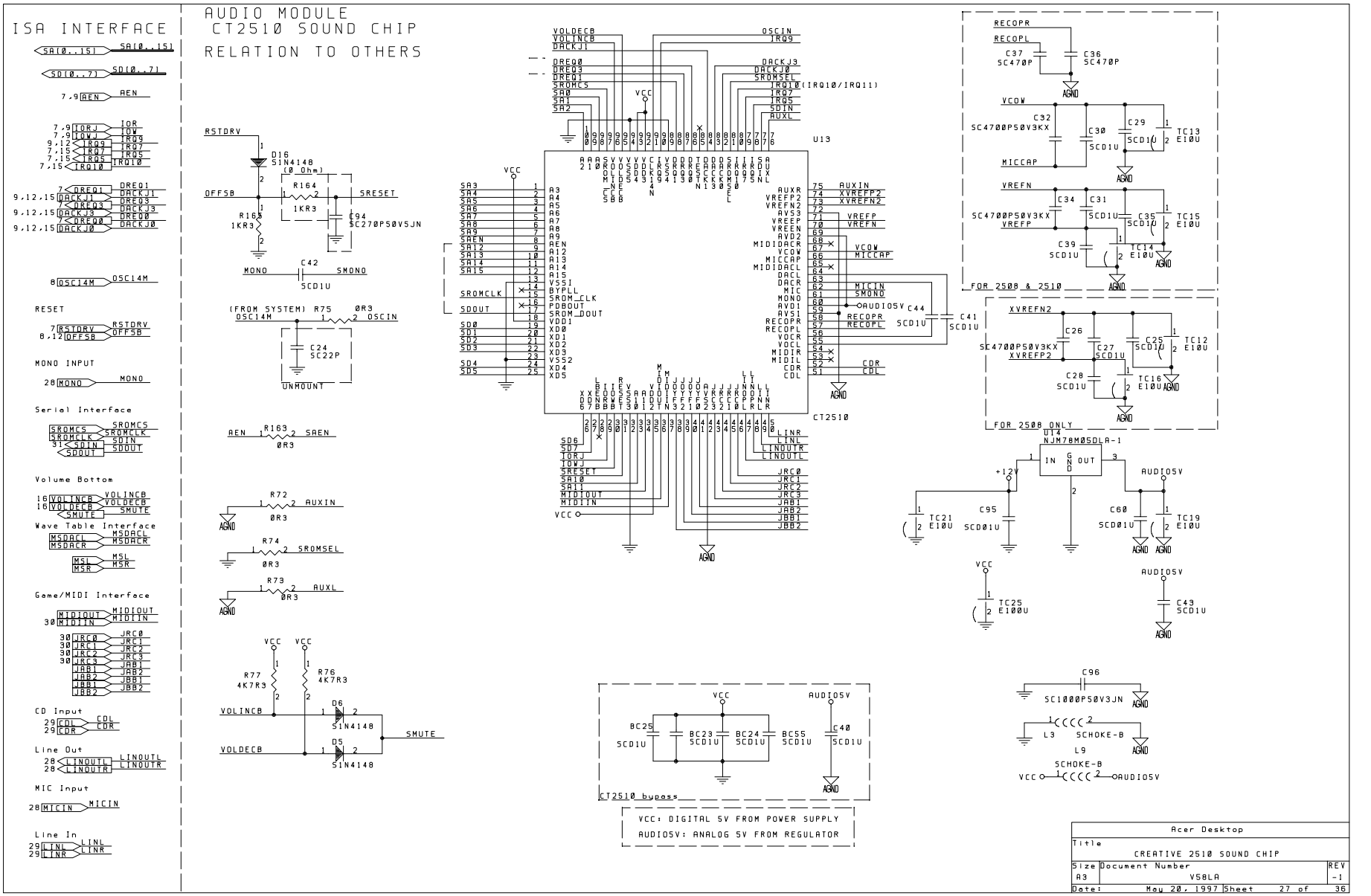
AMC Connector

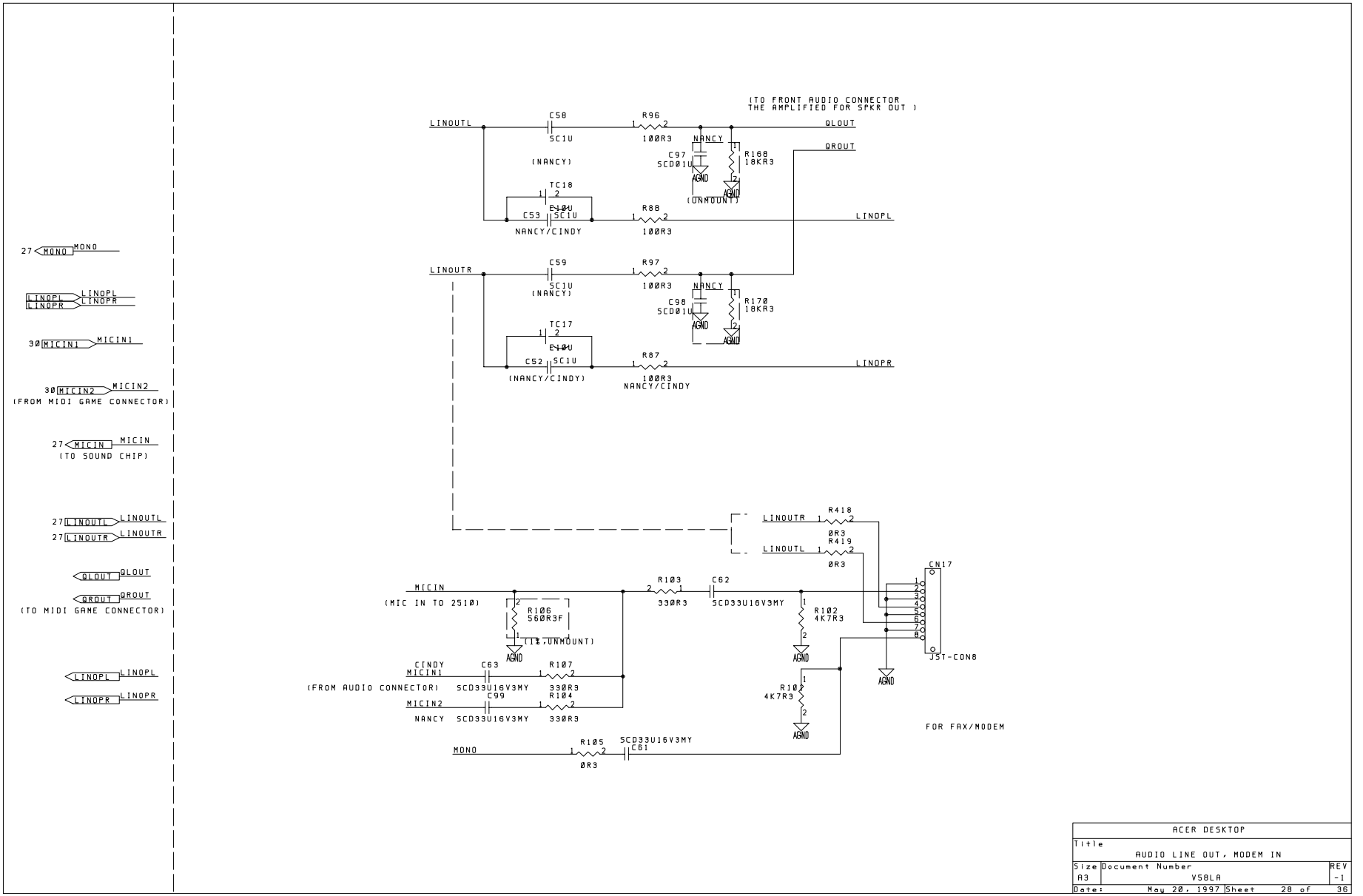


AUDIO MODULE

27. CREATIVE 2510 SOUND CHIP
28. AUDIO OUT
29. AUDIO INPUT
30. MIDI/GAME CONNECTOR, WAVE TABLE CONNECTOR
31. AUDIO MISCELL

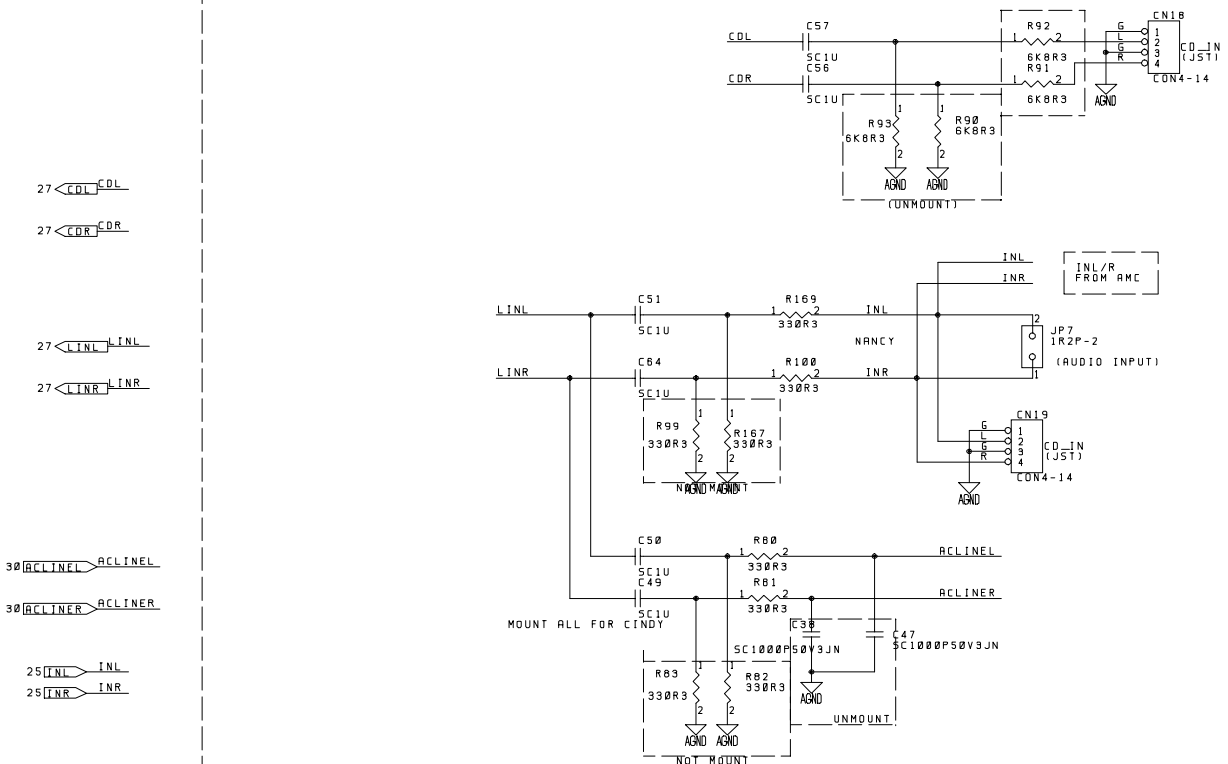
ACER DESKTOP		
Title: AUDIO COVERSHEET		
Size: A3	Document Number: V58LA	REV: 5A
Date: November 28, 1996	Sheet 26 of 36	


ISA INTERFACE
AUDIO MODULE
CT2510 SOUND CHIP
RELATION TO OTHERS
SA[0..15]
SD[0..7]
AEN
IOR
IOW
IRQ9
IRQ7
IRQ5
IRQ10
DREQ1
DACKJ1
DREQ3
DACKJ3
DREQ0
DACKJ0
OSC14M
RESET
RSTDRV
OFF5B
MONO INPUT
MONO
Serial Interface
SROMCS
SROMCLK
SDIN
SDOUT
Volume Bottom
VOLINCB
VOLDECB
SMUTE
Wave Table Interface
MSDACL
MSDACR
MSL
MSR
Game/MIDI Interface
MIDIOUT
MIDIIN
JRC0
JRC1
JRC2
JRC3
JAB1
JAB2
JBB1
JBB2
CD Input
CDL
CDR
Line Out
LINOUTL
LINOUTR
MIC Input
MICIN
Line In
LINL
LINR
D16
S1N4148
(0 Ohm)
R164
1KR3
R165
1KR3
C94
SC270P50V5JN
C42
5CD1U
(FROM SYSTEM) R75
0R3
C24
SC22P
UNMOUNT
R163
0R3
R72
0R3
R74
0R3
R73
0R3
R77
4K7R3
R76
4K7R3
D6
D5
U13
CT2510
C44
C41
SCD1U
FOR 2508 & 2510
C36
SC470P
C37
5C470P
C32
SC4700P50V3KX
C30
C29
TC13
E10U
C34
C31
C35
TC15
C39
TC14
C26
C27
C25
TC12
C28
TC16
FOR 2508 ONLY
U14
NJM78M05DLA-1
+12V
C95
C60
TC21
TC19
TC25
C43
C96
SC1000P50V3JN
L3
L9
SCHOKE-B
BC25
BC23
BC24
BC55
C40
CT2510 bypass
VCC: DIGITAL 5V FROM POWER SUPPLY
AUDIO5V: ANALOG 5V FROM REGULATOR
Acer Desktop
Title
CREATIVE 2510 SOUND CHIP
Size
A3
Document Number
V58LA
REV
-1
Date: May 20, 1997
Sheet 27 of 36



ACER DESKTOP		
Title: AUDIO LINE OUT, MODEM IN		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 28 of 36	

AUDIO MODULE
INPUT I/O Connector



Acer Desktop		
Title: CD IN, LINE IN		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 29 of 36	

SOUND MODULE

Audio Connector

MIDI/JOYSTICK INTERFACE

28 MICIN2

COMMON

27 MIDIIN

MIDIOUT

SPROUT SPLOUT

JAB1 JAB2 JBB1 JBB2

JACXA JACYA JBCXA JBCYA

AUDIO INTERFACE

28 MICIN1

29 ACLINER ACLINEL

LINOPL

LINOPR

27 JRC0 JRC1 JRC2 JRC3

PSUP

WAVE TABLE INTERFACE

EMUR EMUL

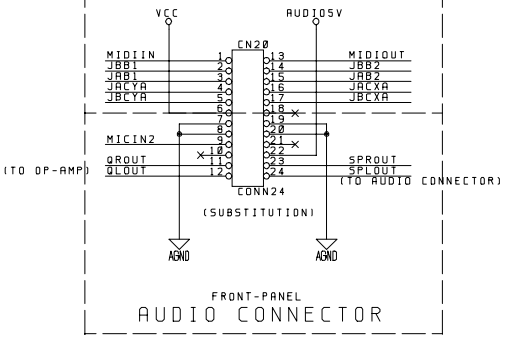
MSL

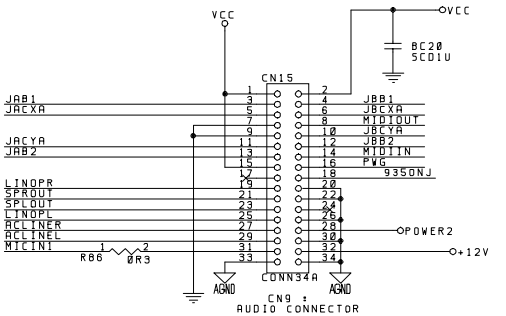
MSR

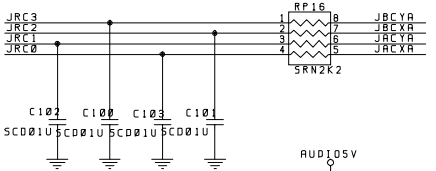
MSDACL

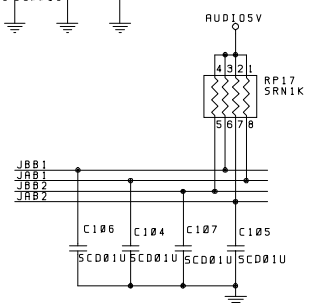
MSDACR

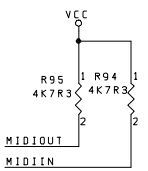
MIDI GAME CONNECTOR





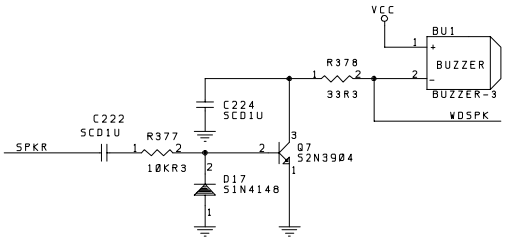






ACER DESKTOP		
Title: MIDI CONNECTOR, WAVE TABLE CONNECTOR		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 30 of 36	

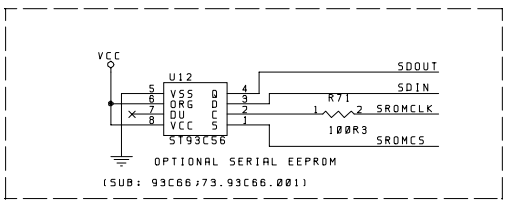
FUNCTION MODULE
Sound I/O Connector



7 SPKR SPKR

11 WDSPK WDSPK

SPKRIN SPKRIN



SDOUT SDOUT

27 SDIN SDIN

SROMCLK SROMCLK

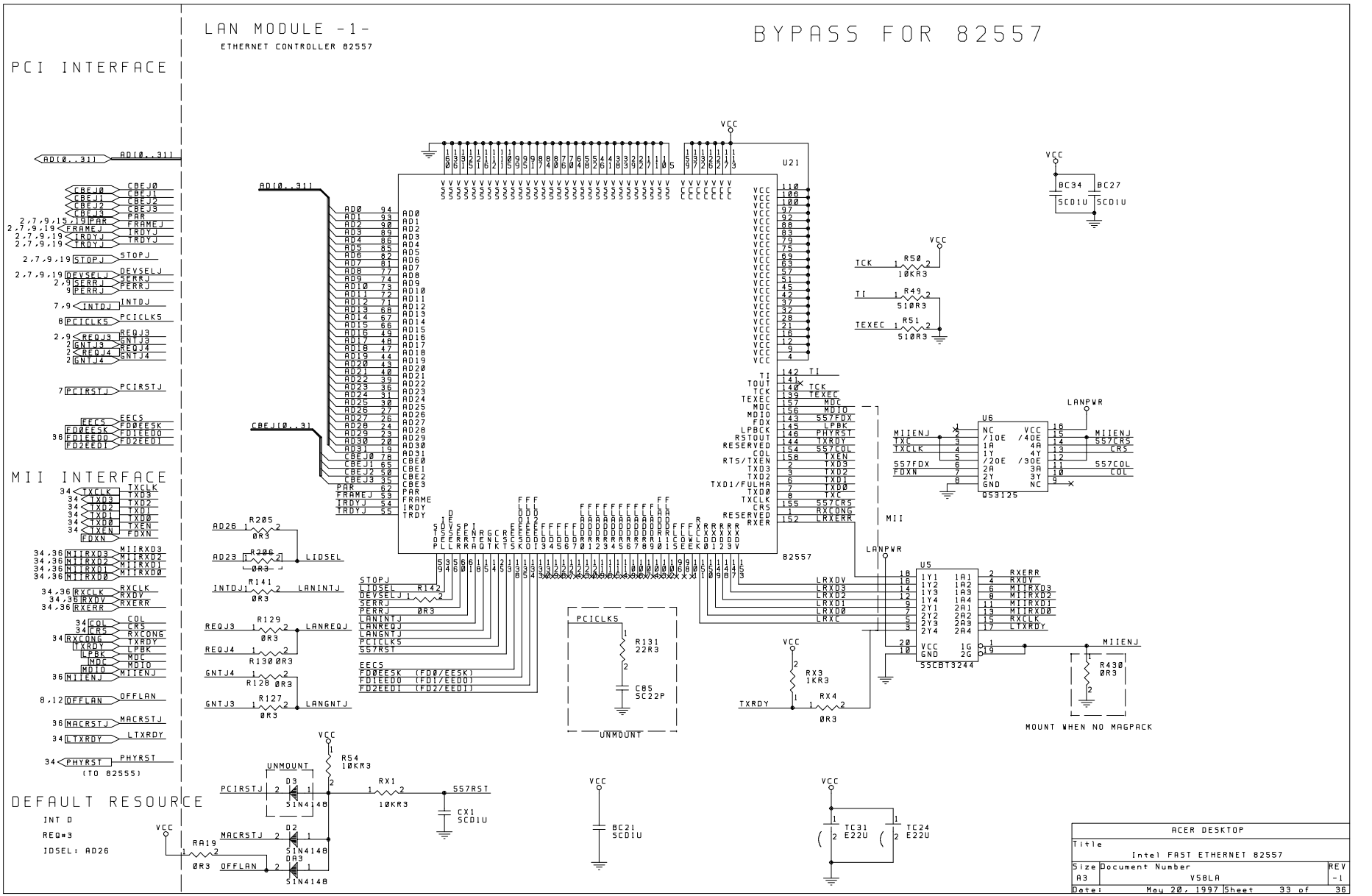
SROMCS SROMCS

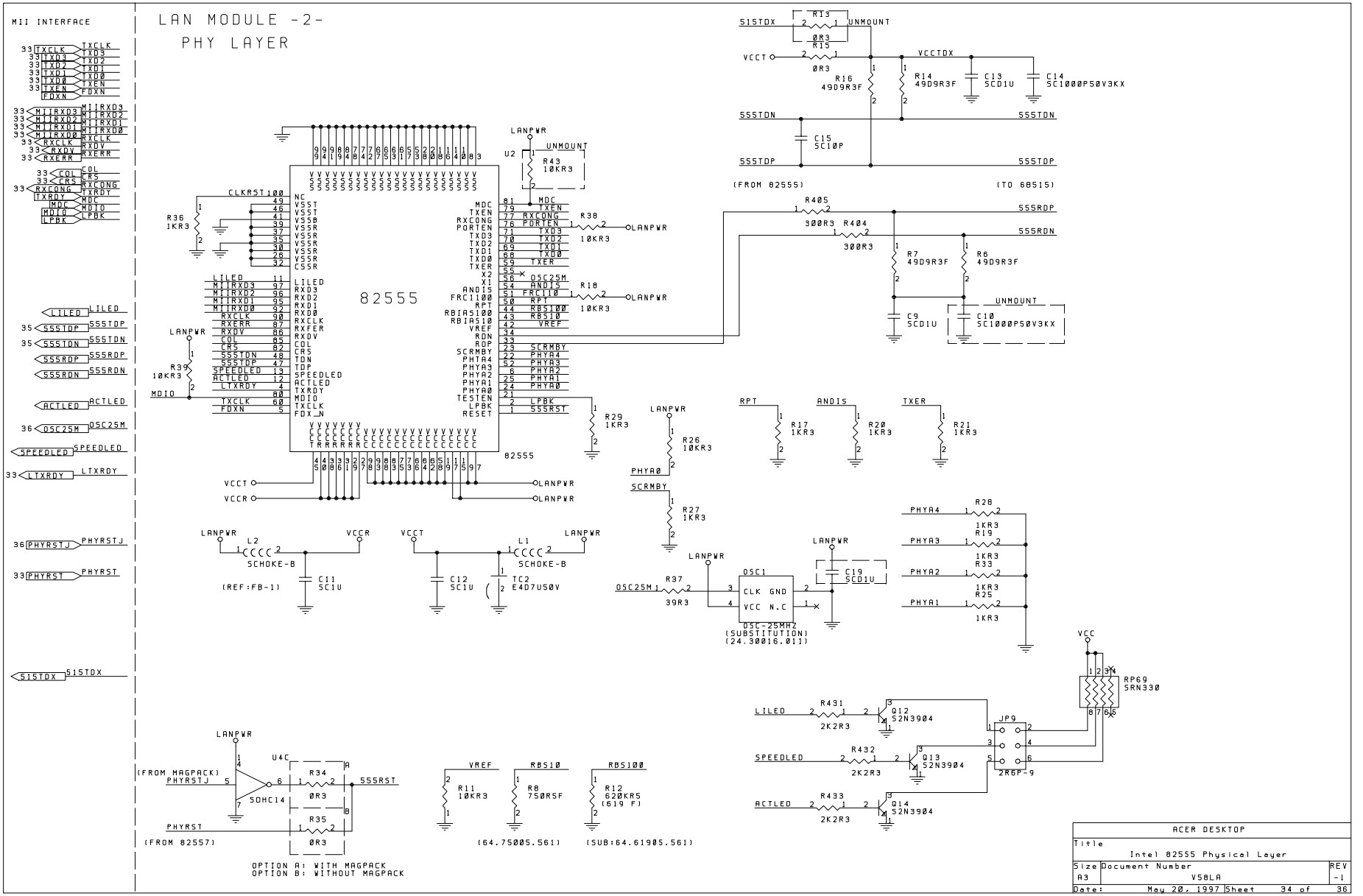
Acer Desktop		
Title: SPKR, EEPROM, DMA		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 31 of 36	

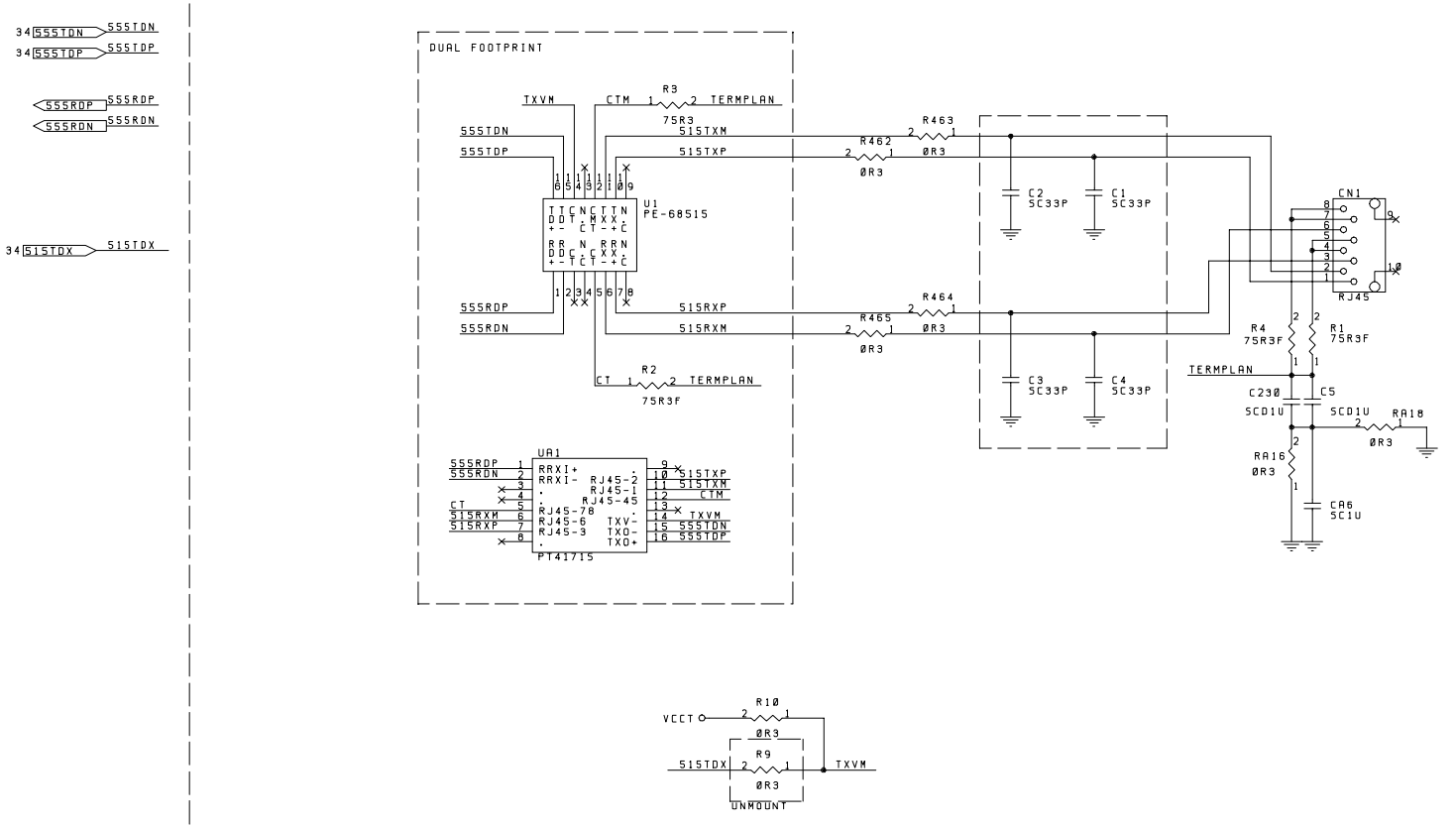
LAN MODULE

33. FAST ETHERNET 82557 CONTROLLER
34. LAN PD83840
35. 83223, 4171

ACER DESKTOP		
Title: LAN COVERSHEET		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 32 of 36	


LAN MODULE -1-
ETHERNET CONTROLLER 82557
BYPASS FOR 82557
PCI INTERFACE
MII INTERFACE
DEFAULT RESOURCE
INT D
REQ#3
IDSEL: AD26
(TO 82555)
U21
B2557
U6
QS3125
U5
SSCBT3244
MII
LANPWR
VCC
UNMOUNT
MOUNT WHEN NO MAGPACK
ACER DESKTOP
Title
Intel FAST ETHERNET 82557
Size A3
Document Number V58LA
REV -1
Date: May 20, 1997
Sheet 33 of 36

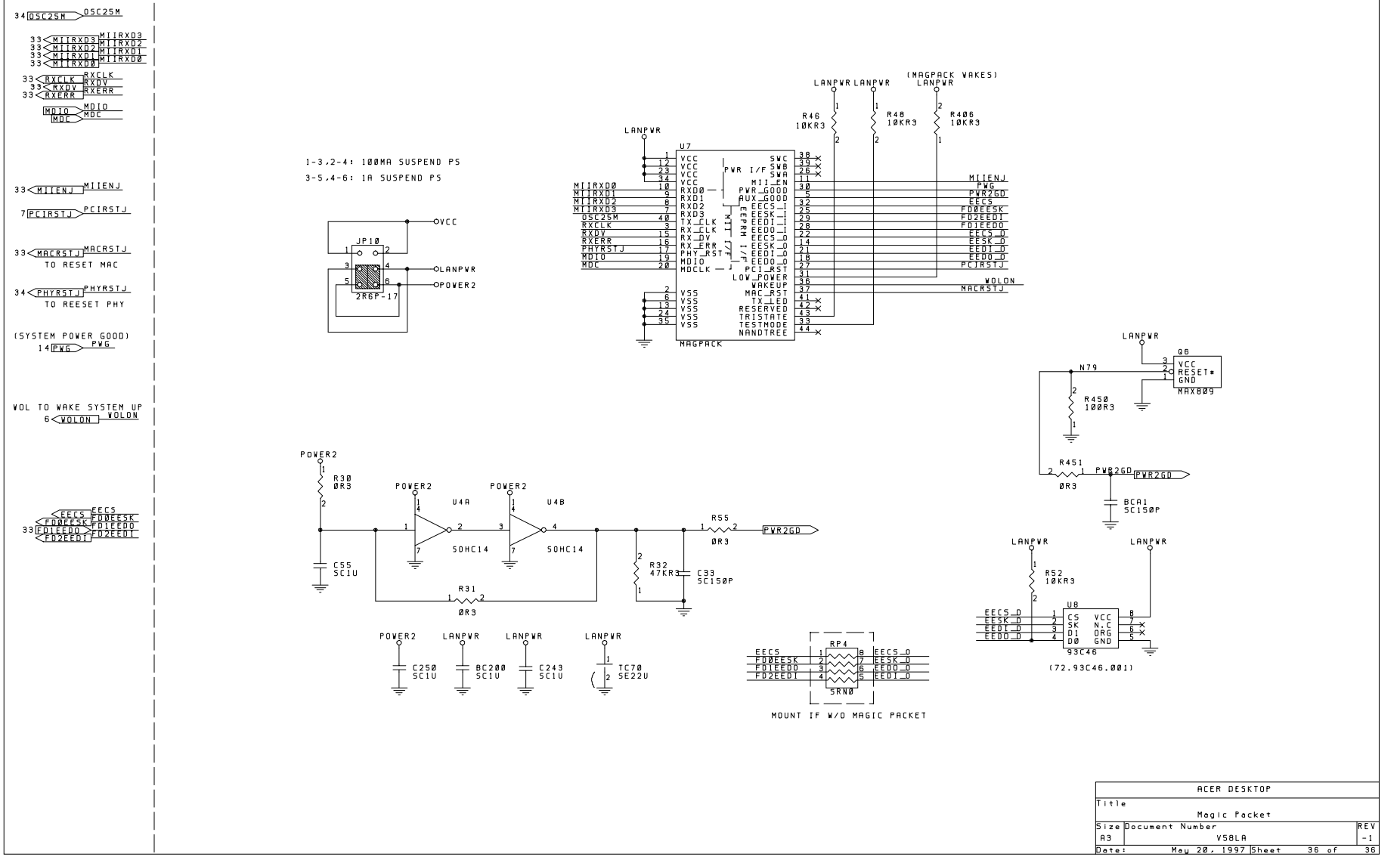

LAN MODULE -2-
PHY LAYER
MII INTERFACE
82555
U2
LANPWR
UNMOUNT
R43 10KR3
R36 1KR3
R38 10KR3
R18 10KR3
R39 10KR3
R29 1KR3
R26 10KR3
R27 1KR3
R17 1KR3
R20 1KR3
R21 1KR3
R28 1KR3
R19 1KR3
R33 1KR3
R25 1KR3
R405 300R3
R404 300R3
R7 49D9R3F
R6 49D9R3F
C9 SCD1U
C10 SC1000P50V3KX
515TDX
R13 0R3
R15 0R3
VCCT
VCCTDX
R16 49D9R3F
R14 49D9R3F
C13 SCD1U
C14 SC1000P50V3KX
555TDN
C15 SC10P
555TDP
(FROM 82555)
(TO 68515)
555RDP
555RDN
L2 SCHOKE-B
L1 SCHOKE-B
(REF:FB-1)
C11 SC1U
C12 SC1U
TC2 E4D7U50V
VCCR
OSC1
CLK GND
VCC N.C
R37 39R3
C19 SCD1U
OSC-25MHZ
(SUBSTITUTION)
(24.30016.011)
RP69 SRN330
R431 2K2R3
R432 2K2R3
R433 2K2R3
Q12 S2N3904
Q13 S2N3904
Q14 S2N3904
JP9
2R6P-9
U4C
SOHC14
R34 0R3
R35 0R3
(FROM MAGPACK)
(FROM 82557)
555SRST
OPTION A: WITH MAGPACK
OPTION B: WITHOUT MAGPACK
R11 10KR3
R8 750R5F
R12 620KR5 (619 F)
(64.75005.561)
(SUB:64.61905.561)
ACER DESKTOP
Intel 82555 Physical Layer
Size A3
Document Number V58LA
REV -1
Date: May 20, 1997
Sheet 34 of 36



ACER DESKTOP		
Title: LAN PHY AND RJ PHONE JACK		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 35 of 36	

LAN MODULE -4-

Magic Packet



ACER DESKTOP		
Title: Magic Packet		
Size: A3	Document Number: V58LA	REV: -1
Date: May 20, 1997	Sheet 36 of 36	

BIOS POST Check Points

D.1. Power-On Self-Test (POST)

The Power-On Self Test (POST) is a BIOS procedure that boots the system, initializes and diagnoses the system components, and controls the operation of the power-on password option. If POST discovers errors in system operations at power-on, it displays error messages, generates a check point code at port 80h or even halts the system if the error is fatal.

The main components on the system board that must be diagnosed and/or initialized by POST to ensure system functionality are as follows:

- Microprocessor with built-in numeric coprocessor and cache memory subsystem
- Direct memory access (DMA) controller (8237 module)
- Interrupt system (8259 module)
- Three programmable timers (system timer and 8254 module)
- ROM subsystem
- RAM subsystem
- CMOS RAM subsystem and real time clock/calendar with battery backup
- Onboard serial interface controller
- Onboard parallel interface controller
- Embedded hard disk interface and one diskette drive interface
- Keyboard and auxiliary device controllers
- I/O ports
  - two RS232 serial ports
  - one parallel port
  - one PS/2-compatible mouse port
  - one PS/2-compatible keyboard port

D.1.1 Post Check Points

When POST executes a task, it uses a series of preset numbers called check points to be latched at port 80h, indicating the stages it is currently running. This latch can be read and shown on a debug board.

Table D-1 describes the Acer common tasks carried out by POST. A unique check point number represents each task.

Table D-1 POST Check Points

Check Point	Descriptions
04H	• Determines if the current booting procedure is from cold boot (press reset button or turn the system on), from warm boot (press CTRL + ALT + ESC) or from exiting BIOS setup. *Note: At the beginning of POST, port 64 bit 2 (8042 system flag) is read to determine whether this POST is caused by a cold or warm boot. If it is a cold boot, a complete POST is performed. If it is a warm boot, the chip initialization and memory test is eliminated from the POST routine.*
08H	• Disables Non-Maskable Interrupt (NMI), Alarm Interrupt Enable (AIE), Periodical Interrupt Enable (PIE), and Update-ended Interrupt Enable (UIE). *Note: These interrupts are disabled in order to avoid any mis-action happened during the POST routine.*
09H, 0AH	• Initializes Chipset point (I)
10H	• DMA controller (8237) test and initialization
14H	• System timer (8254) test and initialization
18H	• Memory refresh test; refresh occurrence verification (IRQ0)
1CH	• Verifies CMOS shutdown byte, battery and check sum *Note: Several parts of the POST routine require the system to be in protected mode. When returning to real mode from protected mode, the processor is reset, therefore POST is re-entered. In order to prevent re-initialization of the system, POST reads the shutdown code stored in location 0Fh in CMOS RAM. Then it jumps around the initialization procedure to the appropriate entry point.* *The CMOS shutdown byte verification assures that CMOS 0Fh area is fine to execute POST properly.* • Initializes CMOS default setting • Initializes RTC time base *Note: The RTC has an embedded oscillator that generates 32.768 KHz frequency. To initial RTC time base, turn on this oscillator and set a divisor to 32768 so that RTC can count time correctly.*
1DH	• Searches DRAM existence on each DRAM slot

Table D-1 POST Check Points

Check Point	Descriptions
1Eh	• DRAM type determination
2CH	• Tests 128K base memory *Note: The 128K base memory area is tested for POST execution. The remaining memory area is tested later.*
20H	• Tests keyboard controller (8041/8042) • Determines keyboard type (AT, XT, PS/2)
24H	• Tests programmable interrupt controller (8259) • Initializes system interrupt
30H	• System shadow RAM
34H	• DRAM sizing
3CH	• Sets interrupt service for POST
3FH	• Enables/Disables USB host controller
4BH	• Checks CPU brand, ID
4CH	• Checks CPU external frequency
35H	• PCI pass 0
40H	• Initializes PCI (1)
41H	• Initializes PCI (2)
42H	• Initializes PCI (3)
44H	• Initializes PCI (4)
45H	• Initializes PCI (5)
4EH	• Scans PnP devices
4FH	• Configures PnP devices
50H	• Initializes video display *Note: If system has any display card, it should be initialized via its I/O ROM or corresponding initialization program.*
54h	• Processes VGA shadow region
58H	• Displays Acer (or OEM) logo (if necessary) • Displays Acer copyright message (if necessary) • Displays BIOS serial number
59H	• Hooks INT 1CH for Quiet Boot
5CH	• Memory test (except the 128K base memory)
5AH	• Tests SM RAM

Table D-1 POST Check Points

Check Point	Descriptions
5FH	• Enables/Disables USB function
60H	• Initializes SRAM cache capacity • Enables the cache function
64H	• Tests keyboard interface *Note: The keyboard LEDs should flash once.*
68H	• Enables UIE, then checks RTC update cycle *Note: The RTC executes an update cycle per second. When the UIE is set, an interrupt (IRQ8) occurs after every update cycle and indicates that over 999ms are available to read valid time and date information.*
70H	• Initializes parallel port(s)
74H	• Initializes serial port(s)
75H	• Initializes RDM
78H	• Resets math coprocessor
7CH	• Checks and initializes pointing device
84H	• Initializes keyboard
88H	• Sets HDD type and features (i.e. transfer speed, mode, ...) • Tests HDD controller
6CH	• Tests and initializes FDD *Note: The FDD LED should flash once and its head should be positioned.*
80H	• Sets security status
90H	• Displays POST status
89H	• CPU Internet Frequency testing
93H	• Rehooks INT 1CH for Quiet Boot
94H	• Initializes I/O ROM *Note: I/O ROM is an optional extension of the BIOS located on an installed add-on card as a part of the I/O subsystem. POST detects I/O ROMs and gives them opportunity to initialize themselves and their hardware environment.*
96H	• Initializes PCI I/O ROM
A0H	• Sets time and day
A2H	• Initializes setup items
A4H	• Initializes security features

Table D-1 POST Check Points

Check Point	Descriptions
A8H	• Setup SMI parameters
ACH	• Enables NMI, parity checking if set, and clear screen.
B0H	• Checks power-on password • Displays configuration mode table • Booting
BDH	• Shutdown 5
BEH	• Shutdown A
BFH	• Shutdown B

D.2. POST Error Messages

The power-on self-test (POST) is a program routine performed by the system BIOS. If there is any error during the POST routine, BIOS detects it and shows the corresponding error message on the CRT screen to guide the technical service engineer on the repair procedure.

Table D-2 POST Error Messages

Error Message	Possible Cause and Corrective Action
Memory Error at MMMM:SSSS:OOOOh (R:xxxxh, W:xxxxh)	• DRAM, SIMMs, or add-on memory card may be defective. ☛ Replace the DRAM chips or the SIMMs
System Management Memory Bad	• System Management Memory (SMM) is bad. This may be caused by the malfunction of system green function. ☛ Replace the DRAM chips or the SIMMs
PS/2 Keyboard Interface Error	• POST detects an error in the interface between the system board and the keyboard. The keyboard circuit module may be defective. ☛ Check the keyboard interface circuit or change the keyboard.
PS/2 Keyboard Error or Keyboard Not Connected	• POST detects an error in the keyboard; or the keyboard is not connected. ☛ Reconnect or replace the keyboard.
PS/2 Keyboard Locked	• The keyboard lock feature prevents any access to keyboard. ☛ Unlock the keyboard.
PS/2 Pointing Device Error	• The pointing device installed may be bad or the device is improperly connected. ☛ Reconnect or replace the pointing device.
PS/2 Pointing Device Interface Error	• POST detects an error in the interface between the system board and the pointing device. ☛ Check the keyboard interface circuit.

Table D-2 POST Error Messages

Error Message	Possible Cause and Corrective Action
IDE Primary Channel Master Drive Error IDE Primary Channel Slave Drive Error IDE Secondary Channel Master Drive Error IDE Secondary Channel Slave Drive Error	• The IDE drive may be bad, type mismatched, or not properly installed. ☛ Replace the disk drive or the hard disk drive controller. Check the HDD cable connections and CMOS setup configuration.
Diskette Drive A Error Diskette Drive B Error	• Diskette A or B may be bad. ☛ Replace the diskette drive.
Diskette Drive Controller Error	• This error is caused by any of the following: (1) The power supply cable is not connected to the diskette drive connector. (2) The diskette drive cable is not plugged to the diskette drive interface on the system board. (3) The diskette drive controller is defective. ☛ Check the diskette drive cable and its connections. If the cable is good and properly connected, the diskette drive controller may be the problem. Change the diskette drive controller or disable the onboard controller by installing another add-on card with a controller.)
CPU Clock Mismatch	• CPU frequency has been changed by the user. ☛ When the user changes the CPU frequency, this message will be shown once. Then the BIOS will adjust CPU clock automatically.
On Board Serial Port 1 Conflict(s) On Board Serial Port 2 Conflict(s)	• Onboard serial port address conflicts with the add-on card serial port. ☛ Change the onboard serial port address in Setup or change the add-on card serial port address.
On Board Parallel Port Conflict(s)	• Onboard parallel port address conflicts with the parallel port of add-on card. ☛ Change onboard parallel port address in CMOS SETUP or set the parallel port address of add-on card to others.
Real Time Clock Error	• POST detects a real-time clock error. ☛ Check RTC circuit or replace the RTC.
CMOS Battery Bad	• CMOS battery power lost. ☛ Replace the onboard lithium battery

Table D-2 POST Error Messages

Error Message	Possible Cause and Corrective Action
CMOS Checksum Error	• CMOS RAM error. ☛ Run Setup again and reconfigure the system.
NVRAM checksum Error	• The NVRAM in the EISA model contains EISA configuration information. Accidental data writes in the NVRAM area causes an error. POST detects the error and displays the corresponding error message. ☛ Run EISA configuration utility (ECU) to restore the original EISA configuration data.
On Board xxx ... Conflict(s)	• On Board device resources (ex. IRQ, DMA, I/O Address) conflict. ☛ Try to reassign or disable on board device resources.
PCI Device Error	• PCI device may be bad. ☛ Check the PCI card. Replace if bad.
System Resource Conflict	• Some system resources conflict with the resources required by the PCI device. ☛ Run Setup to reconfigure the system.
IRQ Setting Error	• Wrong IRQ setting for the PCI device. ☛ Run Setup to reconfigure the system.
Expansion ROM Allocation Fail	• The I/O expansion ROM fails to allocate for the PCI device. ☛ Change the I/O expansion ROM address.

D.3. NMI Error and Warning Messages

Non-Maskable Interrupt (NMI) causes the CPU routines to be interrupted and the system to be halted.

Table D-3 NMI Error Messages and Warning Messages

Error Message	Possible Cause and Corrective Action
RAM Parity Error	• DRAM chips, SIMMs, or add-on memory card may be defective. ☛ Replace the DRAM chips or SIMMs, or disable parity check in Setup if the model supports it.
I/O Parity Error	• The I/O access is not correct. ☛ Check all I/O related circuits (i.e. system I/O controller, memory controller, interrupt controller, DMA controller, etc.)
Press Ctrl_Alt_Esc key to enter SETUP or F1 key to Continue...	• A system configuration error is detected, or the hardware configuration does not match the Setup configuration data in CMOS. ☛ Press CTRL + ALT + ESC to reconfigure the system.
Press 1 key to enter SETUP or other key to continue...	• This message appears on the screen when a terminal instead of a console monitor is installed. ☛ Press 1 to enter Setup and check the configuration. Pressing any other key prevents entering Setup.
Press ESC to turn off NMI, or any key to reboot	• A Non-Maskable Interrupt (NMI) occurs. ☛ Press ESC to reject NMI error or press any other key to reboot the system.
Insert system diskette and press <Enter> key to reboot	• A non-bootable diskette is detected on the diskette drive when the system boots. ☛ Insert a bootable disk in the diskette drive or remove this disk if a hard disk drive is installed.
Equipment Configuration Error	• The hardware configuration does not match the Setup configuration data. ☛ Run Setup and reconfigure the system.
EISA Configuration Error	• This message appears in any one of the following conditions: (1) An add-on card is plugged into the wrong expansion slot. (2) The ECU was not executed when a new add-on card is installed. (3) A old add-on card was move to another slot. ☛ Run ECU.