CH-386-33A/40A

Mainboard

User's-Manual

CH-386-33A/40A

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User's Manual

1 st Edition
Nov 1991

1. Introduction

The OPTI-386 write-back is a highly integrated PC / AT VLSI chipset, for the high end 386-based AT systems, It includes system controller (SYSC,82C391), Data Buffer controller (DBC,82C392) and integrated peripheral controller (82C206)

1-2 Mainboard Specification

- 33MHz/40MHz 80386 DX CPU
- 80387/WEITEK 3167 Socket on board
- Coprocessor supports SYNC mode only
- Copy-Back Direct Mapped Cache with size of 32/64/128/256KB
- 16 bytes Line size for cache miss cycle
- Support 256K/1M/4M DRAM Type
- Up to 32MB Local fast page mode DRAM memory space
- Supports Two Non-cacheable Regions Control
- Shadow RAM support
- Option for Cacheable video BIOS
- Supports Hardware / software switch operation for Turbo / slow speed.
- Supports AT bus clock selectable

- Two 8-bit and Six 16-bit expansion slots
- On board rechargeable battery backup for CMOS configuration and real-time clock
- Optimized for OS/Z, XENIX, WINDOWS/386 software operation

1-3 Cache Control Subsystem

The Cache Control is Copy-Back Direct Mapped Cache with size of 32/64/128/256KB selectable the cache has been designed to operate at non-pipeline mode and support line size of 16 bytes during cache Read miss cycle for update cache memory Data.

The following table on the next page shows the cache sizes support Tag RAM used, cacheable main memory size

CACHE SIZE (KB)	TAG RAM SIZE/TAG RAM LOCATION	CACHE RAM SIZE/CACHE RAM LOCATION	CACHEABLE MAIN MEMORY (MB)
32	4Kx4bit U32,U33,U42	8Kx8bit U34,U35,U36,U37	8
64	4Kx4bit U32,U33,U42	8Kx8bit U34-U37,U43-U46	16
128	16Kx4bit U32,U33,U42	32Kx8bit U34,U35,U36,U37	32
256	16Kx4bit U32,U33,U42	32Kx8bit U34-U37,U43-U46	64

1-4 Local DRAM Control Subsystem

This mainboard support 2 bank, page mode local memory, DRAM devices can be 256K, 1 M or 4M and total memory can be up to 32MB, The following table on the next page illustrates the configurations supported.

BANK 0	BANK 1	TOTAL
256K	X	1M
256K	256K	2M
1M	X	4M
256K	1M	5M
1M	1M	8M
4M	X	16M
1M	4M	20M
4M	1M	20M
4M	4M	32M

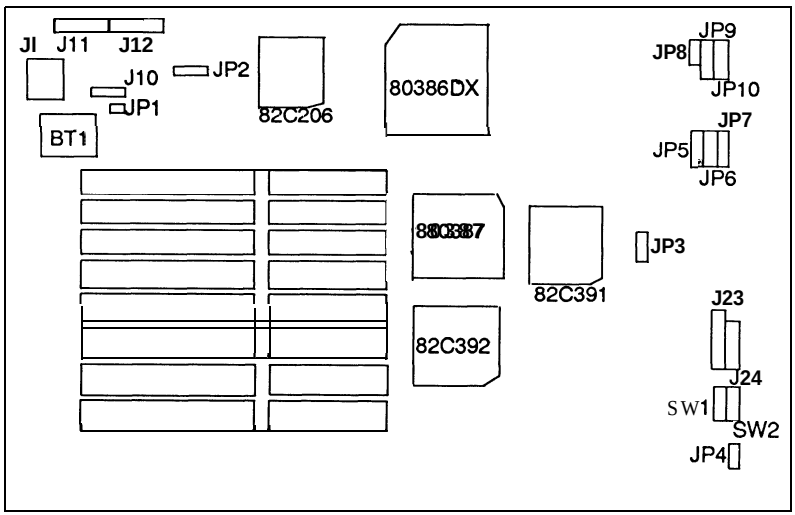
*** fast page mode 80ns DRAM is used**

> * *For* example *:*
>
> *Fuji MB81256-80 does not support fast page mode timing, Upon booting the system will appear parity error message when using the DRAM.*

2. Configuration of the Mainboard

2-1 Connector and Jumper settings.

The following is a description of jumpers and connectors of the CH-386-33A/40A mainboard.



- J1 = Keyboard Connector
- J10 = External Battery Connector
- J11 = Power Connector (P8)
- J12 = Power Connector (P9)
- J23 = Keylock & power LED connector
- J24 = Speaker connector
- JP1 = CRT TYPE Jumper
  open : monochrome monitor
  short : color monitor
- JP2 = CMOS Jumper
  1-2 : clear CMOS memory
  2-3 : normal operation
- JP3 = AT Bus clock selectable jumper
  open : AT Bus clock is CPU clock divided by 6
  short : AT Bus clock is CPU clock divided by 8
  (for 33MHz only, 40MHz always 8MHz)
- JP4 = Turbo LED
- SW1 : Hardware RESET switch connector
- SW2: Hardware TURBO switch connector
- JP5, JP6, JP7, JP8, JP9, JP10 = cache jumper

	JP5	JP6	JP7	JP8	JP9	JP10
32K	1-2	1-2	1-2	OPEN	2-3	2-3
64K	2-3	I-2	I-2	OPEN	2-3	1-2
128K	2-3	I-2	2-3	SHORT	2-3	I-2
256K	2-3	2-3	2-3	SHORT	I-2	1-2

Notes:
Cache even bank: U34, U35, U36, U37
Cache odd bank: U43, U44, U45, U46
Tag RAM: U32, U33, U42
32K cache, put 8Kx8 SRAM at even bank
4Kx4 SRAM at U32, U33, and U42
64K cache, put 8Kx8 SRAM at both even & odd bank,
4Kx4 SRAM at U32, U33, and U42
128K cache, put 32Kx8 SRAM at even bank
16Kx4 SRAM at U32, U33, and U42
256K cache, put 32Kx8 SRAM at both even & odd bank
16Kx4 SRAM at U32, U33, and U42

- TAG RAM access time is 15ns, cache RAM access time is 25ns for 33MHz or 20ns for 40MHz Main Board.

3. BIOS SETUP

3-1. BIOS OVERVIEW

The SETUP program is used to configure the system. This system options are stored in the CMOS. If the CMOS is good, the system is configured with the values stored in the CMOS. If the CMOS is bad, the system is configured with the default values stored in the ROM file.

There are two (2) sets of BIOS values stored in the ROM file :

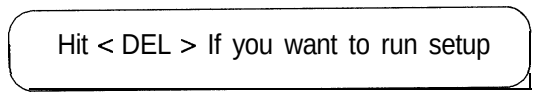
- The BIOS Setup defualt values
- The Power-On default values

The BIOS Setup default values are the default values which are supposed to give optimum performance for the system. They are the best case default values.

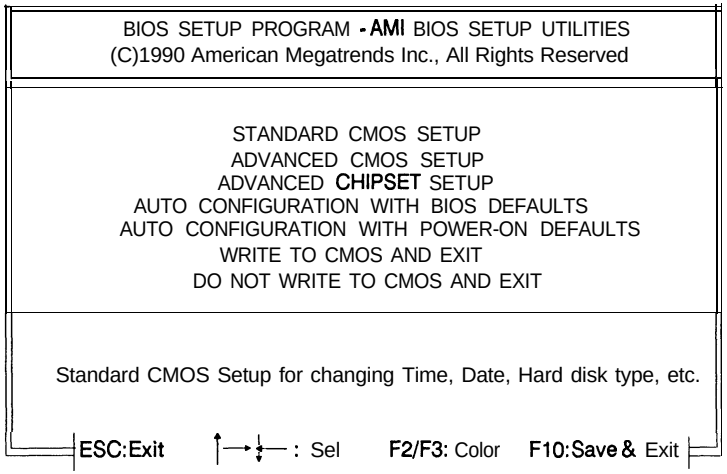
The Power-On default values are the default values for the table values for the system. They are the worst case default values.

There are two ways to enter the BIOS setup program :

- Whenever BIOS detects any equipment error or the **CMOS** contents are not consistent with the equipment.
- After the power on memory test, the screen will show :



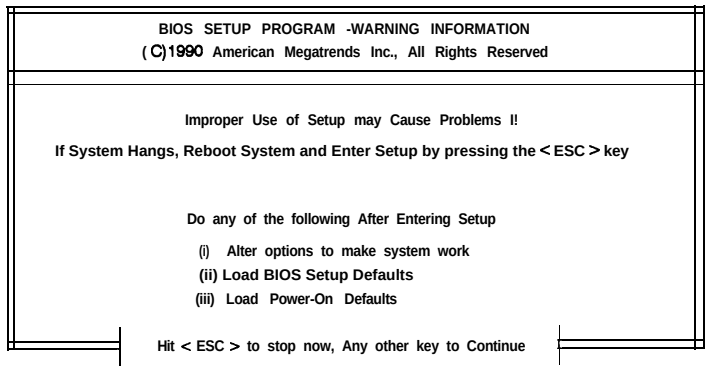
— **Press the DEL key to get the following screen on the next page:**



Explanation of keys :

ESC	: Exit to setup program
Arrow keys	: Cursor movement
F2 / F3	: Change Color
F10	: Save Setup values & Exit to setup program

The User is given a warning message before he is allowed to change any of the setup parameters. The warning message is shown as follows:



— Figure 3 : BIOS Setup Warning Message

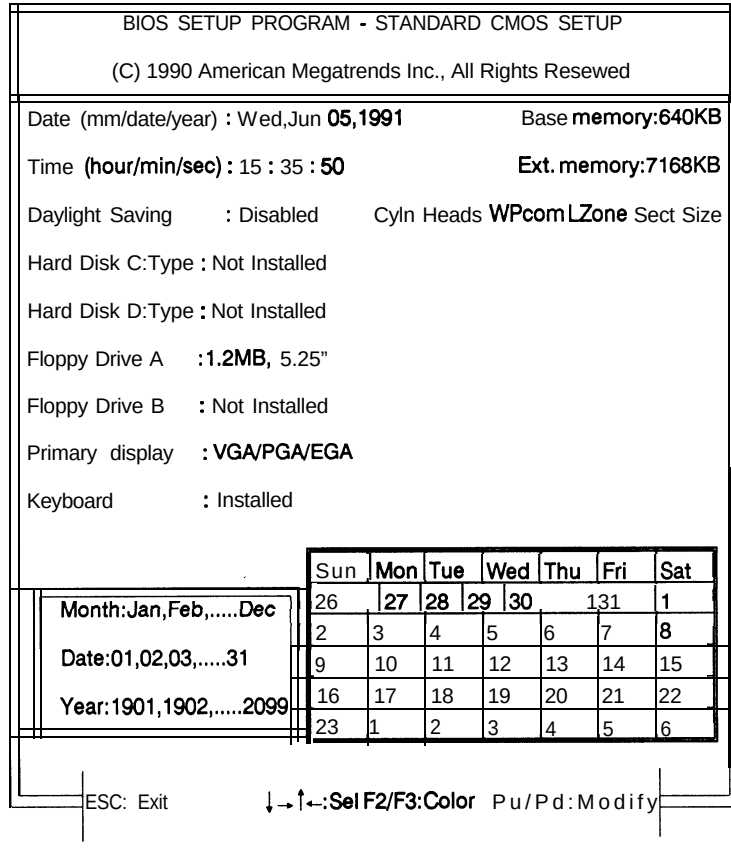
Explanation of keys :

ESC	: Exit to previous screen
Any keys	: Continue choosing setup program

3-2. STANDARD CMOS SETUP

This Option is used to configure the following options:

- Date : Month, Date and Year.
- Time : Hour, Minute and Second.
- Daylight Saving : Disabled or Enabled.
- Hard Disk C: and Hard Disk D: The User can choose any of the standard hard disk types from 1 to 46 or he can choose type 47 which is the user definable type. The User must enter the hard disk parameters if he wants to choose the user-definable hard disk type per drive, i.e., type 47 may be different for drive C: and for drive D:.
- Floppy Drive A: and Floppy Drive B: 360 KB 5.25", 1.2 MB 5.25", 720 KB 3.5", 1.44 MB 3.5", Not Installed.
- Primary Display : Monochrome, Color 40 x 25, VGA/PGA/EGA, Color 80 x 25, Not Installed.
- Keyboard : Installed or Not Installed.


BIOS SETUP PROGRAM - STANDARD CMOS SETUP
(C) 1990 American Megatrends Inc., All Rights Resewed
Date (mm/date/year) : Wed,Jun 05,1991
Base memory:640KB
Time (hour/min/sec) : 15 : 35 : 50
Ext. memory:7168KB
Daylight Saving : Disabled
Cyln Heads WPcom LZone Sect Size
Hard Disk C:Type : Not Installed
Hard Disk D:Type : Not Installed
Floppy Drive A :1.2MB, 5.25"
Floppy Drive B : Not Installed
Primary display : VGA/PGA/EGA
Keyboard : Installed
Month:Jan,Feb,.....Dec
Date:01,02,03,.....31
Year:1901,1902,.....2099
Sun Mon Tue Wed Thu Fri Sat
26 27 28 29 30 31 1
2 3 4 5 6 7 8
9 10 11 12 13 14 15
16 17 18 19 20 21 22
23 1 2 3 4 5 6
ESC: Exit
↓→↑←:Sel F2/F3:Color
Pu/Pd:Modify

- Note : Daylight Saving

  — The RTC has a built-in capability to automatically adjust the time on the two daylight savings days of the year **(*).** If this is desired, set the field to “Enable”.

Otherwise, set field to “Disabled”. Note that in general, nothing will be immediately observable by setting the field to either state.

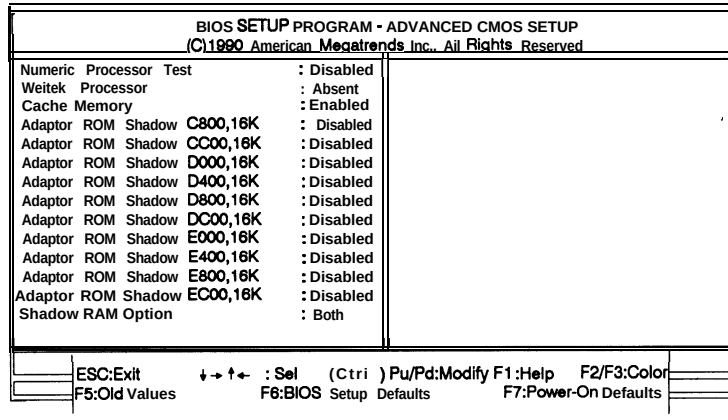
- *Eg, **Daylight Savings.. ..... Enable***
- ***Dayligh t Savings.. .....Disable***

> ***** *On the last Sunday of April, the time increments from 1:59:59 am to 3:00:00 am. On the last Sunday in October, when the time first reaches 1:59:59 am, it is rolled- back to 1:00:00 am.*

3-3. ADVANCED CMOS SETUP

The ADVANCED CMOS SETUP option is used to set the various system options for the user. The User can get various options, some of which are listed below:

- Numeric Processor Test
- Weitek Processor
- Cache Memory
- Adaptor ROM Shadow
- Shadow RAM


BIOS SETUP PROGRAM - ADVANCED CMOS SETUP
(C)1990 American Megatrends Inc., All Rights Reserved
Numeric Processor Test : Disabled
Weitek Processor : Absent
Cache Memory : Enabled
Adaptor ROM Shadow C800,16K : Disabled
Adaptor ROM Shadow CC00,16K : Disabled
Adaptor ROM Shadow D000,16K : Disabled
Adaptor ROM Shadow D400,16K : Disabled
Adaptor ROM Shadow D800,16K : Disabled
Adaptor ROM Shadow DC00,16K : Disabled
Adaptor ROM Shadow E000,16K : Disabled
Adaptor ROM Shadow E400,16K : Disabled
Adaptor ROM Shadow E800,16K : Disabled
Adaptor ROM Shadow EC00,16K : Disabled
Shadow RAM Option : Both
ESC:Exit ↓→↑← : Sel (Ctrl) Pu/Pd:Modify F1:Help F2/F3:Color
F5:Old Values F6:BIOS Setup Defaults F7:Power-On Defaults

Explanation of keys

- ESC : Exit to previous screen
- Arrow keys : Cursor movement
- PageUp / PageDown / Ctrl PageUp / Ctrl PageDown : Modify the value of the option by 1/-1/10/-10. If the option has less than 10 available answers, then < Ctrl PageUp > is the same as < PageUp > and < Ctrl PageDown > is the same as < PageDown > .
- F1 : Option for Help
- F2 / F3 : Change Color
- F5 : Get the old values. These are values with the user starting from the current session. If the CMOS was good, then the old values are the CMOS values, hense they are the BIOS Setup default values.
- F6 : This will load all the options in the Advanced CMOS Setup / Advanced Chipset Setup with the BIOS setup defaults
- F7 : This will load all the options in the Advanced CMOS Setup / Advanced Chipset Setup with the Power-On defaults

☐ Numeric Processor Test

INTEL Coprocessor insert in socket, Enable is set.
When not inserted, Disable is set.

☐ WEITEK Processor

WEITEK coprocessor insert in socket, present is set.
When not inserted in socket, absent is set.

☐ Cache Memory

This function can be setup Enable/Disable External Cache 32/64/128/256KB.

☐ Adaptor RAM Shadow

Adaptor Shadow RAM address range from C8000H to EFFFFH, each block size at the 16KB for Enable or Disable

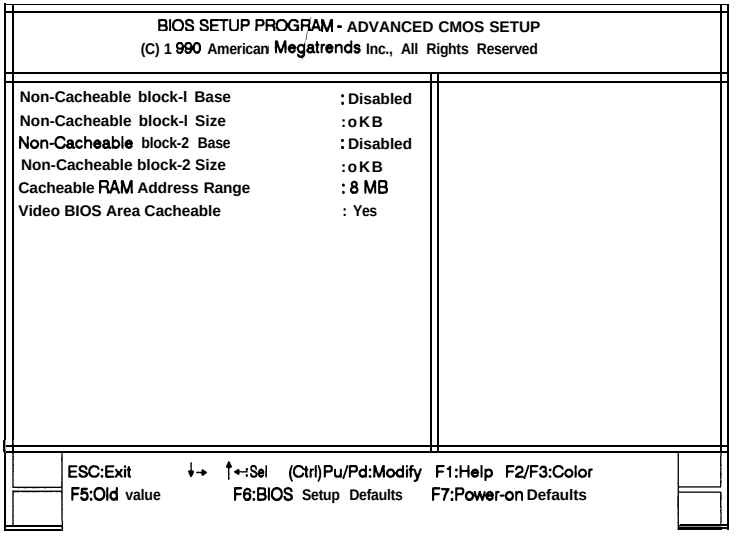
☐ Shadow RAM

There are four functions that can be selected:

Video	: Video shadow (C0000 ~ C7FFFH)
Main	: Main BIOS shadow (FOOOO ~ FFFFFH)
Both	: Video and Main BIOS shadow
Disable	: Disable shadow

3-4. ADVANCED CHIPSET SETUP

The ADVANCED CHIPSET SETUP option is used to change the register values for the chipset registers. The chipset registers control most of the system options in the computer.



Explanation of keys :

- ESC : Exit to previous screen
- Arrow keys : Cursor movement
- PageUp / PageDown / Ctrl PageUp / Ctrl PageDown : Modify the value of the option 1/-1/10/-10. If the option has less than 10 available answers, then < Ctrl PageUp > is the same as < PageUp > and < Ctrl PageDown > is the same as < pageDown >
- F1 : Option for Help
- F2 / F3 : Change Color
- F5 : Get the old values. This are the values with the user starting from the current session. If the CMOS was good, then the old values are the CMOS values, hence they are the BIOS Setup default values.
- F6 : This will load all the options in the Advanced CMOS Setup / Advanced Chipset Setup with the BIOS Setup defaults
- F7 : This will load all the options in the Advanced CMOS Setup / Advanced Chipset Setup with the Power-On defaults

☐ Non-Cacheable Block Size

This setup for set Non-Cacheable block size of 64/128/256/512K/Disable

☐ Non-Cacheable Block Base

This setup for set Non-Cacheable block starting address for example, if a 512KB non-cacheable block is selected, its starting address is a multiple of 512KB

☐ Cacheable RAM Address Range

This Cacheable DRAM size, you can select from range (1-64MB)

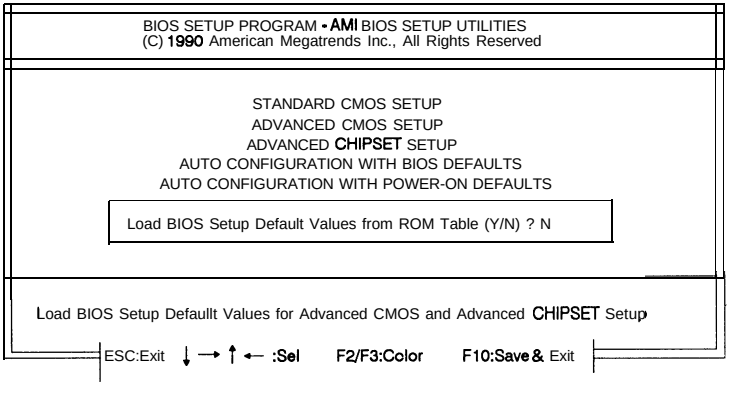
☐ Video BIOS Area Cacheable

Enable or Disable Video BIOS Cacheable

Please check you VGA card, If OAK VGA card (slow speed), this function must disable

3-5. AUTO CONFIGURATION WITH BIOS DEFAULTS

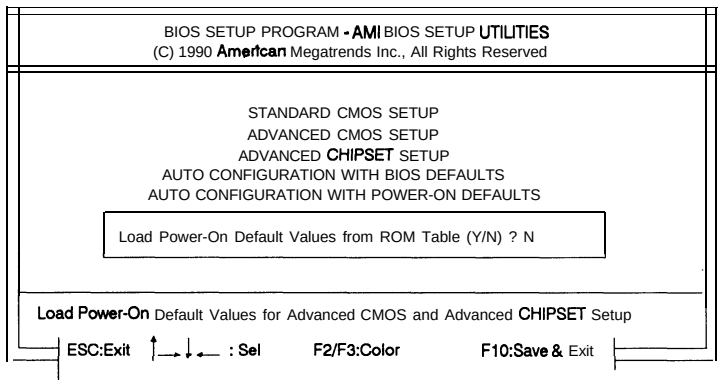
When you enter AUTO CONFIGURATION WITH BIOS DEFAULTS, the screen will be as follows:



- Press "Y" or "N" to change ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP with BIOS default values.

3-6. AUTO CONFIGURATION WITH POWER-ON DEFAULTS.

When you enter AUTO CONFIGURATION WITH POWER-ON DEFAULTS, the screen will be as follows:



— Press "Y" or "N" to change ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP with Power-On default values.

3-9. WRITE TO CMOS AND EXIT

The options set in the Standard Setup, Advanced Setup, Advanced Chipset Setup and the New password (If it has been changed) are stored in the CMOS. The CMOS checksum is calculated and writtten into the CMOS. After that, control is passed back to the BIOS.

3-10. DO NOT WRITE TO CMOS AND EXIT

Control is passed back to the BIOS without writing to the CMOS.