CH-486-33A

User's Manual

1st Edition, June 1991

The information contained in this manual is subject to change without notice

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1 .Introduction

The CH-486-33A is a three-chip solution offering optional performance for high-end 486-based AT systems. The CH-486-33A is designed for INTEL 80486DX running 33 MHz or INTEL 80486SX running for 20/25MHz combines three major functions:

- The 82C493 System Controller (sysc)
- The 82C392 Data Buffer Contrdler (DBC)
- The 82C206 Integrated Peripheral Controller (IPC)

I-I. CH-486-33A Mainboard Specification

- 33 MHz INTEL 80486 DX CPU OR 20/25 MHz INTEL 80486 SX CPU
- ISA architecture
- Copy-Back Direct-Mapped Cache with size of 64KB or 256 KB selectable
- Up to 32 MB of local high-speed page-mode DRAM memory space
- DRAM TYPE support 256K/1M/4MB
- Control of two non-cacheable regions
- Shadow RAM support
- Optional Cacheable of shadow video BIOS
- Turbo/slow speed selectable for hardware and software controller

- WEITEK 4167 coprocessor socket on board
- On board rechargeable battery back-up for CMOS configuration and real-time dock
- Optimized for **OS/2, window/386,** window 3.0, XENIX, UNIX software operation
- Baby AT size, with XT/AT mounting **hole**

2. Hardware Description

2-1 System Description

80486 Microprocessor

The 80486 is a high performance 32-bit microprocessor with on-chip memory management, floating point and cache memory units. It is binary compatible with members of the 86 architectural family. The 486 CPU contains all the features of the 386 CPU with enhancements to increase performance.

On-chip Floating Point Control Unit

The operation of the 486 microprocessor's on-chip floating point control unit is exactly the same as the 387 math coprocessor. Software written for the 387 math coprocessor will run on the on-chip floating point unit without any modification. It occupies I/O address range of 800000F0H-800000FFH and operates in parallel with the arithmetic and logic unit and provides arithmetic instructions for a variety of numeric data types.

On-chip Cache Memory

The 8KB on-chip cache is a 4-way set associative write-through code and data cache memory. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware.

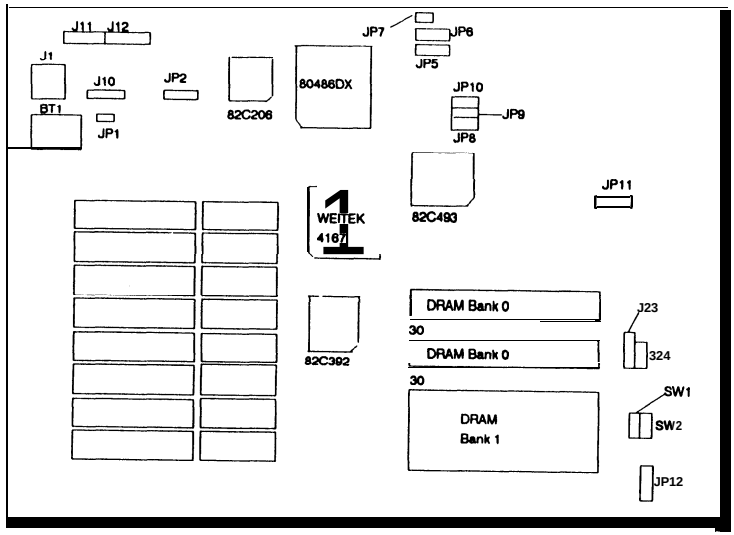
4167 Floating-point Coprocessor

The WEITEK 4167 is a high-performance single-chip floating-point coprocessor for 80486 microprocessor. It is upwardly binary compatible with the WEITEK 3167 coprocessor.

The 4167 coprocessor is a memory-mapped peripheral that communicates with the 80486 over the same address bus that connects the main memory to CPU. The coprocessor will respond to memory addresses C0000000H through C1FFFFFFH. Writing to this address space will cause the 4167 to execute this fractions and reading from it will cause the coprocessor to drive the data bus.

2-2 Connector and Jumper Settings

This chapter describes the CH-486-33A main board's jumpers and connectors
The system layout are shown on the next page.


J11
J12
J1
J10
JP2
BT1
JP1
82C206
80486DX
JP7
JP6
JP5
JP10
JP9
JP8
82C493
JP11
WEITEK
4167
82C392
DRAM Bank 0
30
DRAM Bank 0
30
DRAM
Bank 1
J23
324
SW1
SW2
JP12

SW1 : Hardware Reset switch Connector

sw2: Hardware Turbo Switch Connector

J1: Keyboard Connector

J10: External Battery Connector

J11, J12: Power Connector

J23: **Keylock** and Power LED Connector

J24: Speaker Connector

JP12: Turbo LED Connector

Jumper	Description	Setting
JP1	Monitor Type Selectable	Short : Color Open : Monochrome
JP2	CMOS power	1-2 : Clear CMOS RAM 2-3 : Backup CMOS RAM
JP4		Always 2-3 Short
JP5	CPU selectable	1-2 : 487SX (2-3 : 486DX 1-3 Open : 486SX
JP6	CPU selectable	1-2 : 486 DX, 487SX 2-3 : 486 SX
JP7	CPU selectable	[Short : 486 DX, 487SX Open : 486 SX
JP8	Cache size selectable	Short : 256K Open : 64K
JP9	Cache size selectable	Short : 256K Open : 64K
JP10		[Always Open
JP11	Cache size selectable	Short : 256K Open : 64K

NOTE : 1. Those enclosed in box are Mainboard Default
2. This Mainboard only support Intel C or later stepping of processor.

2-3. DRAM Bank Configuration

The CH-486-33A supports 2 banks of page mode local memory, DRAM devices are either 256Kb, 1Mb or 4Mb large. Total memory is between 1MB and 32MB. The following table illustrates the configuration supported.

Bank 0	Bank 1	Total
256K		1MB
256K	256K	2MB
1M		4MB
256K	1M	5MB
1M	1M	8MB
4M		16MB
1M	4M	20MB
4M	1M	20MB
4M	4M	32MB

* Use 80ns DRAM

2-4 SRAM Configuration

The CH-486-33A has a non-pipeline mode with a 16 bytes line size copy-back Direct-mapped cache, because this cache controller design two-way interleave cache read/write, so only support 64K or 256K secondary cache size.

The following table shows the TAG RAM size, cache RAM size and cacheable main memory size supported by CH-486-33A.

Cache size (KB)	TAG RAM size	Cache RAM size	Cacheable main memory
64K	8K x 8bit U34 64K x 1bit U33	8K x 8bit u47 ~U49 U51 ~ U55	16MB
256K	32K x 8bit U34 64K x 1 bit U33	32K x 8bit u47 ~U49 U51 ~ U55	32MB

Note : . If you want to change second level cache size, you must change the SRA M and TAG RAM size and Jumper Setting.

3. BIOS SETUP

3-1. BIOS OVERVIEW

The SETUP program is used to configure the system. These system options are stored in the CMOS. If the CMOS is good, the system is configured with the values stored in the CMOS. If the CMOS is bad, the system is configured with the default values stored in the ROM file.

There are two (2) sets of BIOS values stored in the ROM file :

- The BIOS Setup default values
- The Power-On default values

The BIOS Setup default values are the default values which are supposed to give optimum performance for the system. They are the best case default values.

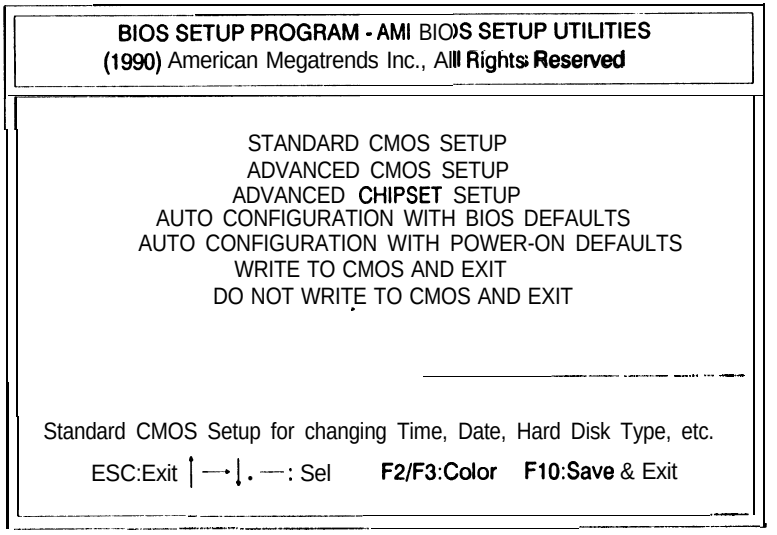
The Power-On default values are the default values for the table values for the system. They are the worst case default values.

There are two ways to enter the BIOS setup program

1. Whenever BIOS detects any equipment error or the CMOS contents are not consistent with the equipment.
2. After the power on memory test, the screen will show:

Hit <DEL> If you want to run setup

Press the DEL key to get the following screen:



Explanation of keys:

ESC:	Exit to setup program
Arrow keys:	Cursor movement
F2/ F3:	Change Color
F10:	Save Setup values & Exit to setup program

The user is given a warning message before he is allowed to change any of the setup parameters. The warning message is shown as following:

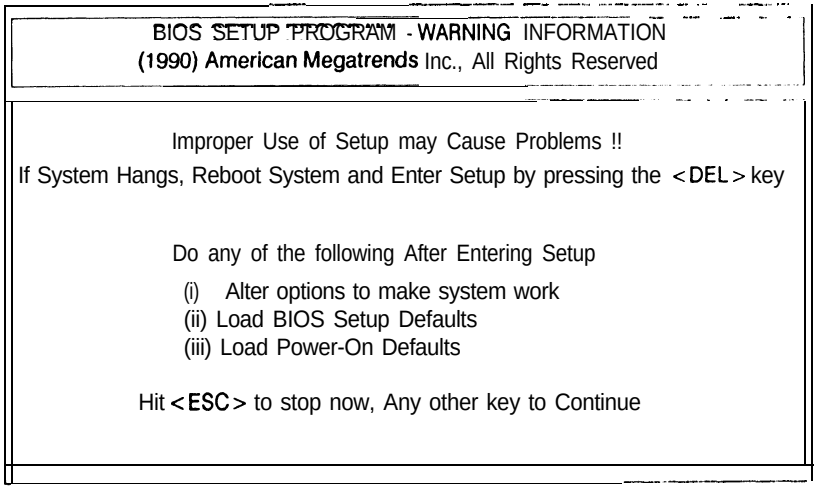


Figure 3 : BIOS Setup Warning Message

Explanation of keys:
Esc : Exit to previous screen
Any keys : Continue choose setup program

3-2 STANDARD CMOS SETUP

This option is used to configure the following options:

- Date: Month, Date and Year
- Time: Hour, Minute and Second
- Daylight Saving: Disabled or Enabled
- Hard Disk C: and Hard Disk D: The user can choose any of the standard hard disk types from 1 to 46 or he can choose type 47 which is the user defineable type. The user must enter the hard disk parameters if he wants to choose the user-definable hard disk type per drive, i.e., type 47 may be different for drive C: and for drive D:.
- Floppy drive A: and Floppy drive B: 360KB 5.25", 1.2MB 5.25", 720KB 3.5",1.44MB 3.5", Not Installed
- Primary Display: Monochrome, Color 40 x 25, VGA/PGA/EGA, Color 80x25, Not Installed
- Keyboard: Installed or Not Installed

BIOS SETUP PROGRAM-STANDARD CMOS SETUP
(C)1990 American Megatrends Inc., All Rights Reserved

Date (mm/ date/ year): Wed, Jun 05 1991 Base memory: 640 KB
lime (hour/ min/ sec) : 15 : 35 : 50 Ext. memory: 7168 KB
Daylight saving : Disabled Cyln Head WPcom LZone Sect Size
Hard disk C: type : Not Installed
Hard disk D: type : Not Installed
Floppy drive A : 1.2 MB, 5.25"
Floppy drive B : Not Installed
Primary display : VGA/ PGA/ EGA
Key board : Installed

Month:Jan,Feb,....Dec
Date :01,02,03....31
Year :1901,1902....2099

SUN	MON	TUE	WED	THU	FRI	SAT
26	27	28	29	30	31	1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	1	2	3	4	5	6

ESC:Exit ← ↑ → ↓ Select F2/ F3: Color PU/ PD:Modify

Note: Daylight Saving

The RTC has a built-in capability to automatically adjust the time on the two daylight savings days of the year **(*).** If this is desired, set the field to "Enable".

Otherwise, set field to "Disabled". Note that in general, nothing will be immediately observable by setting the field to either state.

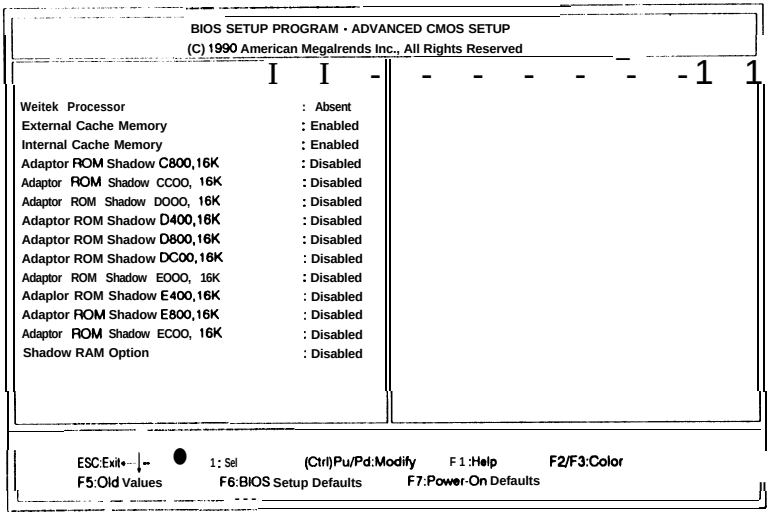
Eg, Daylight Savings.. ..... Enable
Daylight Savings.. ..... Disable

***** *On the last Sunday of April, the time increments from 1:59:59 am to 3:00:00 am On the last Sunday in October, when the time first reaches 1:59:59 am, it is rolled-back to 1:OO:OO am.*

3-3. ADVANCE CMOS SETUP

The ADVANCED CMOS SETUP option is used to set the various system options for the user. The user can get various options, some of which are listed below:

- Weitek Processor
- External Cache Memory
- Internal Cache Memory
- Adaptor ROM Shadow
- Shadow RAM


BIOS SETUP PROGRAM - ADVANCED CMOS SETUP
(C) 1990 American Megalrends Inc., All Rights Reserved
Weitek Processor : Absent
External Cache Memory : Enabled
Internal Cache Memory : Enabled
Adaptor ROM Shadow C800,16K : Disabled
Adaptor ROM Shadow CCOO, 16K : Disabled
Adaptor ROM Shadow DOOO, 16K : Disabled
Adaptor ROM Shadow D400,16K : Disabled
Adaptor ROM Shadow D800,16K : Disabled
Adaptor ROM Shadow DC00,16K : Disabled
Adaptor ROM Shadow EOOO, 16K : Disabled
Adaplor ROM Shadow E400,16K : Disabled
Adaptor ROM Shadow E800,16K : Disabled
Adaptor ROM Shadow ECOO, 16K : Disabled
Shadow RAM Option : Disabled
ESC:Exit
1: Sel
(Ctrl)Pu/Pd:Modify
F1:Help
F2/F3:Color
F5:Old Values
F6:BIOS Setup Defaults
F7:Power-On Defaults

Explanation of keys:

ESC : Exit to previous screen
Arrow keys : Cursor movement
PageUp/PageDown/Ctrl PageUp/Ctrl PageDown: Modify the value of the option by 1/-1/10/-10. If the option has less than 10 available answers, then < Ctrl PageUP > is the same as < PageUP > and < Ctrl PageDown > isthesameas < PageDown >
Fl : Opiton for Help
F2/F3 : Change Color
F5 : Get the old values. These are the values with the user starting from the current session. If the CMOS was good, then the old values are the CMOS values, hense they are the BIOS Setup default values.
F6 : This will load all the Options in the Advanced CMOS Setup/Advanced Chipset Setup with the BIOS Setup defaults
F7 : This will load all the Options in the Advanced CMOS Setup/Advanced Chipset Setup with the Power-On defaults

WEITEK Processor

WEITEK coprocessor insert in socket ,preset is set
When not inserted in socket, absent is set.

External Cache Memory

This function can be setup enable/disable External Cache (second leave cache) 64/256KB.

Internal Cache Memory

This function can be setup enable/disable CPU Internal cache 8 KB.

Adaptor RAM Shadow

Adaptor Shadow RAM address range from C8000H to EFFFFH, each Block size at 16KB for enable or disable

Shadow RAM

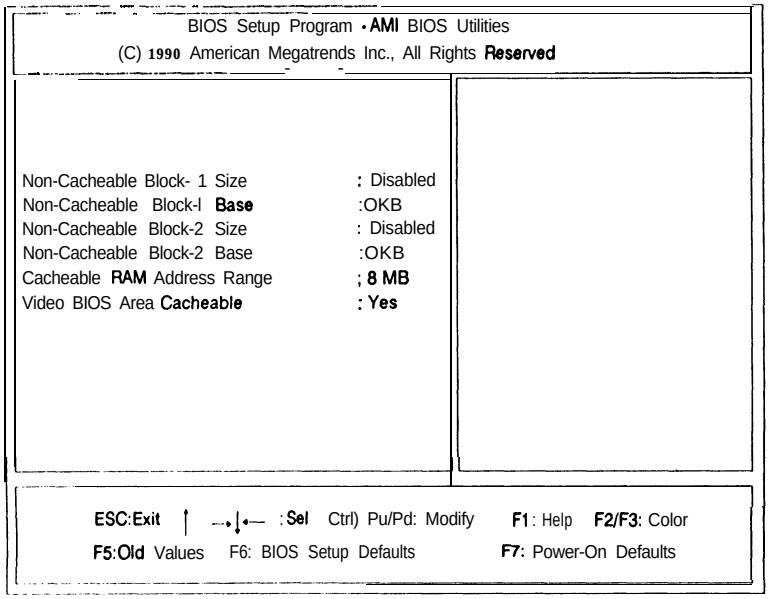
There are four function that can be selected:
Video : Video shadow (C0000 ~ C7FFFH)
Main : Main BIOS shadow (F0000 ~ FFFFFH)
both : Video and Main BIOS Shadow
Disable : Disable shadow

3-4 ADVANCED CHIPSET SETUP

The ADVANCED CHIPSET SETUP option is used to change the register values for the chipset registers. The chipset registers control most of the system options in the computer.

Explanation keys:

ESC : Exit to previous screen
Arrow keys : Cursor movement
PageUp/PageDown/Ctrl PageUp/Ctrl PageDown : Modify the value of the option by 1/-1/10/-10. If the option has less than 10 available answers, then <Ctrl PageUp> is same as <PageUp> and <Ctrl PageDown> is same as <PageDown>
F1: Help for the option
F2/F3: Change Color
F5: Get the old values. These are the values with the user starting from the current session. If the CMOS was good, then the old values are the CMOS values, hence they are the BIOS Setup default values.
F6 : This will load all the Options in the Advanced CMOS Setup/Advanced Chipset Setup with the BIOS Setup defaults
F7: This will load all the Options in the Advanced CMOS Setup/Advanced Chipset Setup with the Power-On defaults


BIOS Setup Program • AMI BIOS Utilities
(C) 1990 American Megatrends Inc., All Rights Reserved
Non-Cacheable Block- 1 Size : Disabled
Non-Cacheable Block-I Base :OKB
Non-Cacheable Block-2 Size : Disabled
Non-Cacheable Block-2 Base :OKB
Cacheable RAM Address Range ; 8 MB
Video BIOS Area Cacheable : Yes
ESC:Exit ↑ →|← :Sel Ctrl) Pu/Pd: Modify F1 : Help F2/F3: Color
F5:Old Values F6: BIOS Setup Defaults F7: Power-On Defaults

Non-Cacheable Block Size

This setup for set Non-Cacheable block size of 64/128/256/512K/Disable

Non-Cacheable Block Base

This setup for set Non-Cacheable Block Starting address for example, if a 512KB non-cacheable block is selected its starting address is a multiple of 512KB

Cacheable RAM Address Range

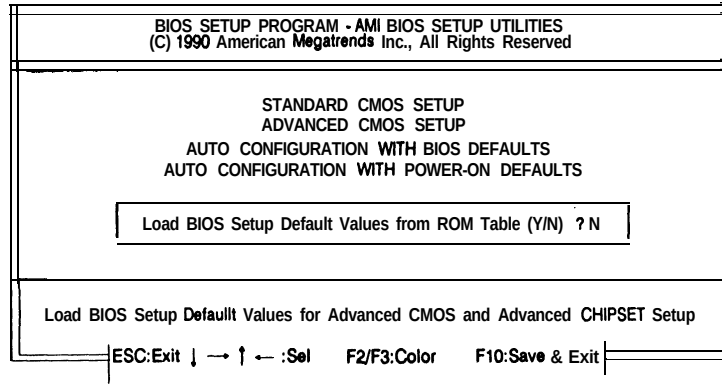
This Cacheable DRAM size, you can select from range (l-64MB)

Video BIOS Area Cacheable

Enable or Disable Video BIOS Cacheable
Please check your VGA card, If OAK VGA card (slow speed), this function must disable

3-5. AUTO CONFIGURATION WITH BIOS DEFAULTS

When you enter AUTO CONFIGURATION WITH BIOS DEFAULTS, the screen will be as follows:

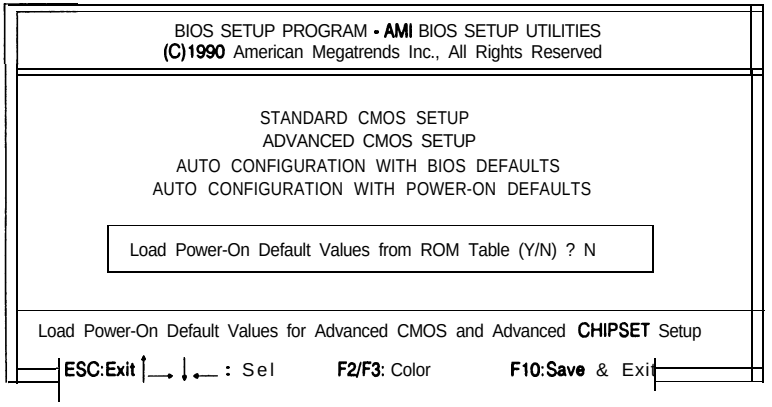


Press "Y" or " N" to change ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP with BIOS default values.

> *Note: The BIOS default values, setup chipset* register for *mainboard running high performance.*

3-6 AUTO CONFIGURATION WITH POWER-ON DEFAULTS.

When you enter **AUTO** CONFIGURATION WITH POWER-ON DEFAULTS, the screen will be as follows:



Press **"Y"** or **"N"** to change ADVANCED CMOS SETUP and ADVANCED **CHIPSET** SETUP with Power-on default values.

> *Note : The Power-On default values, setup chipset register for mainboard running low performance.*

3-9. WRITE TO CMOS AND EXIT

The options set in the Standard Setup, Advanced Setup, Advanced Chip-set Setup and the New Password (if it has been changed) are stored in the CMOS. The CMOS checksum is calculated and written into the CMOS. After that, control is passed back to the BIOS.

3-10. DO NOT WRITE TO CMOS AND EXIT

Control is passed back to the BIOS without writing to the CMOS.