CH 486

Mainboard

User's Manual

1st Edition, September 1991

The information contained in this manual is

subject to change without notice

NOTICE

Please set JP1 Pin1 & Pin2 to SHORT by a pin holder
Before using this MotherBoard for the first time!!

P/N : 252-0486S-D01

Table Of Contents

1. Introduction

The Mainboard is a three-chip solution offering optional performance for high-end 486-based AT systems. The board is designed for INTEL 80486DX running 33/50 MHz or INTEL 80486SX running for 20/25MHz combines three major functions:

- The 82C493 or 82C495 System Controller (sysc)
- The 82C392 Data Buffer Controller (DBC)
- The 82C206 Integrated Peripheral Controller (IPC)

1-1. Mainboard specification

- 33/50 MHz INTEL 80486 DX CPU OR 20/25 MHz INTEL 80486 SX CPU
- ISA architecture
- Copy-Back Direct-Mapped Cache with size of 64/256 KB (82C493) or 64/128/256 KB (82C495) selectable.
- Up to 32 MB of local high-speed page-mode DRAM memory space
- DRAM TYPE supports 256K/1M/4MB
- Control of two non-cacheable regions
- Shadow RAM support
- Optional Cacheable of shadow video BIOS
- Turbo/slow speed selectable for hardware and software controller
- WEITEK 4167 coprocessor socket on board
- On board rechargeable battery back-up for CMOS configuration and real-time clock
- Optimized for OS/2, window/386, window 3.0, XENIX, UNIX software operation
- Baby AT size, with XT/AT mounting hole

2. Hardware Description

2-1 System Description

☐ 80486 Microprocessor

The 80486 is a high performance 32-bit microprocessor with on-chip memory management, floating point and cache memory units. It is binary compatible with members of the 86 architectural family. The 486 CPU contains all the features of the 386 CPU with enhancements to increase performance.

☐ On-chip Floating Point Control Unit

The operation of the 486 microprocessor's on-chip floating point control unit is exactly the same as the 387 math coprocessor. Software written for the 387 math coprocessor will run on the on-chip floating point unit without any modification. It occupies I/O address range of 800000F0H-800000FFH and operates in parallel with the arithmetic and logic unit and provides arithmetic instructions for a variety of numeric data types.

☐ On-chip Cache Memory

The 8KB on-chip cache is a 4-way set associative write-through code and data cache memory. Individual pages can be designated as cacheable or non-cacheable by software or hardware. The cache can also be enabled and disabled by software or hardware.

☐ 4167 Floating-point Coprocessor

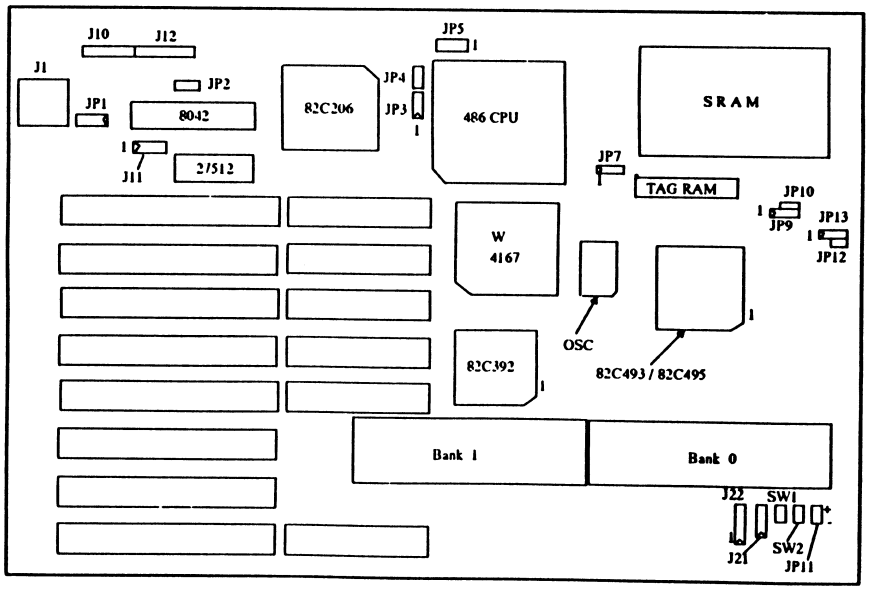
The WEITEK 4167 is a high-performance single-chip floating-point coprocessor for 80486 microprocessor. It is upwardly binary compatible with the WEITEK 3167 coprocessor.

The 4167 coprocessor is a memory-mapped peripheral that communicates with the 80486 over the same address bus that connects the main memory to CPU. The coprocessor will respond to memory addresses C0000000H through C1FFFFFFH. Writing to this address space will cause the 4167 to execute this fractions and reading from it will cause the coprocessor to drive the data bus.

2-2 Connector and Jumper Settings

This chapter describes the main board's jumpers and connectors

The system layout is shown as follows :



JUMPER	FUNCTION
SW1	Hardware Reset Switch Connector
SW2	Hardware Turbo Switch Connector
J1	Keyboard Connector
J10, J12	Power Connector
J11	External Battery Connector
J21	Speaker Connector
J22	Keylock and Power LED Connector
JP11	Turbo LED Connector

JUMPER	FUNCTION	SETTING
JP1	CMOS Power	1-2 : Clear CMOS RAM 2-3 : Backup CMOS RAM
JP2	Monitor Select	Open : Mono Monitor Short : Color Monitor
JP3	CPU Select	1-2 : 80486SX 2-3 : 80486DX Open : 80487SX
JP4	CPU Select	Short : 80486DX, 80486SX Open : 80487SX
JP5	CPU Select	1-2 : 80486DX, 80486SX 2-3 : 80487SX
JP7	CPU frequency select	2-3 : Short for frequency smaller than or equal to 33 MHz 1-2 : Short for 50 MHz frequency
JP9	Cache size select	1-2 : 256KB 2-3 : 64KB
JP10	Cache size select	Short : 128KB / 256KB Open : 64KB
JP12	Cache size select	Short : 128KB / 256KB Open : 64KB
JP13	82C493 chip	Always 1-2 short
	82C495 chip	1-2 : 64 / 256KB Cache size 2-3 : 128KB Cache size

* *Opti 82C495 chipset :* *running at 50 MHz, cache support 64 / 256KB*
running up to 33 MHz, cache support 64 / 128 / 256KB

2-3. DRAM Banks Configuration

The Mainboard supports 2 banks of page mode local memory, DRAM devices are either 256KB, 1MB or 4MB large. Total memory is between 1MB and 32MB. The following table on the next page illustrates the configuration supported:

BANK 0	BANK 1	TOTAL
256K		1M
256K	256K	2M
1M		4M
256K	1M	5M
1M	1M	8M
4M		16M
1M	4M	20M
4M	1M	20M
4M	4M	32M

Note : 80 ns fast page mode DRAM Module be required.

2-4 SRAM Configuration

The OPTI 82C493 and 82C495 CHIPSET is pin to pin compatible and only support non-pipeline mode with a 16 bytes line size. Copy-back direct mapped cache control, 82C493 chip only support 64/256KB cache size, 82C495 support 64/128/256KB cache size.

The following table shows the Cache size configuration:

CACHE MEMORY	TAG RAM SIZE	CACHE RAM TYPE
64KB	8K x 8 bit	8K x 8 bit
128KB	8K x 8 bit	32K x 8 bit
256KB	32K x 8 bit	32K x 8 bit

The following table shows the SRAM speed requirement.

CPU	TAG RAM	CACHE RAM
486SX-20	25nx	25ns
486SC-25	25ns	25ns
486DX-33/50	20/15ns	20ns

NOTE :
If you want to change secondary level cache size, you must change the TAGRAM size, cache RAM type and change the Jumpers Setting for the corresponding cache size .

If change the cache size, please check 82C493 or 82C495 chipset on the following examples on the next page :

1) **82C493 chipset :**

Examples:
64KB cache memory : insert 8K x 8 bit SRAM AT U34, U35,U36,U37,U38,U50,U51,U52,U53 socket and jumper

JP9	:	2-3 short
JP10	:	Open
JP12	:	Open
JP13	:	1-2 Short

256K cache memory : insert 32Kx8 bit SRAM AT U34, U35,U36,U37,U38,U50,U51,U52,U53 socket andjumper

JP9	:	1-2 short
JP10	:	short
JP12	:	short
JP13	:	1-2 short

2) **82C495 chipset**

Examples :
64/256KB cache size jumper setting 82C493 chipset are the same.
128KB cache memory : insert 32K x 8 bit SRAM AT U35,U36,U37,U38 socket, 8K x 8 bit SRAM AT U34 socket and jumper

JP9	:	2-3 short
JP10	:	short
JP12	:	short
JP13	:	2-3 short

3. BIOS SETUP

3-1. BIOS Overview

The SETUP program is used to configure the system. These system options are stored in the CMOS. If the CMOS is correct, the system is configured with the values stored in the CMOS. If the CMOS is in-correct, the system is configured with the default values stored in the ROM file.

There are two (2) sets of BIOS values stored in the ROM file :

- The BIOS Setup default values
- The Power-On default values

The BIOS Setup default values are the default values which are supposed to give optimum performance for the system. They are the best case default values.

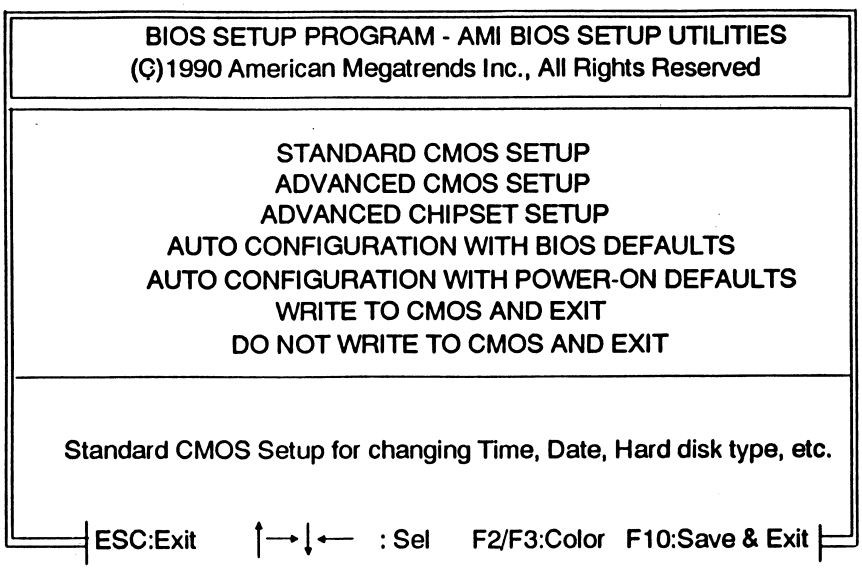
The Power-On default values are the default values for the table values for the system. They are the worst case default values.

There are two ways to enter the BIOS setup program

1. Whenever BIOS detects any equipment error or the CMOS contents are not consistent with the equipment.
2. After the power on memory test, the screen will show:

> Hit < DEL > If you want to run setup

PRESS THE DEL KEY TO GET THE FOLLOWING SCREEN :



Explanation of keys :

ESC	:	Exit to setup program
Arrow keys	:	Cursor movement
F2/F3	:	Change Color
F10	:	Save Setup values & Exit to setup program

The User is given a warning message before he is allowed to change any of the setup parameters. The warning message is shown as following :

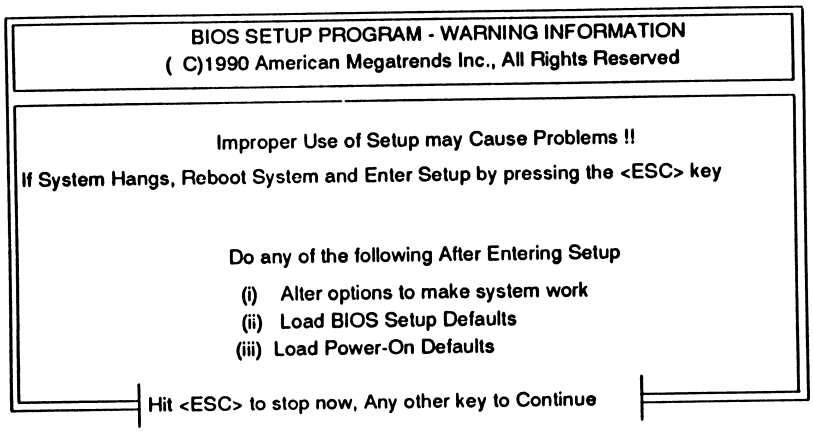
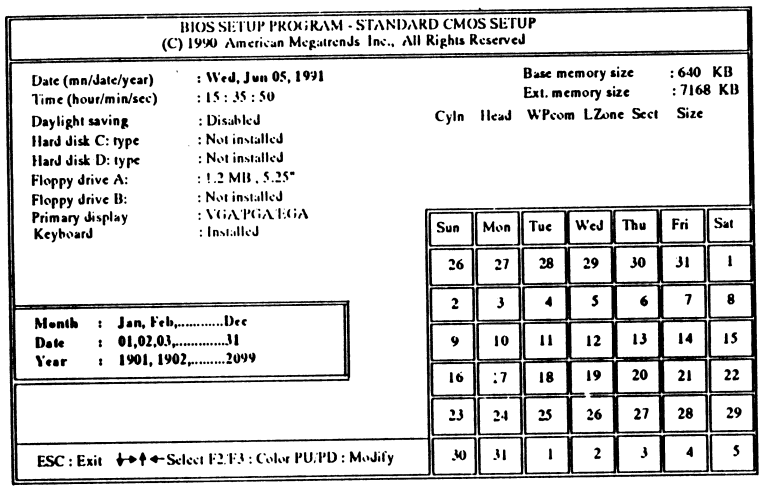


Figure 3 : BIOS Setup warning message

Explanation of keys :

Esc : Exit to previous screen
Any keys : Continue choose setup program



☐ Note : Daylight Savings

The RTC has a built-in capability to automatically adjust the time on the two daylight savings days of the year (*). If this is desired, set the field to "Enable".

Otherwise, set field to "Disabled". Note that in general, nothing will be immediately observable by setting the field to either state.

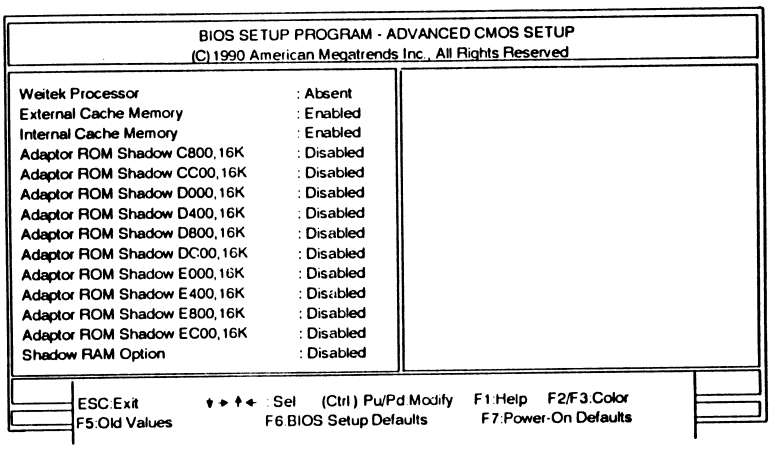
Eg, Daylight Savings.....Enable
Daylight Savings.....Disable

* *ON THE LAST SUNDAY OF APRIL, THE TIME INCREMENTS FROM 1:59:59 AM TO 3:00:00 AM. ON THE LAST SUNDAY IN OCTOBER, WHEN THE TIME FIRST REACHES 1:59:59 AM, IT IS ROLLED-BACK TO 1:00:00 AM.*

3-3. Advance CMOS Setup

The ADVANCED CMOS SETUP option is used to set the various system options for the user. The user can get various options, some of which are listed below:

- Numeric Processor Test
- Weitek Processor
- Cache Memory
- Adaptor ROM Shadow
- Shadow RAM



☐ WEITEK Processor

WEITEK coprocessor insert in socket ,preset is set
When not inserted in socket, absent is set.

☐ Cache Memory

This function can be setup enable/disable External Cache 64/256KB.

☐ Adaptor RAM Shadow

Adaptor Shadow RAM address range from C8000H to EFFFFH, each Block size at 16KB for enable or disable.

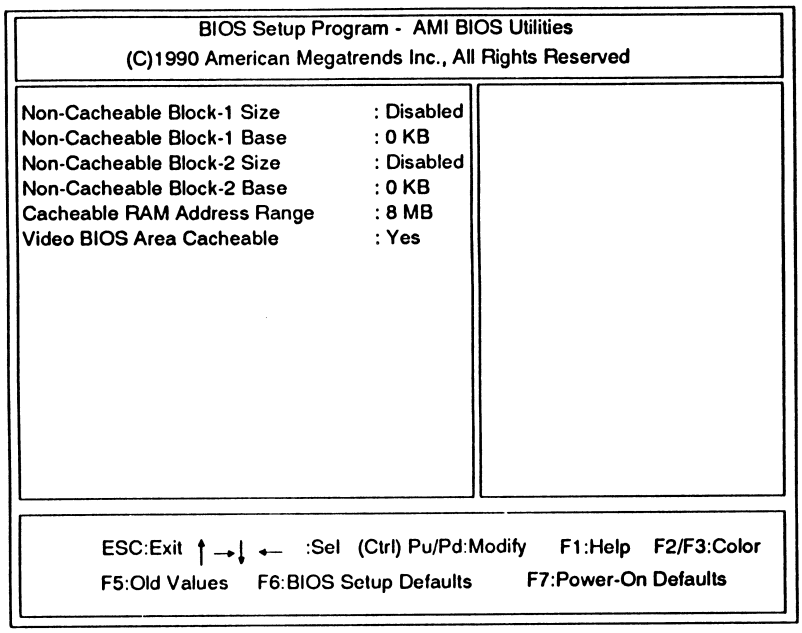
☐ Shadow RAM

There are four function that can be selected:

Video: Video shadow (C0000~ C7FFFH)
Main : Main BIOS shadow (F0000~ FFFFFH)
both : Video and Main BIOS Shadow
Disable : Disable shadow

3-4 Advance Chipset Setup

The ADVANCED CHIPSET SETUP option is used to change the register values for the chipset registers. The chipset registers control most of the system options in the computer.



☐ **Non-Cacheable Block Size**

This setup for set Non-Cacheable block size of 64/128/256/512K/Disable

☐ **Non-Cacheable Block Base**

This setup for set Non-Cacheable Block Starting address for example, if a 512KB non-cacheable block is selected, its starting address is a multiple of 512KB

☐ **Cacheable RAM Address Range**

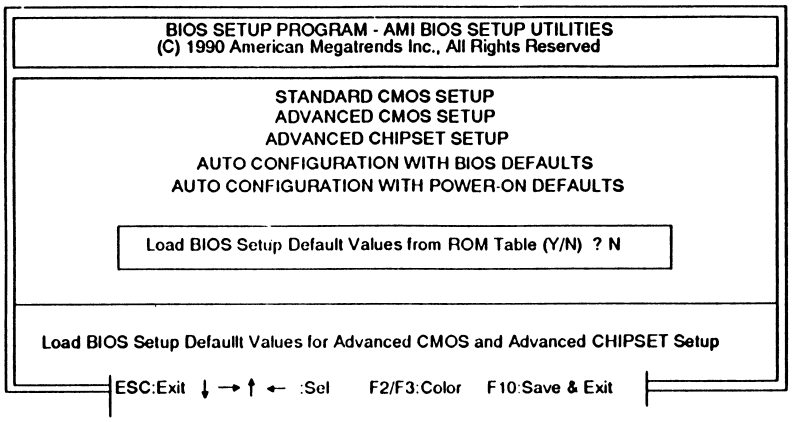
This Cacheable DRAM size, you can select from range (1-64MB)

☐ **Video BIOS Area Cacheable**

Enable or Disable Video BIOS Cacheable
Please check your VGA card, If OAK VGA card (slow speed), this function must disable

3-5. Auto Configuration with BIOS Defaults

When you enter AUTO CONFIGURATION WITH BIOS DEFAULTS, the screen will be as follows:

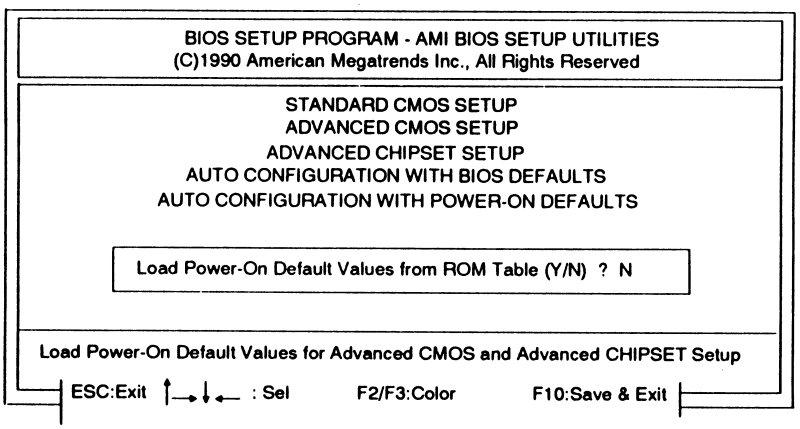


Press "Y" or "N" to change ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP with BIOS default values.

NOTE :
The BIOS default values setup chipset register for mainboard running high performance.

3-6 Auto Configuration with Power-On Defaults.

When you enter AUTO CONFIGURATION WITH POWER-ON DEFAULTS, the screen will be as follows:



Press "**Y**" or "**N**" to change ADVANCED CMOS SETUP and ADVANCED CHIPSET SETUP with Power-on default values.

NOTE :
The Power-On default values setup chipset register for mainboard running low performance.

3-9. Write to CMOS and Exit

The options set in the Standard Setup, Advanced Setup, Advanced Chip-set Setup and the New Password (if it has been changed) are stored in the CMOS. The CMOS checksum is calculated and written into the CMOS. After that, control is passed back to the BIOS.

3-10. Do Not Write to CMOS and Exit

Control is passed back to the BIOS without writing to the CMOS.