SUPERO®

440LX Chipset

AMI BIOS

REFERENCE MANUAL

Revision 1.1

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Do not upgrade the BIOS unless you are notified to do so. Please call technical support first before upgrading the boot-block BIOS.

SUPER BBS # (408) 895-2022 (24 hours)
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Chapter 1
AMI BIOS

1-1 Introduction

This chapter describes the AMIBIOS for the Intel 440FX/440LX chipset which is designed for Intel Pentium® Pro 150/166/180/200 MHz and Pentium II 233/266/300 MHz processors. The AMI ROM BIOS is stored in the Flash EEPROM and is easily upgraded using a floppy disk-based program.

System BIOS

The BIOS is the basic input output system used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. The WinBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-compatible systems, also called ISA (Industry Standard Architecture) must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of non-volatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real Time Clock. Many systems have 128 bytes of CMOS RAM.

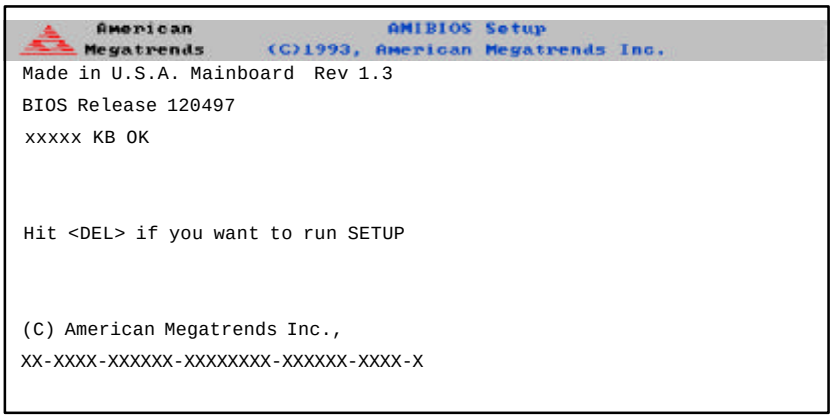
How Data Is Configured

AMIBIOS provides a Setup utility in ROM that is accessed by pressing <Del> at the appropriate time during system boot. Setup configures data in CMOS RAM.

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.



1-2 BIOS Features

- supports Plug and Play V1.0A and DMI 2.0
- supports Intel PCI 2.1 (Peripheral Component Interconnect) local bus specification
- supports EDO (Extended Data Out), ECC and FPM DRAM
- supports ECC (Error Checking and Correction)
- supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120:

- can be used as a boot device
- is accessible as the next available floppy drive

AMIBIOS supports the National Semiconductor LM75 and LM78 data acquisition chips. When a failure occurs in a monitored activity, AMIBIOS can sound an alarm and display a message. The LM75 and LM78 chips monitor:

- CPU temperature
- additional temperature sensors

- chassis intrusion detector input
- watchdog comparison of all monitored values
- POST code storage RAM
- ISA and I²C serial bus interfaces
- up to five positive voltage inputs
- up to two negative voltage inputs
- up to three fan speed monitoring inputs

BIOS Configuration Summary Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

AMIBIOS System Configuration (C) 1985-1994 American Megatrends Inc.,			
Main Processor	: Pentium(tm) II	Base Memory Size	: 640 KB
Math Processor	: Built-In	Ext. Memory Size	: 31744 KB
Floppy Drive A:	: 1.2 MB, 5¼	Display Type	: VGA/EGA
Floppy Drive B:	: 1.44 MB, 3½	Serial Port(s)	: 3F8,2F8
AMI-BIOS Date	: 7/15/95	Parallel Port(s)	: 378
Processor Clock	: 200MHz	Power Management	: APM, SMI

AMIBIOS Setup

See the following page for examples of the AMIBIOS Setup screen, featuring options and settings. Figure 1-1 shows the ***Standard*** option highlighted. To highlight other options, use the arrow keys, or use the tab key to move to other option boxes. Figure 1-2 shows the settings for the Standard setup. Settings can be viewed by highlighting a desired option and pressing <Enter>. Use the arrow keys to choose a setting. Note: Optimal settings for all options can be set automatically. Go to the ***Optimal*** icon in the default box and press <Enter>. Use the arrow keys to highlight *yes,* then press <Enter>.

Figure 1-1. Standard Option Highlighted

Figure 1-2. Settings for Standard Option

Chapter 2
Running Setup*

Optimal and Fail-Safe default settings are bolded in text unless otherwise noted.

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All displayed icons are described in this section, although the screen display is often all you need to understand how to set the option.

2-1 Setup

2-1-1 Standard Setup

Pri Master
Pri Slave
Sec Master
Sec Slave
Choose these icons to configure the hard disk drive. When you click on an icon, the following parameters are listed: *Type, LBA/ Large Mode, Block Mode, 32Bit Mode, and PIO Mode*. All parameters relate to IDE drives except *Type*.

If the hard disk drive to be configured is an IDE drive, select the appropriate drive icon, choose the *Type* parameter and select *Auto*. The BIOS will automatically detect the IDE drive parameters and display them. Click on the OK button to accept these parameters.

Click on *LBA/Large Mode* and choose *On* to enable support for IDE drives with capacities greater than 528MB. Click on *Block Mode* and choose *On* to support IDE drives that use Block Mode. Click on *32Bit Mode* and click on *On* to support IDE drives that permit 32-bit accesses.

To configure an old MFM hard disk drive, you must know the drive parameters (number of heads, number of cylinders, number of sectors, the starting write precompensation cylinder, and drive capacity). Select the hard disk drive type (1-46). Refer to table below.

AMI BIOS Hard Disk Drive Types

Type	Cylinders	Heads	Write Precompensation	Landing Zone	Sectors	Size
1	306	4	128	305	17	10 MB
2	615	4	300	615	17	20 MB
3	615	6	300	615	17	31 MB
4	940	8	512	940	17	62 MB
5	940	6	512	940	17	47 MB
6	615	4	65535	615	17	20 MB
7	462	8	256	511	17	31 MB
8	733	5	65535	733	17	30 MB
9	900	15	65535	901	17	112 MB
10	820	3	65535	820	17	20 MB
11	855	5	65535	855	17	35 MB
12	855	7	65535	855	17	50 MB
13	306	8	128	319	17	20 MB
14	733	7	65535	733	17	43 MB
16	612	4	0	663	17	20 MB
17	977	5	300	977	17	41 MB
18	977	7	65535	977	17	57 MB
19	1024	7	512	1023	17	60 MB
20	733	5	300	732	17	30 MB
21	733	7	300	732	17	43 MB
22	733	5	300	733	17	30 MB
23	306	4	0	336	17	10 MB
24	925	7	0	925	17	54 MB
25	925	9	65535	925	17	69 MB
26	754	7	754	754	17	44 MB
27	754	11	65535	754	17	69 MB
28	699	7	256	699	17	41 MB
29	823	10	65535	823	17	68 MB
30	918	7	918	918	17	53 MB
31	1024	11	65535	1024	17	94 MB
32	1024	15	65535	1024	17	128 MB
33	1024	5	1024	1024	17	43 MB
34	612	2	128	612	17	10 MB
35	1024	9	65535	1024	17	77 MB
36	1024	8	512	1024	17	68 MB
37	615	8	128	615	17	41 MB
38	987	3	987	987	17	25 MB
39	987	7	987	987	17	57 MB
40	820	6	820	820	17	41 MB
41	977	5	977	977	17	41 MB
42	981	5	981	981	17	41 MB
43	830	7	512	831	17	48 MB
44	830	10	65535	830	17	69 MB
45	917	15	65535	918	17	114 MB
46	1224	15	65535	1223	17	152 MB
47	ENTER PARAMETERS PROVIDED WITH HARD DRIVE					

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number for a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of a sector gets progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter is the track number where write precompensation begins.
Landing Zone	This number is the cylinder location where the heads will normally park when the system is shut down.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drive may have even more sectors per track.
Capacity	The formatted capacity of the drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Date and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values through the keyboard.

Floppy A

Floppy B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are ***Not Installed***, *360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch* or *2.88 MB 3½ inch*.

2-1-2 Advanced Setup

Quick Boot
Set this option to Enabled to permit AMIBIOS to boot within 5 seconds. The Settings are ***Disabled*** or *Enabled*.

Pri Master ARMD Emulated as
Pri Slave ARMD Emulated as
Sec Master ARMD Emulated as
Sec Slave ARMD Emulated as
Options for Pri Master ARMD Emulated as, Pri Slave ARMD Emulated as, Sec Master ARMD Emulated as and Sec Slave ARMD Emulated as are ***Auto****, Floppy and Hard disk*.

1st Boot Device
2nd Boot Device
3rd Boot Device
4th Boot Device
The options for 1st Boot Device are *3rd IDE-HDD, 4th IDE-HDD,* ***Floppy****, ARMD-FDD, ARMD-HDD, ATAPI CD ROM, SCSI or Network*. The options for 2nd Boot Device are ***1st IDE-HDD****, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or ATAPI*. The options for 3rd Boot Device are *1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD or* ***ATAPI CD ROM***. The options for the 4th Boot Device are ***Disabled****, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD*. The *Disabled* option in the 4th boot device means that setup will not be considered during the boot process.

1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks than can be installed by the BIOS. 1st IDE-HDD is the first hard disk installed by the BIOS, 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to Primary Slave and another hard disk to Secondary Master, then 1st IDE-HDD will be referred to as the hard disk connected to Primary Slave and 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of the initialization of the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third, and Secondary Slave fourth.

The BIOS will attempt to read the boot record from 1st, 2nd, 3rd and 4th boot device in the selected order until it is successful in reading the booting record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

Try Other Boot Device

This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are ***Yes*** or *No*. If *Yes* is selected and all the selected boot devices failed to boot, the BIOS will try to boot from the other boot devices (in a pre-defined sequence) which are present but not selected as boot devices in the setup (and hence not yet been tried for booting). If selected as *No* and all selected boot devices failed to boot, the BIOS will try not to boot from the other boot devices which may be present but not selected as boot devices in setup.

Initial Display Mode

This option determines the display screen with which the POST is going to start the display. The settings for this option are ***BIOS*** or *Silent*. If selected as *BIOS,* the POST will start with the normal sign-on message screen. If *Silent* is selected, the POST will start with the silent screen.

Display Mode at Add-on ROM Init

This option determines the display mode during add-on ROM (except Video add-on ROM) initialization. The settings for this option are ***Force BIOS*** or *Keep Current*. If selected as *Force BIOS,* the POST will force the display to be changed to BIOS mode before giving control to any add-on ROM. If no add-on ROM is found, then the current display mode will remain unchanged even if this setup question is selected as *Force BIOS.* If selected as *Keep Current,* then the current display mode will remain unchanged.

Floppy Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

Hard Disk Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

S.M.A.R.T. for Hard Disks

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of the hard disk

by predicting future device failures. The hard disk needs to be S.M.A.R.T. capable. The settings for this option are ***Disabled*** or *Enabled*. ***Note: SMART cannot predict all future device failures. SMART should be used as a warning tool, not as a tool to predict the device reliability.***

Boot Up Num-Lock
Settings for this option are ***On*** or *Off*. When this option is set to *On*, the BIOS turns off the Num Lock key when the system is powered on. This will enable the end user to use the arrow keys on both the numeric keypad and the keyboard.

PS/2 Mouse Support
Settings for this option are ***Enabled*** or *Disabled*. When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse.

Primary Display
This option specifies the type of display adapter card installed in the system. The settings are *Absent,* ***VGA/EGA***, *CGA40x25*, *CGA80x25* or *Mono*.

Password Check
This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if WinBIOS Setup is executed.

Boot to OS/2
If DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are ***No*** or *Yes*.

CPU MicroCode Updation
The settings for this option are *Disabled* or ***Enabled***. Set this option to *Enabled* to allow the CPU microcode to be updated online at any time.

Internal Cache
This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled, WriteThru* or ***WriteBack***.

System Bios Cacheable
AMIBIOS always copies the system BIOS from ROM to RAM for faster execution. The settings are *Disabled* or ***Enabled***. *Note: the Fail-Safe default setting is* ***Disabled****.* Set this option to *Enabled* to permit the contents of F0000h RAM memory segment to be written to and read from cache memory.

C000, 16K Shadow
C400, 16K Shadow
These options specify how the contents of the video ROM are handled. The settings are: *Disabled*, *Enabled or* ***Cached***. When set to *Cached*, the contents of the video ROM area from C0000h-C7FFFh are not only copied from ROM to RAM, the contents of the C0000h-C7FFFh RAM can be written to or read from cache memory.

C800, 16K Shadow
CC00, 16K Shadow
D000, 16K Shadow
D400, 16K Shadow
D800, 16K Shadow
DC00, 16K Shadow
These options specify how the contents of the adaptor ROM named in the option title are handled. The ROM area that is not used by ISA adapter cards will be allocated to PCI adapter cards. The settings are: ***Disabled****, Enabled or Cached*.

2-1-3 Chipset Setup

USB Function
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB (Universal Serial Bus) functions.

USB KB/Mouse Legacy Support
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB keyboard and mouse.

SDRAM Autosizing Support
If the Serial Presence Detect (SPD) is not available, then the BIOS will try to detect the memory and do the autosizing. The settings for this option are ***Auto****, Enabled* or *Disabled*.

EDO DRAM Speed (ns)
This option should be set according to the speed of the EDO DRAM in the system. The value of this option determines how the EDO DRAM timings should be programmed in the chipset. The settings for this option are ***Auto****, Manual*, *50, 60* or *70*.

EDO Read Burst Timing
Burst mode EDO have internal column counters. Because of this, they do not need to accept row addresses and starting column addresses from the EDO memory controller. This eliminates the setup and hold time for the second and subsequent column addresses. It also improves the EDO Read access time. The settings for this option are ***x333*** or *x222*.

EDO Write Burst Timing
Burst mode EDO have internal column counters. Because of this, they do not need to accept row addresses and starting column addresses from the EDO memory controller. This eliminates the setup and hold time for the second and subsequent column addresses. It also improves the EDO Write access time. The settings for this option are ***x333*** or *x222*.

EDO RAS Precharge
Memory needs to be recharged to ensure the information stored is not lost. This feature eliminates the RAS (Row Address Strobe) recharge time since memory must always be addressed in the order of Row first, then Column. The settings for this option are ***4 Clks*** or *3 Clks*.

EDO RAS to CAS
As previously described, memory must always be addressed in the order of Row, then Column. The EDO RAS to CAS feature sets the timing delay between Row addressing and Column addressing. The settings for this option are ***3 Clks*** or *2 Clks*.

MA Waitstate
Use this feature to configure the memory address wait state. The settings for this option are ***Slow*** or *Fast*.

SDRAM Timing Latency
Use this feature to select the SDRAM timing delay. The settings for this option are *Manual* or ***Auto***.

SDRAM RAS to CAS
The settings for this option are ***3 Clks*** or *2 Clks*.

SDRAM CAS Lat
This feature is for the Column Address Strobe latency. The settings for this option are ***3 Clks*** or *2 Clks*.

SDRAM RAS Precharge
This feature is for the SDRAM Row Address Strobe delay. The settings for this option are ***3 Clks*** or *2 Clks*.

VGA Frame Buffer USWC
USWC is a memory cycle type that stands for Uncacheable Speculative Write Combining. The settings are: ***Disabled*** or *Enabled*.

PCI Frame Buffer USWC
The settings for this option are: ***Disabled*** or *Enabled*. When *Enabled,* the PCI frame buffer address and length are divided into 2. The value is then programmed into the processor Variable MTRR (3) with the value for USWC (01h).

DRAM Integrity Mode (ECC)
The settings for this option are: ***Non ECC***, *EC only* or *ECC*. Set this option to *Enabled* to enable ECC DRAM integrity mode. ECC allows critical system to detect and correct memory errors, while normal parity generator/checker can only detect such memory errors.

Fixed Memory Hole
This option allows a memory hole to be specified for either the 512-640K region or the 15-16M region. The settings for this option are ***Disabled***, *512-640KB* or *15-16MB*.

Type F DMA Buffer Control 1
Type F DMA Buffer Control 2
Instead of 8 sysclock, Type F DMA only requires 3 sysclock to finish the data transfer. These two options are device dependent. The settings are *Channel 0*, *Channel 1, Channel 2,* ***Disabled****, Channel 3, Channel 5, Channel 6 or Channel 7.*

DMA-0 Type
DMA-1 Type
DMA-2 Type
DMA-3 Type
DMA-5 Type
DMA-6 Type
DMA-7 Type
The settings for these Direct Memory Access channels are ***Normal ISA***, *PC/PCI* or *Distributed*.

AGP Aperture Size
This register determines the effective size of the Graphics Aperture used in the particular PAC configuration. This register can be updated by the PAC-specific BIOS configuration sequence before PCI standard bus enumeration sequence takes place. If the register is not updated, a default value selects aperture of maximum size (i.e., 256 MB). The settings are: *4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB* or ***256 MB***.

System Type
The settings are: ***Auto****, DP* or *UP*.

USWC Write I/O Post
Use this feature for the WC Write Post During I/O Bridge Access Enable (WPIO). When set to *Enabled,* posting of WC transactions to PCI occur, even if the I/O bridge has been granted access to the PCI bus via corresponding arbitration and buffer management protocol. USWC Write posting should only be enabled if a USWC region is located on the PCI bus. The settings are: ***Auto****, Disabled* or *Enabled*.

MAA 1:0 Buf. Strength
MECC Buf. Strength
MD Buf. Strength
RCSA0/RCSB0 Buf. Strength
MAB 1:0 Buf. Strength

MAA 13.2 Bufl Strength
RCSA1/RCSB1 Buf. Strength
RCSA2/RCSB2 Buf. Strength
RCSA3/RCSB3 Buf. Strength
RCSA4/RCSB4 Buf. Strength
CDQB 5,1 Buf. Strength
CDQA 5,1 Buf. Strength
CDQA 0, 2:4, 6:7 Buf. Strength
RCSA5/RCSB5 Buf. Strength
RCSA6/RCSB6 Buf. Strength
RCSA7/RCSB7 Buf. Strength
The above features control the memory buffer strength. They are used to program the various DRAM interface signal buffer strengths, based on memory configuration, DRAM type (EDO or SDRAM), DRAM density (x4, x8, x16, or x32), DRAM technology (16 Mb or 64 Mb), and rows populated. *Note the Optimal and Fail-Safe default settings are* ***Auto.***

PAC Bus SERR#
The settings for this option are: *Disabled* or ***Enabled***. When set to *Enabled*, the PAC's SERR# signal driver is enabled and SERR# is asserted for all relevant bits set in the ERRSTS and PCISTS as controlled by the corresponding bits of the ERRCMD register. When *Disabled*, SERR# is never driven by the PAC.

AGP Common SERR#
The settings are: *Disabled* or ***Enabled***. Set to *Enabled* to permit a common SERR# signal for AGP and the standard PCI bus.

AGP System Error Forwarding
The settings are: *Disabled* or ***Enabled***. Set this option to *Enabled* to enable AGP systems errors to be forwarded.

AGP Parity Error Response
The settings are: *Disabled* or ***Enabled***. Set this option to *Enabled* to enable AGP parity error response.

IRQ12
The settings are: ***Auto****, Standard* or *Mouse*. When this option is set to *Auto* the AMIBIOS automatically determines how IRQ12 should be allocated. In the *Standard* setting IRQ12 is made available for use on the ISA bus. IRQ12 is used by the PS/2 Mouse, when in *Mouse* setting.

PIIX4 SERR#
Use this feature for the SERR# generation due to delayed transaction time-out enable. The settings are: ***Disabled*** or *Enabled*.

USB Passive Release Enable
The settings for this option are: *Disabled* or ***Enabled***. When set to *Enabled,* it allows the PIIX4 to use Passive Release while transferring control information or data for USB transactions. When *Disabled,* PIIX4 will perform PCI accesses for USB without using Passive Release.

PIIX4 Passive
Use the PIIX4 Passive feature to enable the Passive Release mechanism encoded on the PHOLD# signal when PIIX4 is a PCI master. The settings are: *Disabled* or ***Enabled***.

PIIX4 Delayed Transaction
Use this feature to enable the Delayed Transaction mechanism when the PIIX4 is the target of a PCI transaction. The settings are: *Disabled* or ***Enabled***.

Master Lat. Timer
Master Latency Timer is an 8-bit register that controls the amount of time the PAC, as a PCI bus master, can burst data on the PCI bus. The count value is an 8 bit quantity. However, MLT[2:0] are 0 when determining the count value. The PAC's MLT is used to guarantee to the PCI agents (other than PAC) a minimum amount of the system resources. *Note: Settings are in increments with an Optimal and Fail-Safe default setting of* ***40H****.*

MTT
Multi-Transaction Timer is an 8-bit register that controls the amount of time that the PAC's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. The PAC's MTT mechanism is used to guarantee the fair share of the PCI bandwidth to an initiator that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it cannot use long burst transfers). *Note: Settings are in increments with an Optimal and Fail-Safe default setting of* ***20H***.

2-1-4 Power Management

ACPI Aware OS
Use this feature if your operating system supports Microsoft's Advanced Configuration and Power Interface (ACPI) standard. The settings are: *Yes* or ***No***.

Power Management/APM
This power conservation feature is specified by Intel and Microsoft INT 15h Advance Power Management BIOS functions. The settings are: ***Disabled*** or *Enabled*. When this feature is set to *Enabled,* the system power conservation features are controlled by the system BIOS, not by the operating system.

Power Button Function
This feature is used to select the functionality of the power supply's power button. The settings are: *Suspend* or ***On/Off***.

Power Supply Type
The settings for power supply type are ***AT*** *or ATX.*

Instant on Support
Instant-on is one of ACPI's standard features. The system comes back on instantly from ACPI's SoftOff state. The settings are: ***Disabled*** or *Enabled*.

Green PC Monitor Power State
This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power savings state after the specified period of display inactivity has expired. The settings are ***Standby***, *Suspend* or *Off*.

Video Power Down Mode
This option specifies the power conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby*, or ***Suspend***.

Hard Disk Power Down Mode
This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled*, *Standby*, or ***Suspend***.

Hard Disk Timeout (Minute)
This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters power-conserving state specified in the Hard Disk Power Down Mode option. The settings are ***Disabled*** and *1 Min through 15 Min in 1 minute intervals*.

Standby/Suspend Timer Unit
This allows you to set the standby time out and suspend time out timer unit. The settings are *32 secs*, *4 msecs*, ***4 min*** or *4 secs.*

Standby Time Out
This option specifies the length of a period of system inactivity while in full power on state. When this length of time expires, the computer enters standby power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Suspend Timeout (Minutes)
This option specifies the length of a period of system inactivity while in standby state. When this length of time expires, the computer enters suspend power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Slow Clock Ratio
The value of the slow clock ratio indicates the percentage of time the STPCLK# signal is asserted while in the thermal throttle mode. The settings are ***Disabled****, 12.5%*, *25%*, *37.5%*, *50%*, *62.5%*, *75%*, and *87.5%*.

Display Activity
This option specifies if AMIBIOS is to monitor display activity for power conservation purposes. When this option is set to *Monitor* and there is no display activity for the length of time specified in the Standby Timeout (Minute) option, the computer enters a power savings state. The settings are *Monitor* or ***Ignore***.

Device 6 (Serial port 1)
Device 7 (Serial port 2)
Device 8 (Parallel port)
Device 5 (Floppy disk)
Device 0 (Primary Master IDE)
Device 1 (Primary Slave IDE)
Device 2 (Secondary Master IDE)

Device 3 (Secondary Slave IDE)
These options are for event monitoring. The settings for each of these options are Monitor or ***Ignore***.

LAN Wake-Up
RTC Wake-UP
Hour
Minute
Options for LAN Wake-Up and RTC Wake-Up are ***Disabled*** and *Enabled*. *Note: The optimal setting for Hour and Minute is* ***N/A****.* There is no fail-safe setting for *Hour* and *Minute.*

2-1-5 PCI/PnP Setup

Plug and Play-Aware OS
The settings for this option are *Yes* or ***No***. Set this option to *Yes* if the operating system in the computer is aware of and follows the Plug and Play specification. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. Currently, only Windows 95 is PnP-Aware. Set this option to *No* if the operating system (such as DOS, OS/2, Windows 3.x) does not use PnP. You must set this option correctly. Otherwise, PnP-aware adapter cards installed in the computer will not be configured properly.

PCI Latency Timer (PCI Clocks)
This option specifies the latency timings in PCI clocks for all PCI devices. The settings are *32*, ***64***, *96*, *128*, *160*, *192*, *224*, or *248*.

PCI VGA Palette Snoop
The settings for this option are ***Disabled*** or *Enabled.* When set to *Enabled,* multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example: if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is only directed to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette regis-

ters of both devices to be identical. This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping.

PCI IDE Busmaster
The settings are: ***Disabled*** or *Enabled*.

Offboard PCI IDE Card
This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are ***Auto*** (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4, Slot 5* or *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ
Offboard PCI IDE Secondary IRQ
These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are ***Disabled***, *Hardwired*, *INTA*, *INTB*, *INTC*, or *INTD*.

PCI Slot1 IRQ Priority
PCI Slot2 IRQ Priority
PCI Slot3 IRQ Priority
PCI Slot4 IRQ Priority
These options specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are ***Auto****, (IRQ) 3, 4, 5, 7, 8, 10, and 11, in priority order****.***

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7
These DMA channels control the data transfers between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are ***PnP*** or *ISA/EISA.*

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
These options specify which bus the specified IRQ line is used on and allow you to reserve IRQs for legacy ISA adapter cards. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an ISA/EISA setting to it. Onboard I/O is configured by AMIBIOS. All IRQs used by onboard I/O are configured as PCI/PnP.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to ISA/EISA and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is because at least one IRQ must be available for PCI and PnP devices. The settings are ***PCI/PnP*** or *ISA/EISA.*

Reserved Memory Size
This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are ***Disabled***, *16K*, *32K,* or *64K*.

Reserved Memory Address
This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C0000*, *C4000*, *C8000*, *CC000*, *D0000*, *D4000*, ***D8000***, or *DC000*.

2-1-6 Peripheral Setup

OnBoard FDC
This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are ***Auto*** (AMIBIOS automatically determines if the floppy controller should be enabled), *Disabled*, or *Enabled*.

OnBoard Serial Port 1
This option specifies the base I/O port address of serial port 1. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h*, *2F8h*, *3E8h*, or *2E8h*.

OnBoard Serial Port 2
This option specifies the base I/O port address of serial port 2. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h*, *2F8h*, *3E8h*, or *2E8h*.

Serial Port 2 Mode
The settings are ***Normal***, *Sharp-IR, IrDA,* or *TV Remote.*

IR Duplex Mode
The settings are *Half* or *Full. Note: The Optimal and Fail-Safe default settings are* ***N/A***.

IR Receiver Pin
The settings are *IRRX1* or *IRRX2. Note: The Optimal and Fail-Safe default settings are* ***N/A***.

OnBoard Parallel Port
This option specifies the base I/O port address of the parallel port on the motherboard. The settings are ***Auto*** (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *378*, *278*, or *3BC*.

Parallel Port Mode
This option specifies the parallel port mode. The settings are *Normal*, ***Bi-Dir***, *EPP* or *ECP*. When set to *Normal,* the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication.

EPP Version
The settings are *1.7* or *1.9. Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

Parallel Port IRQ
This option specifies the IRQ to be used by the parallel port. The settings are ***Auto***, *5* or *7*.

Parallel Port DMA Channel
This option is only available if the setting of the parallel port mode option is ECP. The settings are *0*, *1*, *2*, *3*, *5*, *6* or *7*. *Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

OnBoard IDE
This option specifies the onboard IDE controller channels to be used. The settings are *Disabled, Primary*, *Secondary*, or ***Both***.

OnBoard NAT307 Mode Set
The settings for this option are ***Non-PnP*** and *PnP*.

OnBoard SCSI
Enable the OnBoard SCSI feature to use the onboard SCSI on the motherboard. The settings are *Disabled* or *Enabled*. *Note: The Optimal and Fail-Safe default settings are* ***N/A****.*

Remote Power On
Microsoft's Memphis OS supports this feature which can wake-up the system from SoftOff state through devices (such as an external modem) that are connected to COM1 or COM2. The settings are ***Disabled*** or *Enabled*.

AC Power Lost Restart: Disabled
The settings for this option are ***Disabled***.

CPU Current Temperature
The current CPU temperature is displayed in this option.

CPU Overheat Warning Temperature
Use this option to set the CPU overheat warning temperature. The settings are *25 ◦C through 75 ◦C in 1 ◦C intervals*. *Note: The Optimal and Fail-Safe default settings are* ***55 ◦C***.

CPU Overheat Clock Down
The CPU internal clock will slow down to the specified frequency percentage when it is overheated. The settings are ***Disabled***, *12.5%, 25%, 37.5%, 50%, 62.5%, 75%* or *87.5%*.

LM78 In0 (CPU 1)
LM78 In1 (CPU 2)
LM78 In2 (+3.3V)
LM78 In3 (+5V)
LM78 In4 (+12V)
LM78 In5 (-12V)
LM78 In6 (-5V)
CPU1 Fan
CPU2 Fan
Chassis Fan
The above features are for the onboard National Semiconductor's LM 78 System Hardware Monitor used for PC health monitoring. The motherboards with LM 78 have seven onboard voltage monitors for the CPU core, CPU I/O, +3.3V, +5V, -5V, +12V, and -12V, and three fan status monitors.

2-2 Security Setup

2-2-1 Supervisor User

The system can be configured so that all users must enter a password every time the system boots or when the WINBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing the password on the keyboard, selecting each letter via the mouse, or selecting each letter via the pen stylus. Pen access must be customized for each specific hardware platform.

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must drain CMOS RAM and reconfigure.

2-2-2 Anti-Virus

When this icon is selected, AMIBIOS issues a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. The settings are *Enabled* or ***Disabled***.

2-3 Utility Setup

2-3-1 Language

Note: The Optimal and Fail-Safe default settings for this option are ***English****.*

2-3-2 Detect IDE

Use this icon to let the BIOS autodetect the IDE hard drive.

2-4 Default Setting

Every option in WinBIOS Setup contains two default settings: a Fail-Safe default, and an Optimal default.

2-4-1 Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

2-4-2 Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Appendix A
BIOS Error Beep Codes

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Non-fatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. ***Please Note:*** This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.
11	Cache memory bad - do not enable cache	The cache memory test failed. Cache memory is disabled. ***Do not press <Ctrl>+<Alt>+<Shift> and <+> to enable cache memory.***

Refer to the table on page A-3 for solutions to the error beep codes.

If it beeps...	**then ...**
1, 2, 3 times	reseat the memory SIMMs or DIPs. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
11 times	reseat the cache memory on the motherboard. If it still beeps, replace the cache memory.
4, 5, 7, or 10 times	the motherboard must be replaced.

Appendix B

AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-tests (POST) port 80 codes for the AMI BIOS.

Check Point	Description
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
OB	Next, performing any required initialization before keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.

Check Point	Description
11	Next, checking if the <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or the <End> key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and perfoming any necessary configuration before initializing the interrupt vectors.
24	The configuration required before interrupt vector initialization has completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting video mode will be done next.
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.

Check Point	Description
2A	Bus initialization system, static, output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.
38	Initializing the bus input, IPL, and general devices next, if present.
39	Displaying bus initialization error messages.

Check Point	Description
3A	The new cursor position has been read and saved. Displaying the Hit <DEL> message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB memory next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.

Check Point	Description
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity, and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59	The Hit <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and interrupt controller test next.
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.

Check Point	Description
62	The DMA controller 1 base register test passed. Performing the DMA controller 2 base register test next.
65	The DMA controller 2 base register test passed. Programming DMA controllers 1 and 2 next.
66	Completed programming DMA controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.

Check Point	Description
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.

Check Point	Description
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the Coprocessor test next.
9C	Required initialization before the Coprocessor test is over. Initializing the Coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the Coprocessor test next.
9E	Initialization after the Coprocessor test is complete. Checking the extended keyboard, keyboard ID, and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h completed. Passing control to the adaptor ROM at E000h next.
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.

Check Point	Description
AA	Initialization after E000 option ROM control has completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
B0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.