SUPER®

SUPER P6DGH

USER'S AND BIOS

MANUAL

Revision 1.0

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Preface

About This Manual

This manual is written for system houses, experienced PC technicians and knowledgeable PC end users. It provides information for the installation and use of the SUPER P6DGH motherboard. The SUPER P6DGH supports Pentium II 233-450 MHz Slot 1 processors.

The Pentium II processor with Dual Independent Bus Architecture is housed in a new packaging technology called the Single Edge Contact Cartridge (S.E.C.C.). This new cartridge package and its associated "Slot 1" infrastructure will provide the headroom for future high-performance processors.

Manual Organization

Chapter 1, Introduction, describes the features, specifications and performance of the SUPER P6DGH system board, provides detailed information about the chipset, and offers warranty information.

Refer to Chapter 2, Installation, for instructions on how to install the Pentium II processor, the retention mechanism and the heat sink support. This chapter also provides you with instructions for handling static-sensitive devices. Read this chapter when you want to install or remove SIMM/DIMM memory modules and to mount the system board in the chassis. Also refer to this chapter to connect the floppy and hard disk drives, IDE interfaces, and the parallel and serial ports as well as the cables for the power supply, the reset cable, the Keylock/Power LED, the speaker and the keyboard.

If you encounter any problems, please see Chapter 3, Troubleshooting, which describes troubleshooting procedures for the video, the memory and the setup configuration stored in memory. Instructions are also included for contacting a technical assistance support representative, returning merchandise for service and visiting our website for BIOS upgrades.

See Chapter 4 for configuration data and the AMIBIOS features. Chapter 5 covers the WinBIOS setup options.

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Chapter 1
Introduction

1-1 Overview

The SUPER P6DGH supports dual Pentium II 233-450 MHz processors. This motherboard is based on Intel's 440GX chipset, which enables a 100 MHz system bus speed, an Accelerated Graphics Port (AGP), Wake-on-LAN™, SDRAM, concurrent PCI and an Ultra DMA 33 MB/s burst data transfer rate. In addition, the SUPER P6DGH is I_2O™–ready with a built-in 66MHz Intel i960® RD I/O processor.

The motherboard is Full AT size (13.2" x 12.2"). The SUPER P6DGH provides 9 PCI slots, 2 ISA slots and an Accelerated Graphics Port. It can accommodate a total of 2 GB registered DIMM or EDO supported (66Mhz), or 1 GB SDRAM memory with 4 168-pin DIMM sockets.

AGP reduces contention between the CPU and I/O devices by broadening the bandwidth of graphics to memory. It delivers a maximum of 532 MB/s 2x transfer mode, which is quadruple the PCI speed!

The I_2O architecture of the SUPER P6DGH consists of a 66 MHz i960 RD I/O processor, an 8 Mb Flash I/O BIOS and local IOP memory (optional) of up to 64 MB in 2 72-pin SIMMS. The I_2O architecture provides a standard way to off-load the I/O functions from the CPU, creating a direct I/O pipeline that no longer passes through the host processor. Besides delivering increased system performance, the I_2O specification eliminates the need for different drivers for each combination of operating system and SCSI or Network Interface Card. Because the drivers may be standardized and not rewritten for new operating system releases, they can become more highly optimized and robust to improve performance and reliability in mission-critical enterprise computing.

To attain portability across multiple operating systems and host platforms, I_2O drivers are divided into the OS Services Module (OSM) and the Hardware Device Module (HDM). The first module interfaces with the host operating system. The second interfaces with the particular device, media or server managed by the driver. The two modules interface with each other through a two-layered communications system. A Message Layer sets up a communications session and a Transport Layer defines how information will be shared. The Message Layer resides on the Transport Layer.

The i960 RD I/O processor (IU20) is a highly integrated, intelligent I/O subsystem on a chip. Mode 3 is the default setting for normal I_2O operation. The i960 RD has two main functions. As a local processor, it off-loads interrupt-intensive I/O tasks from the host CPU. Its architecture is composed of a RISC core surrounded by peripherals essential to the I/O function. The onboard PCI-to-PCI bridge enables designers to connect I/O components directly to the PCI bus and to also add additional PCI slots. The bridge improves overall system performance by reducing bus traffic.

Wake-on-LAN allows for remote network management and configuration of the PC, even in off-hours when the PC is turned off. This reduces the complexity of managing the network.

Other features that maximize simplicity in managing the computer are PC 98-ready and support for an Advanced Configuration and Power Interface (ACPI). With PC Health Monitoring, you can protect your system from problems before they even occur.

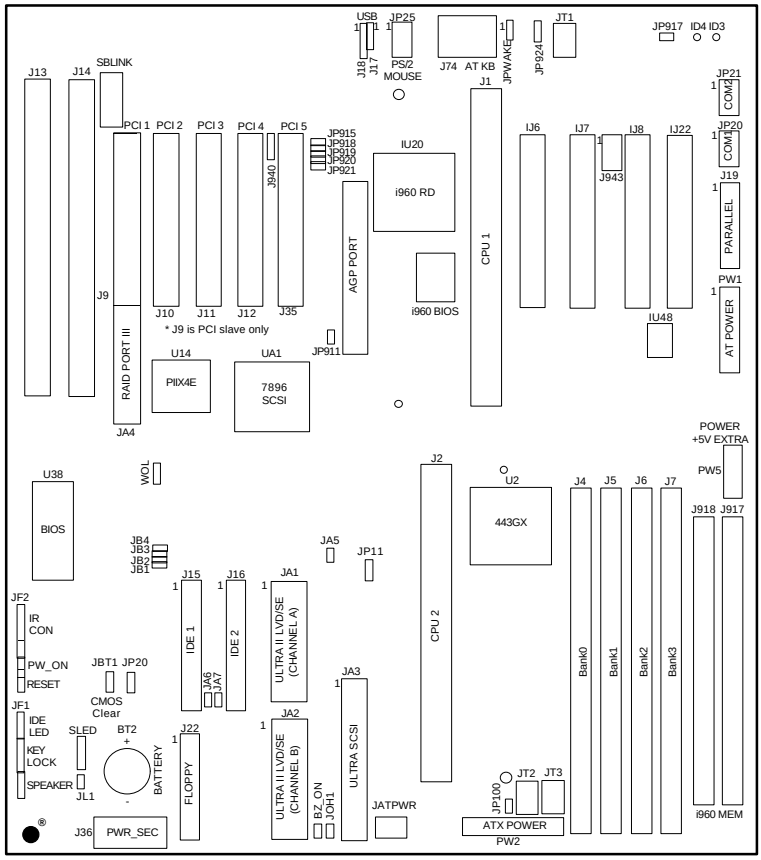
Included in the I/O are 2 EIDE ports, a floppy port, an ECP/EPP parallel port, a PS/2 mouse port, 2 serial ports (including an infrared port) and 2 USB ports. The SUPER P6DGH has an onboard Adaptec 7896 dual-channel Ultra II LVD (Low Voltage Device) SCSI controller with a data transfer rate of up to 80 MB/s. This supports the Adaptec ARO-1130CA2 RAIDport III card for increased I/O performance and fault tolerance. The boards come with a CD that includes such software utilities as the SUPERMICRO PIIX4 Upgrade

Utility for Windows® 95, a BIOS Flash Upgrade Utility, a DMI Browser for Windows 95/98, a DMI Wizard, the SUPERMICRO SUPER Doctor Utility ver 1.31a and Intel's® LANDesk® Client Manager for Windows NT® and Windows 95/98® (optional).

SUPER P6DGH

Figure 1-1. SUPER P6DGH Motherboard Image

Figure 1-2. P6DGH Motherboard Layout



——— Primary Jumper Settings ———

BZ_ON: ON (default)
JA5: ON
JA6: ON
JA7: ON
JBT1: 1-2 (default)
2-3 CMOS Clear
JL1: OFF (default)
JP11: 1-2 Auto (default)
2-3 66 Mhz
OFF 100 Mhz
JP20: 1-2 PIIX4 CTL
2-3 Save PD State (default)
JP911: ON
JP917: ON
JP924: 1-2

———————————————

CPU Core/ Bus Ratio	JB1	JB2	JB3	JB4
3.0	ON	OFF	ON	ON
3.5	OFF	OFF	ON	ON
4.0	ON	ON	OFF	ON
4.5	OFF	ON	OFF	ON
5.0	ON	OFF	OFF	ON
5.5	OFF	OFF	OFF	ON
6.0	ON	ON	ON	OFF

i960 Initialization Jumper Defaults (See page 2-21.)

JP915 OFF
JP918 ON (Mode 0)
JP919 ON (Mode 0)
JP920 OFF (Enable 960)
JP921 ON (Disable BIST)

———————————————

SUPER P6DGH Features

The following list covers the general features of the SUPER P6DGH.

CPU
- Dual Pentium II 233-450 MHz processors

I_2O-Ready
- 66 MHz i960 RD I/O processor
- Up to 64 MB Local IOP memory
- 8 MB Flash I/O BIOS

Memory
- 2 GB Registered DIMM or EDO, or 1 GB SDRAM
- Error Checking and Correction and Parity Checking support

Chipset
- Intel 440GX

Expansion Slots
- 9 PCI slots
- 2 ISA slots
- 1 AGP slot

BIOS
- 2 MB AMI® Flash BIOS
- DMI 2.0, Plug and Play (PnP)

PC Health Monitoring (781D)
- Seven onboard voltage monitors for CPU cores, +3.3V, ±5V and ±12V
- Three fan-status monitors with firmware/software on/off control
- Chassis temperature monitor and control
- CPU fan auto-off in sleep mode
- System overheat control and alarm
- Chassis intrusion detection
- System resource alert
- Hardware BIOS virus protection
- Switching voltage regulators for the CPU core
- SUPERMICRO SUPER Doctor and Intel LANDesk Client

Manager (LDCM) support

ACPI/PC 98 Features

- Microsoft® OnNow
- Slow blinking LED for sleep-state indicator (ATX power only)
- BIOS support for USB keyboard
- Real-time clock wake-up alarm (ATX power only)
- Main switch override mechanism (ATX power only)
- External modem ring-on (wake-on-ring) (ATX power only)

Onboard I/O

- Two 68-pin 16-bit Ultra II LVD/SE SCSI connectors and one 50-pin 8-bit Ultra SCSI connector
- RAIDport for Adaptec ARO-1130CA2 RAIDport III card
- Two EIDE Bus Master interfaces that support Ultra DMA/33 and Mode 4
- One floppy interface
- Two UART 16550A serial ports
- One parallel port that supports both EPP (Enhanced Parallel Port) and ECP (Extended Capabilities Port)
- PS/2 mouse port
- Infrared port
- Two USB ports

CD Utilities

- Intel LANDesk Client Manager for Windows NT® and Windows® 95 (optional)
- PIIX4 Upgrade Utility for Windows 95
- BIOS Flash Upgrade Utility
- SUPER Doctor Utility
- SCSI Utility, manual and driver

Dimensions

- Full AT size (13.2" x 12.2")

1-2 PC Health Monitoring

This section describes the PC health monitoring features of the SUPER P6DGH. It has an onboard Winbond 781D System Hardware Monitor chip that supports PC health monitoring.

Seven Onboard Voltage Monitors for the CPU Cores, +3.3V, ±5V, and ±12V

The onboard voltage monitors scan seven voltages every second. When running SUPER Doctor or Intel LDCM, once a voltage becomes unstable, a warning or an error message will be reported on-screen. Users can adjust the threshold of the monitored voltage to determine the sensitivity of the voltage monitor.

Three Fan-Status Monitors with Firmware/Software On/Off Control

The PC health monitor can check the RPM status of the cooling fans. The onboard 3-pin CPU fans are controlled by the ACPI BIOS and the ACPI-enabled operating system. The thermal fan is controlled by the overheat detection logic.

Chassis Temperature Control

The thermal control sensor monitors the real-time chassis temperature. It will turn on the backup fan whenever the chassis temperature exceeds a user-defined threshold. The overheat circuitry runs independently from the CPU. It can still monitor for overheat conditions even if the CPU is in sleep mode. Once it detects that the chassis temperature is too high, it will automatically turn on the backup fan and trigger the overheat LED (JOH1) and the overheat buzzer (BZ_ON). The onboard chassis thermal circuitry can monitor the overall system temperature and alert users when the chassis temperature gets too high.

CPU Fan Auto-Off in Sleep Mode

The CPU fan(s) runs when the power is on, but can be turned off when the CPU is in sleep mode. When in sleep mode, the CPU does not run at full power and therefore generates less heat. For power saving purposes, the user has the option of shutting down the CPU fan(s) at such times.

System Overheat Alarm and LED

This feature is available when used with SUPERMICRO's SUPER Doctor Utility. The program will generate a beep sound via the speaker when it detects a system overheat condition. The overheat condition can be defined by the user. The program can also give an on-screen indication when the system overheats.

Chassis Intrusion Detection

The chassis intrusion circuitry can detect unauthorized intrusion to the system. The chassis intrusion connector is located on JL1. Attach a microswitch to JL1. When the microswitch is closed, it means that the chassis has been opened. The circuitry will then alert the user with a warning message when the system is turned on. This circuitry uses the onboard battery for power.

System Resource Alert

This feature is available when used with the Intel LANDesk Client Manager. It is used to notify the user of certain system events. For example, if the system is running low on virtual memory, there might not be enough hard drive space to save the data. LDCM will then alert the user of the potential problem.

Hardware BIOS Virus Protection

The system BIOS is protected by hardware so that no virus can infect the BIOS area. The user can only change the BIOS content through the flash utility provided by SUPERMICRO. This feature can prevent viruses from infecting the BIOS area and destroying valuable data.

Switching Voltage Regulator for the CPU Core

The switching voltage regulator for the CPU core can support current up to 20A with the auto-sensing voltage ID ranging from 1.8V to 3.5V. This will allow the regulator to run cooler and thus make the system more stable.

Intel LANDesk Client Manager (LDCM) Support

As the computer industry grows, PC systems have become more complex and harder to manage. Historically, only experts have been able to fully understand and control these complex systems. Today's users want manageable systems that they can interact with automatically. Client Manager enables both administrators and clients to:

- Review system inventory
- View DMI-compliant component information
- Back up and restore system configuration files
- Troubleshoot
- Receive notifications of system events
- Transfer files to and from client workstations
- Remotely reboot client workstations

1-3 ACPI/PC 98 Features

ACPI stands for Advanced Configuration and Power Interface. The ACPI specification defines a flexible and abstract hardware interface that provides a standard way to integrate power management features throughout a PC system, which includes its hardware, the operating system and application software. This enables the system to automatically turn on and off peripherals such as CD-ROMs, network cards, hard disk drives and printers. This also includes consumer devices connected to the PC such as VCRs, TVs, telephones and stereos.

In addition to enabling operating system-directed power management, ACPI provides a generic system event mechanism for Plug and Play and an operating system-independent interface for configuration control. ACPI leverages the Plug and Play BIOS data structures while providing an architecture-independent processor implementation that is compatible with both Windows 95 and Windows NT.

Microsoft OnNow

The OnNow design initiative is a comprehensive, system-wide approach to system and device power control. OnNow is a term for a PC that is always on but appears to be off and that can respond immediately to user or other requests.

Slow Blinking LED for Sleep-State Indicator

When the CPU goes into a sleep state, the power LED will start blinking to indicate that the CPU is in sleep mode. When the user presses any key, the CPU will wake-up and the LED will automatically stop blinking and remain on.

BIOS Support for USB Keyboard

If the USB keyboard is the only keyboard in the system. It will work like a normal keyboard during system boot-up.

Real-Time Clock Wake-up Alarm (ATX power only)

Although the PC is perceived to be off when not in use, it is still capable of responding to wake-up events according to a scheduled date and time. The user can set a timer to wake-up or shutdown the system at some predetermined time.

Main Switch Override Mechanism (ATX power only)

When an ATX power supply is used, the power button can function as a system suspend button. When the user presses the power button, the system will enter a SoftOff state. The monitor will be suspended and the hard drive will spin down. Pressing the power button again will cause the whole system to wake-up. During the SoftOff state, the ATX power supply provides power to keep the required system circuitry alive. If the system malfunctions and you want to turn off the power, just press and hold the power button for approximately 4 seconds. The power will turn off and enter the SoftOff state.

External Modem Ring-On (ATX power only)

Wake-up events can be triggered by a device (such as an external modem ringing) when BIOS enables this function and the system is in the SoftOff state.

1-4 Chipset Overview

The 440GX chipset developed by Intel is the ultimate processor platform targeted for 3D graphics and multimedia applications. Along with System-to-PCI bridge integrated with optimized DRAM control-

ler and data path, the chipset supports the Accelerated Graphics Port (AGP) interface. AGP is a high performance, component level interconnect targeted at 3D applications and is based on a set of performance enhancements to PCI. The I/O subsystem portion of the 440GX platform is based on the PIIX4, a highly integrated version of Intel's PCI-to-ISA bridge family.

The PCI/AGP and system bus interface controller (82443GX) supports up to two Pentium II processors. It provides an optimized 72-bit DRAM interface (64-bit data plus ECC). This interface supports 3.3V DRAM technologies. The controller provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with the PCI Rev 2.1 Specification. The AGP interface is based on AGP Specification Rev 1.0. It can support up to 133 MHz (532 MB/s) data transfer rates.

1-5 Wake-On-LAN (WOL) (ATX power only)

Wake on LAN is defined as the ability of a management application to remotely power up a computer which is powered off. Remote PC setup, updates and asset tracking can occur after-hours and on weekends, so daily LAN traffic is kept to a minimum and users are not interrupted.

The motherboard has a 3-pin header (WOL) that connects to the 3-pin header on the Network Interface Card (NIC), which has WOL capability.

1-6 Power Supply

As with all computer products, a stable power source is necessary for proper and reliable operation. It is even more important for Pentium II processors that have high CPU clock rates of 300 MHz and above.

The SUPER P6DGH accommodates both AT and ATX power supplies. Although most power supplies generally meet the specifications required by the CPU, some are inadequate. To obtain the highest system reliability, be certain that your AT power supply provides +5 VDC with a voltage range between +4.95 VDC (minimum) and +5.25 VDC (maximum) and a current rating of 25 A or above.

It is highly recommended that you use a high quality power supply. Additionally, in areas where noisy power transmission is present, you may choose to install a line filter to shield the computer from noise. It is recommended that you also install a power surge protector to help avoid problems caused by power surges. For serious workstation/server applications, it is highly recommended that users employ the secondary power connector PW5 (for AT power) or J36 (for ATX power) to ensure balanced power distribution.

1-7 Winbond Super I/O Controller

The disk drive adapter functions of the Super I/O chip include a floppy disk drive controller that is compatible with industry standard 82077/765, a data separator, write pre-compensation circuitry, decode logic, data rate selection, a clock generator, drive interface control logic and interrupt and DMA logic. The wide range of functions integrated into the Super I/O chip greatly reduces the number of components required for interfacing with floppy disk drives. The Super I/O supports four 360 K, 720 K, 1.2 M, 1.44 M or 2.88 M disk drives and data transfer rates of 250 Kb/s, 500 Kb/s or 1 Mb/s.

It also provides two high-speed serial communication ports (UARTs), one of which can support serial infrared communication. Each UART includes a 16-byte send/receive FIFO, a programmable baud rate generator, complete modem control capability and a processor interrupt system. Both UARTs provide legacy speed with baud rates up to 115.2 Kbps as well as advanced speed with baud rates of 230 K, 460 K, or 921 Kbps, which support higher speed modems.

The Super I/O controller provides support for one PC-compatible printer port (SPP), Bidirectional Printer Port (BPP), Enhanced Parallel Port (EPP) or Extended Capabilities Port (ECP). Also available, through the printer port interface pins, are Extension FDD and Extension 2FDD Modes, allowing one or two external floppy disk drives to be connected.

The Super I/O provides functions that comply with ACPI (Advanced Configuration and Power Interface), which includes support for legacy and ACPI power management through an SMI or SCI function pin. It also features auto power management to reduce power consumption.

The Super I/O complies with **the Microsoft PC97 Hardware Design Guide**. IRQs, DMAs and I/O space resources can flexibly adjust to meet ISA PnP requirements. Moreover, it meets the specifications of PC97's requirement regarding power management: ACPI and DPM (Device Power Management).

1-8 AIC-7896 MultiChannel™ Single-Chip UltraSCSI Controller

The SUPER P6DGH has an onboard Adaptec SCSI controller, which is 100% compatible with all major operating and hardware platforms. PCI 2.1 and SCAM Level 1 compliance are assured.

Two independent Ultra II LVD SCSI channels provide a per channel data transfer rate of 80 MB/s. Connectors include two 68-pin 16-bit Ultra Wide SCSI connectors (JA1 and JA2) and one 50-pin 8-bit Ultra SCSI connector (JA3). The AIC-7896 Ultra II SCSI chip connects to a 32-bit PCI bus. You can connect up to 15 devices (seven 8-bit internal and eight 16-bit internal or external SCSI devices, or 15 Wide internal and external SCSI devices).

When Fast SCSI devices are connected, the total length of all cables (internal and external) must not exceed 3 meters (9.8 ft) to ensure reliable operation. If no Fast SCSI devices are connected, the total length of all cables must not exceed 6 meters (19.7 ft).

The AIC-7896 consolidates the functions of two SCSI chips to eliminate the need of a PCI bridge. Reducing PCI bus loading enables system capabilities to be expanded with additional PCI devices.

1-9 Warranty, Technical Support and Service

The manufacturer will repair or exchange any unit or parts that fail due to manufacturing defects. This warranty covers the cost of parts for one year (12 months) and the cost of labor for two years (24 months) from the original invoice date of purchase.

Warranty Terms and Conditions

Super Micro Computer, Inc. warrants its products to be free from defects in material and workmanship. The warranty period is for two years (24 months) beginning from the original purchase date. Super Micro shall, at our option and cost, repair or replace the defective product if the product is returned within the applicable warranty period and if the product is found by Super Micro to be defective within the terms of this warranty. Before presenting any motherboard for warranty service, the customer must first remove the CPU(s), memory or other peripherals.

This warranty shall not apply to any failure or defect caused by misuse, abnormal or unusually heavy use, neglect, abuse, alteration, improper installation, unauthorized repair or modification, improper testing, or accidents or causes external to the product such as, but not limited to, excessive heat or humidity, power failure, power surges or acts of God/Nature. Super Micro makes no warranty with respect to (i) expendable components, (ii) any software products

supplied by us, (iii) any experimental or developmental products and (iv) products not manufactured by us; all of which components, software and products are provided "AS-IS."

This warranty is in lieu of any other warranty expressed or implied. In no event will Super Micro be held liable for incidental or consequential damages, such as loss of revenue or loss of business arising from the purchase of Super Micro products.

Returns

If you must return products for any reason, refer to the section in Chapter 3 of this manual entitled “Returning Merchandise for Service.”

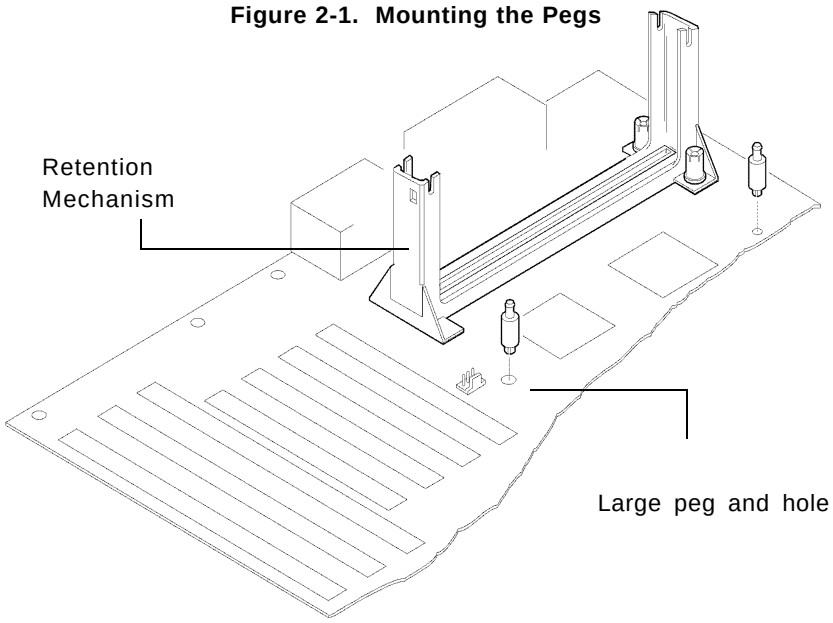
Chapter 2
Installation

2-1 Pentium II Processor Installation

1. Check the Intel-boxed processor kit for the following items: the processor with the fan/heat sink attached, two black plastic pegs, two black plastic supports and one power cable.

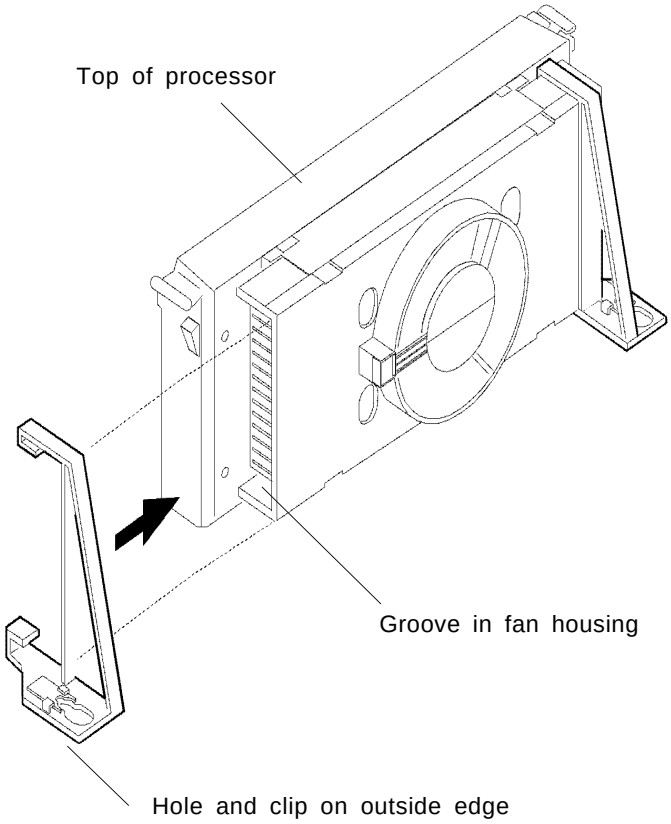
2. Install the retention mechanism attachment mount under the motherboard. Do this before mounting the motherboard in the chassis. Do not screw it too tight. Mount the two black plastic pegs on the motherboard (Figure 2.1). These pegs will be used to attach the fan/heat sink supports. Notice that one hole and the base of one peg are larger than the other hole and peg base. Push each peg into its hole firmly until you hear it "click" into place.

Figure 2-1. Mounting the Pegs



3. Slide a black plastic support onto each end of the fan/heat sink making sure that the hole and clip are on the outside edge of the support. If the supports are reversed, the holes will not line up with the pegs on the motherboard. Slide each support toward the center of the processor until the support is seated in the outside groove in the fan housing.

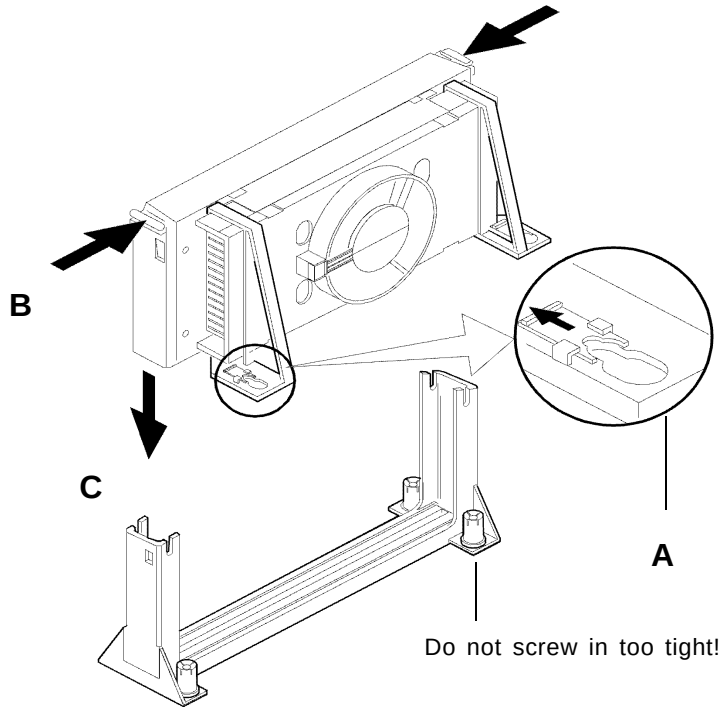
Figure 2-2. Support for Fan/Heat Sink



4. Slid the clip (A) onto each support toward the processor, exposing the hole that will fit over the peg on the motherboard. Push the latches (B) on the processor toward the center of the processor until they click into place.

5. Hold the processor so that the fan shroud is facing toward the pegs on the motherboard. Slide the processor (C) into the retention mechanism and slide the supports onto the pegs. Ensure that the pegs on the motherboard slide into the holes in the heat sink support and that the alignment notch in the SEC cartridge fits over the plug in Slot 1. Push the processor down firmly, with even pressure on both sides of the top, until it is seated.

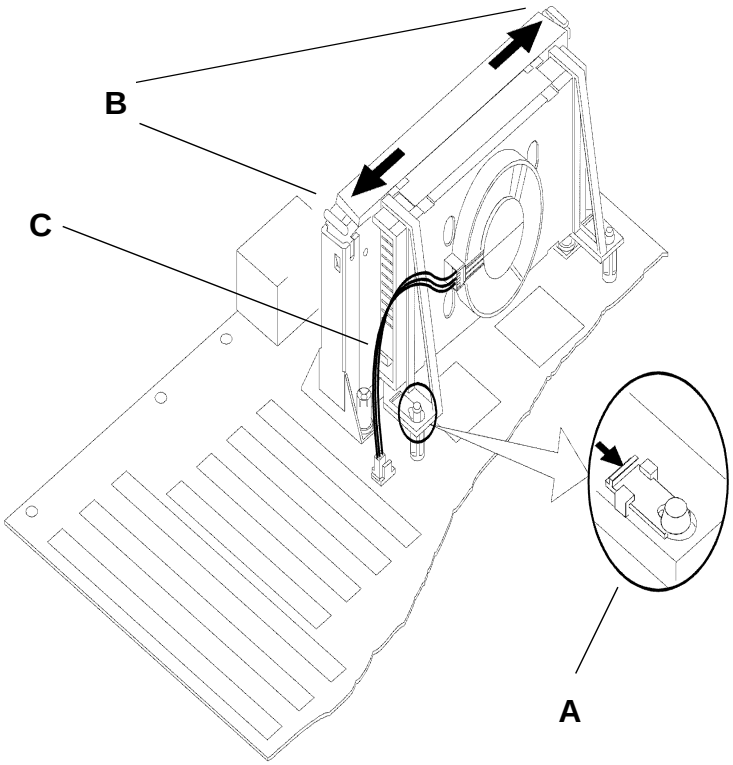
Figure 2-3. Retention Mechanism



6. Slide the clips forward onto the supports (A) until they click into place to hold the pegs securely. Apply slight pressure to the peg and push the peg toward the clip while pushing the clip forward. Push the latches on the processor (B) outward until they click into place in the retention mechanism. The latches must be secured for the proper electrical connection of the processor.

7. Attach the small end of the power cable (C) to the three-pin connector on the processor, then attach the large end to the three-pin connector on the motherboard.

Figure 2-4. Attaching the Power Cable



Installation of the Universal Retention Mechanism (URM)*

Please Note! Screws and washers attach from the bottom of the board and must be installed before mounting the board to the chassis. *(See Figures 2-5 and 2-6)*

1. When Installing the URM be sure the ***Left*** (L) and the ***Right*** (R) sides are placed accordingly.

2. Lift both arms upright and slide the processor into the socket, noting that the notches need to line up.

*These directions may not apply to second source URMs

Figure 2-5. URM and Celeron Installation

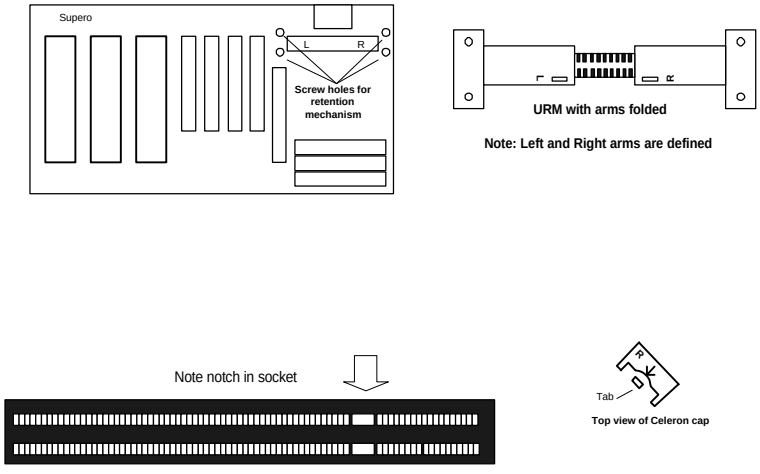


Figure 2-6. Installing a Slot 1 Processor

Removing the Pentium II Processor

To remove the Pentium II processor from the motherboard, follow these steps (the reverse of the installation process).

1. Disconnect the fan power cable from the motherboard. It is recommended to leave the cable connected to the processor.

2. Slide the clips on the supports backward to release the pegs in the motherboard. Push the latches on the processor toward the center of the processor until they click into place.

3. Lift one end of the processor until it is freed from Slot 1. Lift the other end of the processor until it is freed from Slot 1. Lift the entire processor (with the fan/heat sink supports still attached) until it is free from the retention mechanism.

4. Remove the heat sink support pegs from the motherboard and discard them. With one hand, squeeze together the two halves of the peg on the bottom side of the motherboard. With the other hand, pull the peg out of the hole in the motherboard. Do not reuse the pegs.

When handling the Pentium II processor, avoid placing direct pressure on the label area of the fan.

When removing the Pentium II processor, avoid pressing down on the motherboard or any components. Instead, press down on the plastic connectors.

2-2 Static-Sensitive Devices

Static electrical discharges can damage electronic components. To prevent damage to your system board, it is important to handle it very carefully. The following measures are generally sufficient to protect your equipment from static discharge.

Precautions

- Use a grounded wrist strap designed for static discharge.
- Touch a grounded metal object before you remove the board from the antistatic bag.
- Handle the board by its edges only; do not touch its components, peripheral chips, memory modules or gold contacts.
- When handling chips or modules, avoid touching their pins.
- Put the system board and peripherals back into their antistatic bags when not in use.
- For grounding purposes, be sure your computer system's chassis allows for excellent conductive contact between its power supply, the case, the mounting fasteners and the system board.

Unpacking

The system board is shipped in antistatic packaging to avoid static damage. When unpacking the board, be sure the person handling the board is static-protected.

2-3 Changing the CPU Speed

To change the CPU speed for a Pentium II processor, change the jumpers as shown in Table 2-1. Refer to Table 2-2 for the external bus speed jumper settings. The default bus speed is set to "Auto". The following example will show you which CPU Core/Bus Ratio to use. The general rule is to divide the CPU speed by the bus speed (66 or 100 MHz). For example, if you have a 266 MHz CPU, dividing

it by 66 will give you a CPU Core/Bus Ratio of 4. After determining the proper CPU Core/Bus Ratio, refer to Table 2-1 for the jumper settings of JB1, JB2, JB3 and JB4.

$$\text{CPU Core/Bus Ratio} = \frac{\text{CPU Speed}}{\text{Bus Frequency}}$$

$$\text{CPU Core/Bus Ratio} = \frac{266\ \text{MHz}}{66\ \text{MHz}} = 4.0$$

Table 2-1. Pentium II Speed Selection

CPU Core/ Bus Ratio	JB1	JB2	JB3	JB4
3.0	ON	OFF	ON	ON
3.5	OFF	OFF	ON	ON
4.0	ON	ON	OFF	ON
4.5	OFF	ON	OFF	ON
5.0	ON	OFF	OFF	ON
5.5	OFF	OFF	OFF	ON
6.0	ON	ON	ON	OFF

Table 2-2. External Bus Speed Selection

MHz	JP11
Auto	1-2 (default)
66	2-3
100	OFF

For more detailed information, please see Intel's website at www.intel.com.

2-4 Mounting the Motherboard in the Chassis

The SUPER P6DGH has standard mounting holes to fit different types of chassis. Chassis may come with a variety of mounting fasteners made of metal or plastic. Although a chassis may have both metal and plastic fasteners, metal fasteners are the most highly recommended because they ground the system board to the chassis. Therefore, use as many metal fasteners as possible for better grounding.

2-5 Connecting Cables and Jumpers

Power Supply Connectors

After you have securely mounted the motherboard to the chassis, you are ready to connect the cables. The SUPER P6DGH supports both AT and ATX power, only one of which can be used at a time.* Please check the power mode jumper settings on page 2-23.

AT Power: Attach the power supply cables to PW1. Do not force the cables, but make sure they are fully seated. The two black wires on each power connector for PW1 will sit next to each other when correctly installed. For heavy power loads, also connect the power supply to the secondary AT power connector at PW5. See Table 2-3 for the pin definitions of the main AT power connector and Table 2-4 for the pin definitions of the secondary AT power connector.

ATX Power: Attach the power supply cable to PW2, making sure it is fully seated. For heavy power loads, also connect the power supply to the secondary ATX power connector at J36. See Table 2-5 for the pin definitions of the main ATX power connector and Table 2-6 for the pin definitions of the secondary ATX power connector.

***Note:** For heavy-load applications, it is highly recommended that you use both the main AND the secondary power connectors for either AT or ATX power.

Table 2-3. Main AT Power Connector Pin Definitions

Connector Number	Pin Number	Function
PW1	1	Power Good (Power on reset, TTL signal)
	2	+5 VCC
	3	+12 VCC
	4	-12 VCC
	5	Ground (Black wire to be connected)
	6	Ground (Black wire to be connected)
	7	Ground (Black wire to be connected)
	8	Ground (Black wire to be connected)
	9	-5 VCC
	10	+5 VCC
	11	+5 VCC
	12	+5 VCC

Table 2-4. Secondary AT Power Connector Pin Definitions

Connector Number	Pin Number	Function
PW5 (+5V Extra)	1	+5 VCC
	2	+5 VCC
	3	+5 VCC
	4	Ground (Black wire to be connected)
	5	Ground (Black wire to be connected)
	6	Ground (Black wire to be connected)

Table 2-5. Main ATX Power Connector Pin Definitions

Connector Number	Pin Number	Function	Pin Number	Function
PW2 (ATX Power)	1	3.3V	11	3.3V
	2	3.3V	12	-12V
	3	COM	13	COM
	4	5V	14	PS-ON
	5	COM	15	COM
	6	5V	16	COM
	7	COM	17	COM
	8	PW-OK	18	-5V
	9	5VSB	19	5V
	10	12V	20	5V

Table 2-6. Secondary ATX Power Connector Pin Definitions

Connector Number	Pin Number	Function
J36 (PWR_SEC)	1	GND
	2	GND
	3	GND
	4	+3.3V
	5	+3.3V
	6	+5V

PW_ON Connector

The PW_ON connector is located on pins 9 and 10 of JF2. Momentarily contacting both pins will power on/off the system. To turn off the power, hold down the power button for at least 4 seconds. In order to have the "4-second" feature, you need to enable the Power Management/APM in the BIOS and set the Power Button Function to "Suspend". See Table 2-7 for pin definitions.

Table 2-7. PW_ON Connector Pin Definitions

Pin Number	Definition
9	3V_STBY
10	PW_ON

Infrared Connector

The infrared connector is located on pins 1-8 of JF2. See Table 2-8 for pin definitions.

Table 2-8. Infrared Pin Definitions

Pin Number	Definition
1	+5V
2	Key
3	IRRX
4	Ground
5	IRTX
6	N.C.
7	N.C.
8	N.C.

Reset Header

The reset header is located on pins 12 and 13 of JF2. This header attaches to the hardware Reset switch on the computer case. See Table 2-9 for pin definitions.

Table 2-9. Reset Pin Definitions

Pin Number	Definition
12	Ground
13	Reset

Keylock/Power LED Connector

The keylock/power LED connector is located on pins 5 to 9 of JF1. See Table 2-10 for pin definitions. Pins 5 and 7 are for the power LED. Pins 8 and 9 are for the keylock.

Table 2-10. Keylock/Power LED Pin Definitions

Pin Number	Function	Definition
5	+5V	Red wire, LED power
6	+5V	LED power
7	GND	Black wire
8		Keyboard inhibit
9	GND	Black wire

Hard Drive LED

The hard drive LED is located on pins 1 to 4 of JF1. Attach the hard drive LED cable onto pins 1 and 2. See Table 2-11 for pin definitions.

Table 2-11. Hard Drive LED Pin Definitions

Pin Number	Definition
1	+5V
2	HD Active
3	HD Active
4	+5V

Speaker Connector

The speaker connector is located on pins 10 to 13 of JF1. See Table 2-12 for pin definitions.

Table 2-12. Speaker Connector Pin Definitions

Pin Number	Function	Definition
10	+5V	Red wire, power
11	Key	No connection
12	Key	No connection
13	Data	Speaker data

AT Keyboard Connector

Keyboard connector J74 has five pins. See Table 2-13 for pin definitions.

Table 2-13. Keyboard Connector Pin Definitions

Pin Number	Function
1	Keyboard clock
2	Keyboard data
3	Spare
4	Ground
5	+5 VDC

Universal Serial Bus

The Universal Serial Bus is located on J17 and J18. See Table 2-14 for pin definitions.

Table 2-14. USB Pin Definitions

Pin Number	J17 Function	Pin Number	J18 Function
1	+5V	1	+5V
2	P0-	2	P0-
3	P0+	3	P0+
4	GND	4	GND
		5	Key

PS/2 Mouse Header

The PS/2 Mouse header is located on JP25. See Table 2-15 for pin definitions.

Table 2-15. PS/2 Mouse Pin Definitions

Pin Number	Function	Pin Number	Function
1	NC	2	NC
3	NC	4	CLK
5	NC	6	VCC
7	Data	8	NC
9	GND		

Serial Ports

Serial port COM1 is located on J20 and serial port COM2 is located on J21. See Table 2-16 for pin definitions.

Table 2-16. Serial Port Pin Definitions

Pin Number	Function	Pin Number	Function
1	DCD	6	CTS
2	DSR	7	DTR
3	Serial In	8	RI
4	RTS	9	GND
5	Serial Out		

Power On/Off State (ATX power only)

Refer to Table 2-17 on how to set JP20. Save Power Down (PD) State is the default and is used when you want the system to remain in the power-off state when you first apply power to the system or when the system comes back from an AC power failure. PIIX4 control is used if you want the system to be in the power-on state the first time you apply power to the system or when the system comes back from an AC power failure. When set to 2-3, the system will remain off when AC power returns.

Table 2-17. Power On/Off State Pin Definitions

Connector Number	Jumper Position	Function
JP20	1-2 2-3	PIIX4 Ctrl Save PD State

CMOS Clear

Refer to Table 2-18 for instructions on how to clear the CMOS. **For the ATX power supply, you need to completely shut down the system before using JBT1 to clear the CMOS.** Do not use the PW_ON connector to clear the CMOS.

Table 2-18. CMOS Clear Pin Definitions

Connector Number	Jumper Position	Function
JBT1	1-2 2-3	Normal CMOS Clear

Overheat LED

Refer to Table 2-19 to connect an LED to JOH1 to indicate an overheat warning.

Table 2-19. Overheat LED Pin Definitions

Pin Number	Function
1	+12 V
2	Signal

Buzzer Overheat Notification

Refer to Table 2-20 for setting BZ_ON to either enable or disable buzzer BZ1 as an overheat warning.

Table 2-20. Buzzer Enable Jumper Settings

Jumper Position	Function
ON	Enable Buzzer
OFF	Disable Buzzer

Chassis Intrusion Connector

The Chassis Intrusion Detection feature is described on page 1-9. Refer to Table 2-21 for its connector pin definitions on JL1.

Table 2-21. Chassis Intrusion Pin Definitions

Pin Number	Function
1	Intrusion Input
2	Ground

Wake-On-LAN

The Wake-On-LAN connector is located on WOL. Refer to Table 2-22 for pin definitions.

Note: The 5V standby for the ATX power mode requires a minimum of 720 mA or must comply with ATX Specification 2.01 for the WOL function to work.

Table 2-22. Wake-on-LAN Pin Definitions

Pin Number	Function
1	+5V Standby
2	Ground
3	Wake up

Fan Connectors*

The CPU fans are located on JT1, JT2 and JT3. The overheat fan with the tachometer sensor input is located on JT3. Refer to Table 2-23 for pin definitions.

Table 2-23. Fan Pin Definitions

Pin Number	Function
1	Ground
2	+12 V
3	Tachometer

* Caution: These connectors are DC direct.

i960 Serial Port

The i960 serial port is located on J943. Refer to Table 2-24 for pin definitions.

Table 2-24. i960 Serial Port Pin Definitions

Pin Number	Function	Pin Number	Function
1	CD	6	DSR
2	TXD	7	CTS
3	RXD	8	RTS
4	DTR	9	N.C.
5	GND		

i960 Fail LED Indicator

ID4 is used to determine whether Mode 3 of the i960 RD IO processor is functioning properly. Refer to Table 2-25 for the LED indications.

Table 2-25. i960 Fail LED Definitions

LED Status	Definition
OFF	i960 Mode 3 OK
ON	i960 Mode 3 failed (i960 is in Mode 0)

i960 Initialization Modes

Refer to Table 2-26 for instructions on setting the mode.
Mode 0 = i960 is configured as a PCI-PCI bridge.
Mode 3 = i960 is configured as an I/O processor and a PCI-PCI bridge.

Table 2-26. i960 Mode Settings

Jumper	Mode 3	Mode 0 (default)
JP915	OFF	OFF
JP918	OFF	ON
JP919	OFF	ON
JP920	OFF	OFF
JP921	ON	ON

i960 Jumper Settings

Refer to Table 2-27 for more jumper settings related to the i960 IOP.

Table 2-27. i960 Jumper Settings

Jumper	Default	Definition
JP911	OFF	Enables the internal secondary arbiter
JP917	ON	Enables I/O IRQ
JP924	1-2	OFF Ext. debugging mode 960 Flash enable

I²C Connector

The I²C connector located on J940 is for development purposes only. Refer to Table 2-28 for pin definitions.

Table 2-28. I²C Pin Definitions

Pin Number	Function
1	SDA
2	Ground
3	SCL
4	VCC

SLED (SCSI LED) Indicator

The SLED connector is used to provide an LED indication of SCSI activity. Refer to Table 2-29 for connecting the SCSI LED.

Table 2-29. SLED Pin Definitions

Pin Number	Function
1	+5V
2	SCSI Active
3	SCSI Active
4	+5V

$I_2$0 Debug LED (Optional)

An optional 7-segment LED display is located at IU48 for $I_2$0 debug purposes.

AT/ATX Power Mode Jumper Settings*

The JATPWR and JP100 jumpers are used to configure the system for either the AT or ATX power mode. Refer to Table 2-30 for the power mode settings. See page 2-10 for connecting power cables. The default setting is for AT power mode. See precautions below.

Table 2-30. JATPWR and JP100 Jumper Settings

Mode	JATPWR	JP100
AT	 (all on)	 (off)
ATX	 (all off)	 (on)

***Note:** For heavy-load applications, it is highly recommended that you use both the main AND the secondary power connectors for either AT or ATX power.

Note: It is important to verify whether your power supply is AT or ATX and to set the above jumpers correctly **before** you apply power to the system.

SCSI Termination Jumper Settings

Jumpers JA5, JA6 and JA7 are used to terminate the SCSI channels. Refer to Table 2-31 for the results of installing jumpers at these locations.

Table 2-31. SCSI Termination Jumper Settings

Jumper	Setting	Result
JA5	On	Enables JA1 termination
	Off	JA1 termination disabled
JA6	On	Enables termination of low bytes on JA2
	Off	No termination of low bytes on JA2
JA7	On	Enables termination of high bytes on JA2
	Off	No termination of high bytes on JA2

SBLINK Connector

The SBLINK connector is included for audio cards residing in a PCI slot when used with a serial IRQ. See the website of Creative Labs at www.soundblaster.com for more information on using this connector. Refer to Table 2-32 for pin definitions.

Table 2-32. SBLINK Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	GNTA#	2	N.C.
3	GND	4	REQ#A
5	GND	6	SER IRQ
7	IRQ5	8	GND
9	IRQ7	10	IRQ9
11	GND	12	IRQ10
13	GND	14	IRQ11

2-6 Installing/Removing SIMM/DIMM Modules

The SUPER P6DGH can accommodate a maximum of 2 GB Registered DIMM supported or 1 GB SDRAM DIMMs. It has 4 168-pin 3.3V unbuffered DIMM slots. It is not recommended to mix EDO DIMM modules with SDRAM DIMM modules.

There are three types of EDO and SDRAM DIMM modules: x4, x8 and x16. If you are using the x4 type, you can populate the DIMM slots with either 4 single-sided or 2 double-sided memory modules. For memory configurations of 512 MB EDO DIMMs or higher, it is recommended to use x8 or x16 types of memory.

There are no jumpers needed to configure the onboard memory. EDO memory must be 70ns or faster. Refer to Figure 2-7 and the instructions below for installing or removing DIMM modules.

CAUTION

Exercise extreme care when installing or removing SIMM/DIMM modules to prevent any possible damage.

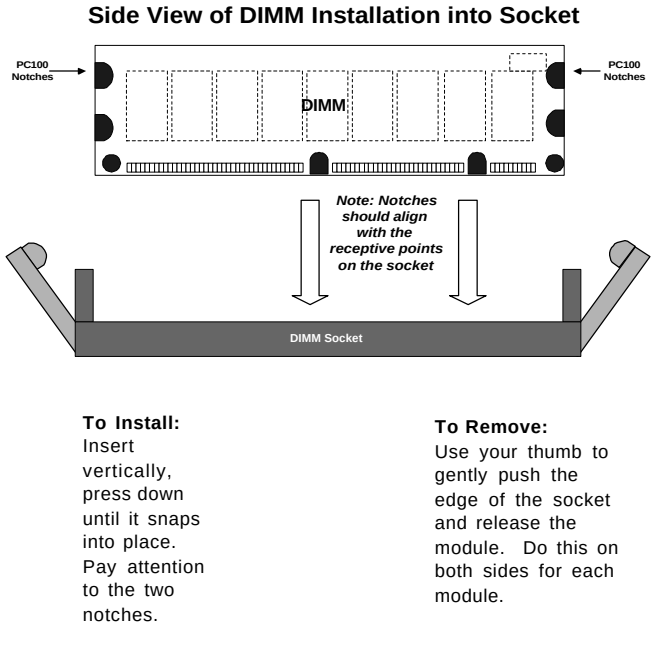


Figure 2-7. Installing/Removing a DIMM Memory Module

SIMM/DIMM Module Installation

1. Insert DIMM modules in Bank 0 through Bank 3 as required for the desired system memory.
2. Insert each DIMM module vertically into its socket. Pay attention to the two notches to prevent inserting the DIMM in the wrong position. Gently press the DIMM module until it snaps upright into place in the socket.
3. Insert each SIMM module into its socket at an angle. Gently press the SIMM module until it snaps upright into place in the socket.

Removing DIMM Modules

1. Remove DIMM modules in any order.
2. Gently push the edge of the sockets to the side to release the module. Remove one side of the DIMM module first, and then the other side to prevent breaking the socket.

Removing SIMM Modules

1. Gently push the edge of the sockets to the side to release the module. Remove one side of the SIMM module first, and then the other side to prevent breaking the socket.

2-7 Connecting Parallel, Floppy and Hard Disk Drives

Use the following information to connect the floppy and hard disk drive cables.

- The floppy disk drive cable has seven twisted wires.
- A red mark on a wire typically designates the location of pin 1.
- A single floppy disk drive ribbon cable has 34 wires and two connectors to provide for two floppy disk drives. The connector with twisted wires always connects to drive A, and the connector that does not have twisted wires always connects to drive B.
- An IDE hard disk drive requires a data ribbon cable with 40 wires, and a SCSI hard disk drive requires a SCSI ribbon cable with 50 wires. A wide SCSI hard disk drive requires a SCSI ribbon cable with 68 wires.
- A single IDE hard disk drive cable has two connectors to provide for two drives. To select an IDE disk drive as C, you would normally set the drive select jumper on the drive to DS1. To select an IDE disk drive as D, you would normally set the drive select jumper on the drive to DS2. Consult the documentation that came with your disk drive for details on actual jumper locations and settings.
- A single SCSI ribbon cable typically has three connectors to provide for two hard disk drives and the SCSI adapter. (Note: most SCSI hard drives are single-ended SCSI devices.) The SCSI ID is determined either by jumpers or by a switch on the SCSI device. The last internal (and external) SCSI device cabled to the SCSI adapter must be terminated.
- Some drives require a special controller card. Read your disk drive manual for details.

Parallel Port Connector

The parallel port is located on J19. See Table 2-33 for pin definitions.

Table 2-33. Parallel Port Pin Definitions

Pin Number	Function	Pin Number	Function
1	Strobe-	2	Auto Feed-
3	Data Bit 0	4	Error-
5	Data Bit 1	6	Init-
7	Data Bit 2	8	SLCT IN-
9	Data Bit 3	10	GND
11	Data Bit 4	12	GND
13	Data Bit 5	14	GND
15	Data Bit 6	16	GND
17	Data Bit 7	18	GND
19	ACJ-	20	GND
21	BUSY	22	GND
23	PE	24	GND
25	SLCT		

Floppy Connector

The floppy connector is located on J22. See Table 2-34 for pin definitions.

Table 2-34. Floppy Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	GND	2	FDHDIN
3	GND	4	Reserved
5	Key	6	FDEDIN
7	GND	8	Index-
9	GND	10	Motor Enable
11	GND	12	Drive Select B-
13	GND	14	Drive Select A-
15	GND	16	Motor Enable
17	GND	18	DIR-
19	GND	20	STEP-
21	GND	22	Write Data-
23	GND	24	Write Gate-
25	GND	26	Track 00-
27	GND	28	Write Protect-
29	GND	30	Read Data-
31	GND	32	Side 1 Select-
33	GND	34	Diskette Change

IDE Interfaces

There are no jumpers to configure the onboard IDE interfaces J15 and J16. Refer to Table 2-35 for pin definitions.

Table 2-35. IDE Connector Pin Definitions

Pin Number	Function	Pin Number	Function
1	Reset IDE	2	GND
3	Host Data 7	4	Host Data 8
5	Host Data 6	6	Host Data 9
7	Host Data 5	8	Host Data 10
9	Host Data 4	10	Host Data 11
11	Host Data 3	12	Host Data 12
13	Host Data 2	14	Host Data 13
15	Host Data 1	16	Host Data 14
17	Host Data 0	18	Host Data 15
19	GND	20	Key
21	DRQ3	22	GND
23	I/O Write-	24	GND
25	I/O Read-	26	GND
27	IOCHRDY	28	BALE
29	DACK3-	30	GND
31	IRQ14	32	IOCS16-
33	Addr 1	34	GND
35	Addr 0	36	Addr 2
37	Chip Select 0	38	Chip Select 1-
39	Activity	40	GND

AGP Port Interface

There are no jumpers to configure the AGP port. Refer to Table 2-36 for pin definitions.

Table 2-36. AGP Pin Definitions

Pin #	B	A	Pin #	B	A
1	Spare	12V	34	Vddq3.3	Vddq3.3
2	5.0V	Spare	35	AD21	AD22
3	5.0V	Reserved*	36	AD19	AD20
4	USB+	USB-	37	GND	GND
5	GND	GND	38	AD17	AD18
6	INTB#	INTA#	39	C/BE2#	AD16
7	CLK	RST#	40	Vddq3.3	Vddq3.3
8	REQ#	GNT#	41	IRDY#	Frame#
9	VCC3.3	VCC3.3	42		
10	ST0	ST1	43	GND	GND
11	ST2	Reserved	44		
12	RBF#	PIPE#	45	VCC3.3	VCC3.3
13	GND	GND	46	DEVSEL#	TRDY#
14	Spare	Spare	47	Vddq3.3	STOP#
15	SBA0	SBA1	48	PERR#	Spare
16	VCC3.3	VCC3.3	49	GND	GND
17	SBA2	SBA3	50	SERR#	PAR
18	SB_STB	Reserved	51	C/BE1#	AD15
19	GND	GND	52	Vddq3.3	Vddq3.3
20	SBA4	SBA5	53	AD14	AD13
21	SBA6	SBA7	54	AD12	AD11
22	KEY	KEY	55	GND	GND
23	KEY	KEY	56	AD10	AD9
24	KEY	KEY	57	AD8	C/BE0#
25	KEY	KEY	58	Vddq3.3	Vddq3.3
26	AD31	AD30	59	AD_STB0	Reserved
27	AD29	AD28	60	AD7	AD6
28	VCC3.3	VCC3.3	61	GND	GND
29	AD27	AD26	62	AD5	AD4
30	AD25	AD24	63	AD3	AD2
31	GND	GND	64	Vddq3.3	Vddq3.3
32	AD_STB1	Reserved	65	AD1	AD0
33	AD23	C/BE3#	66	SMB0	SMB1

Ultra II LVD SCSI Interfaces

Refer to Table 2-31 to configure the Ultra II LVD SCSI interfaces JA1 and JA2. Refer to Table 2-37 for pin definitions.

Table 2-37. Ultra II LVD SCSI Pin Definitions

Connector Contact Number	Signal Names	Connector Contact Number	Signal Names
1	+DB(12)	35	-DB(12)
2	+DB(13)	36	-DB(13)
3	+DB(14)	37	-DB(14)
4	+DB(15)	38	-DB(15)
5	+DB(P1)	39	-DB(P1)
6	+DB(0)	40	-DB(0)
7	+DB(1)	41	-DB(1)
8	+DB(2)	42	-DB(2)
9	+DB(3)	43	-DB(3)
10	+DB(4)	44	-DB(4)
11	+DB(5)	45	-DB(5)
12	+DB(6)	46	-DB(6)
13	+DB(7)	47	-DB(7)
14	+DB(P)	48	-DB(P)
15	GROUND	49	GROUND
16	DIFFSENS	50	GROUND
17	TERMPWR	51	TERMPWR
18	TERMPWR	52	TERMPWR
19	RESERVED	53	RESERVED
20	GROUND	54	GROUND
21	+ATN	55	-ATN
22	GROUND	56	GROUND
23	+BSY	57	-BSY
24	+ACK	58	-ACK
25	+RST	59	-RST
26	+MSG	60	-MSG
27	+SEL	61	-SEL
28	+C/D	62	-C/D
29	+REQ	63	-REQ
30	+I/O	64	-I/O
31	+DB(8)	65	-DB(8)
32	+DB(9)	66	-DB(9)
33	+DB(10)	67	-DB(10)
34	+DB(11)	68	-DB(11)

Wide SCSI Interface

Refer to Table 2-38 for the Wide SCSI pin definitions.

Table 2-38. 50-pin Wide SCSI Pin Definitions

Pin Number	Function	Pin Number	Function
1	GND	26	-DB (0)
2	GND	27	-DB (1)
3	GND	28	-DB (2)
4	GND	29	-DB (3)
5	GND	30	-DB (4)
6	GND	31	-DB (5)
7	GND	32	-DB (6)
8	GND	33	-DB (7)
9	GND	34	-DB (P)
10	GND	35	GND
11	GND	36	GND
12	Reserved	37	Reserved
13	Open	38	Termpwr
14	Reserved	39	Reserved
15	GND	40	GND
16	GND	41	-ATN
17	GND	42	GND
18	GND	43	-BSY
19	GND	44	-ACK
20	GND	45	-RST
21	GND	46	-MSG
22	GND	47	-SEL
23	GND	48	-C/D
24	GND	49	-REQ
25	GND	50	-I/O

Chapter 3
Troubleshooting

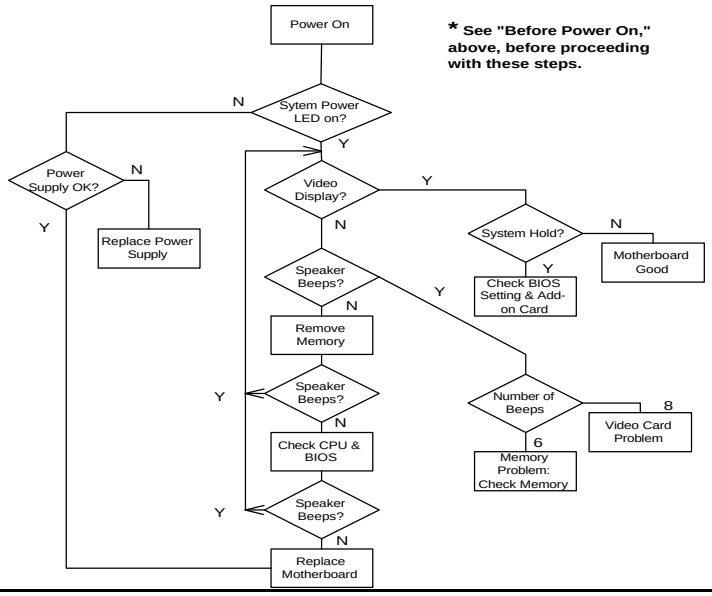
3-1 Troubleshooting Procedures

Use the following procedures and flowchart to troubleshoot your system. If you have followed all of the procedures below and still need assistance, refer to the 'Technical Support Procedures' and/or 'Returning Merchandise for Service' section(s) in this chapter.

Before Power On

1. Make sure there are no short circuits between the motherboard and the chassis.
2. Disconnect all ribbon/wire cables from the motherboard.
3. Remove all the add-in cards except the video graphics card. (Be sure the video/graphic card is inserted properly.)
4. Install the CPU, a chassis speaker and a power LED to the motherboard. (Check all the jumper settings as well.)
5. Install a memory module into one bank.
6. Check the power supply voltage monitor 115V/230V switch.

Figure 3-1. Troubleshooting Flowchart



No Power

1. Make sure the default jumper is on and the CPU is correctly setup.
2. Turn the power switch on and off to test the system.
3. If the power is still not on, turn off the system power and move jumper JP20 from 2-3 to 1-2.
4. If moving the jumper setting has not helped, clear CMOS.
5. Check the power supply voltage monitor. (Check the power supply 115V/230V switch)

No Video

Use the following steps for troubleshooting your system configuration.

1. If the power is on but you have no video, remove all the add-on cards and cables.
2. Check for shorted connections, especially under the motherboard.
3. Check the jumpers settings, clock speed and voltage settings.
4. Use the speaker to determine if any beep codes exist. Refer to Appendix A for details about beep codes.

NOTE

If you are a system integrator, VAR or OEM, a POST diagnostics card is recommended. For port 80h codes, refer to Appendix B.

Memory Errors

If you encounter a memory error, follow the procedures below.

1. Check to determine if the DIMM modules are improperly installed.
2. Make sure that different types of DIMMs have not been installed in different banks.
3. Determine if different speeds of DIMMs have been installed and verify that the BIOS setup is configured for the fastest speed of RAM used. It is recommended to use the same RAM speed for all DIMMs in the system.

4. Check for bad DIMM modules or chips.
5. Try to install the minimum memory first (single bank).

Losing the System's Setup Configuration

1. Check the setting of jumper JBT1. Ensure that you are using a high quality power supply. A poor quality power supply may cause the system to lose the CMOS setup. Refer to Chapter 1 of this manual for details.
2. If the above step does not fix the Setup Configuration problem, contact your vendor for repair.

3-2 Technical Support Procedures

1. Please go through the Troubleshooting Procedures and Frequently Asked Question (FAQ) sections in this chapter of the manual. Also, before contacting Technical Support , check our website FAQ at http://www.supermicro.com.
2. Take note that the motherboard manufacturer Super Micro does not sell directly to end-users, so it is best to check with your distributor or reseller for troubleshooting services. They should know of any possible problem(s) with the specific system configuration that was sold to you.
3. BIOS upgrades can be downloaded from the SUPER BBS# (408) 895-2022, 24 hours a day, using 1200-28800 baud, 8 data bits, 1 stop bit and no parity.
   BIOS upgrades can also be downloaded from our website at http://www.supermicro.com.
4. If you still cannot resolve the problem, include the following information when you e-mail Super Micro for technical support:
   - BIOS release date/version
   - System board serial number
   - Product model name
   - Invoice number and date
   - System configuration

   Due to the volume of e-mail we receive and the time it takes to replicate problems, a response to your question may not be immediately available. Please understand that although we do not have the resources to serve every end-user, we will

try our best to help all our customers.

5. Distributors: For immediate assistance, please have your account number ready when placing a call to our technical support department.

3-3 Frequently Asked Questions

Question: What are the differences between the various memories that the 440GX motherboard can support?

Answer: The 440GX integrates a main memory DRAM controller that supports a 64-bit or 72-bit (64-bit memory data plus 8 ECC bits) DRAM from 8 MB to 1 GB for SDRAM and from 8 MB to 2 GB registered DIMMs. DRAM types supported are EDO, Synchronous DRAM (SDRAM) or Registered DIM modules.

1. Mixing ECC and non-ECC will result in non-ECC operation.

EC/ECC is supported properly in the 440GX only if all the memory is 72 bits wide. A system with a mixture of 64 and 72-bit wide memory will disable the ECC function.

2. Registered SDRAM and unbuffered SDRAM cannot be mixed.

3. Mixing PC/100 DIMMs and PC/66 DIMMs will result in an unexpected memory count or system errors.

4. The user should populate the DIMMs starting with the DIMM socket located the furthest from the GX chip.

Question: **How do I update my BIOS?**

Answer: Update BIOS files are located on our web site at http://www.supermicro.com. Please check the current BIOS revision and make sure it is newer than your BIOS before downloading. Select your motherboard model and download the BIOS file to your computer. Unzip the BIOS update file and you will find three files: readme.txt (flash instructions), sm2flash.com (BIOS flash utility) and the BIOS image file (xxxxxx.rom). Copy these files onto a bootable floppy and reboot your system. There are no BIOS boot block protection jumpers on the motherboard. At the DOS prompt, enter the command "sm2flash". This will start the flash utility and give you an opportunity to save your current BIOS image. Flash the boot block

and enter the filename of the update BIOS image. NOTE: It is important to save your current BIOS and rename it "super.rom" in case you need to recover from a failed BIOS update. Select flash boot block, then enter the update BIOS image. Select "Y" to start the BIOS flash procedure and do not disturb your system until the flash utility displays that the procedure is complete. After updating your BIOS, clear the CMOS and then load the Optimal Values in the BIOS.

Question: **After flashing the BIOS my system does not have video. How can I correct this?**

Answer: If the system does not have video after flashing your new BIOS, the flashing procedure has failed. To remedy this, first clear the CMOS per the instructions in this manual and retry the BIOS flashing procedure. If you still do not have video, please use the following BIOS recovery procedure. Turn your system off and place the floppy disk with the saved BIOS image file called "super.rom" (see above FAQ) in drive A. Press and hold "CTRL" and "Home" at the same time, then turn on the power with these keys pressed until your floppy drive starts reading. Your screen will remain blank until the BIOS program is done. If the system reboots correctly, then the recovery is complete.

Question: **I have memory problems. What is the correct memory to use and which BIOS setting should I choose?**

Answer: The correct memory to use on the SUPER P6DGH is 168-pin DIMM 3.3V non-buffered SPD (Serial Present Detection) SDRAM and SDRAM. SPD SDRAM is preferred but not necessary. NOTE: Do not mix memory types; the results are unpredictable. If your memory count is exactly half of the correct value, go to the BIOS in the Chipset Setup and set "SDRAM AUTOSIZING SUPPORT" to *Enabled*. Change between the available options until one setting displays the correct size of your memory.

Question: **Which Operating System (OS) supports AGP?**

Answer: At present, Windows 98 and Windows NT 5.0 are the only OS's that have built-in support for AGP. Some AGP video adapters can run Windows 95 OSR2.1 with special drivers. Please contact your graphics adapter vendor for more details.

Question: **Do I need the CD that came with your motherboard?**

Answer: The supplied compact disc has quite a few drivers and programs that will greatly enhance your system. We recommend that you review the CD and install the applications you need. Applications included on the CD are PCI IDE Bus Master drivers for Windows 95 and Windows NT, 440GX chipset drivers for Windows 95, and Super Doctor Monitoring software.

Question: **How do I install an onboard SCSI device controller for my P6DGH motherboard?**

Answer: First, install the 3 NT installation disks and then follow the on-screen instructions to complete the procedure.

Question: **Why can't I turn off the power using the momentary power on/off switch?**

Answer: The "instant power off" function is controlled by the BIOS. When this feature is enabled in the BIOS, the motherboard will have instant-off capabilities as long as the BIOS has control of the system. When this feature is disabled or when the BIOS is not in control, such as during the memory count (the first screen that appears when the system is turned on), the momentary on/off switch must be held for more than four seconds to shut down. This feature is required to implement ACPI features on the motherboard.

Question: **I see some of my PCI devices sharing IRQs, but the system seems to be fine. Is this correct or not?**

Answer: Most PCI devices can share IRQs without performance penalties. These devices are designed to work correctly while sharing IRQs.

Question: **When I connect my Ultra II LVD Hard Drive on the JA1/ JA2 SCSI connection, the drive is not recognized by BIOS or it fails to boot. Do I need a special cable?**

Answer: Yes, for an Ultra II LVD Drive, you need a special 68-pin cable with active termination at the end of the cable, since Ultra II LVD Hard Drives do not have termination on the drive. Also, make sure the onboard terminations are enabled (JA5-JA7).

Question: **In the P6DGH, there are 5 PCI slots and onboard SCSI devices on the primary PCI bus. How are the PCI interrupt resources shared?**

Answer: The PCI interrupts are assigned as follows:

PIRQ A#: PCI 1 (J9), onboard SCSI (both channels on 7896)

PIRQ B#: PCI 2 (J10), AGP

PIRQ C#: PCI 3 (J11), PCI 5 (J35)

PIRQ D#: PCI 4 (J12), USB, i960RD

3-4 Returning Merchandise for Service

A receipt or copy of your invoice marked with the date of purchase is required before any warranty service will be rendered. You can obtain service by calling your vendor for a Returned Merchandise Authorization (RMA) number. When returning to the manufacturer, the RMA number should be prominently displayed on the outside of the shipping carton and the package should be mailed prepaid or hand-carried. Shipping and handling charges will be applied for all orders that must be mailed when service is complete.

This warranty only covers normal consumer use and does not cover damages incurred in shipping or from failure due to the alternation, misuse, abuse or improper maintenance of products.

During the warranty period, contact your distributor first for any product problems.

Chapter 4
AMIBIOS

4-1 Introduction

This chapter describes the AMIBIOS for the Intel 440GX Pentium II Xeon 450/400 MHz processors. The AMIBIOS is stored in the Flash EEPROM and can be easily upgraded using a DOS program.

System BIOS

BIOS is the Basic Input Output System used in all IBM® PC, XT™, AT®, and PS/2® compatible computers. WinBIOS is a high-quality example of a system BIOS.

Configuration Data

AT-compatible systems, also called ISA (Industry Standard Architecture), must have a place to store system information when the computer is turned off. The original IBM AT had 64 bytes of nonvolatile memory storage in CMOS RAM. All AT-compatible systems have at least 64 bytes of CMOS RAM, which is usually part of the Real-Time Clock. Many systems have 128 bytes of CMOS memory.

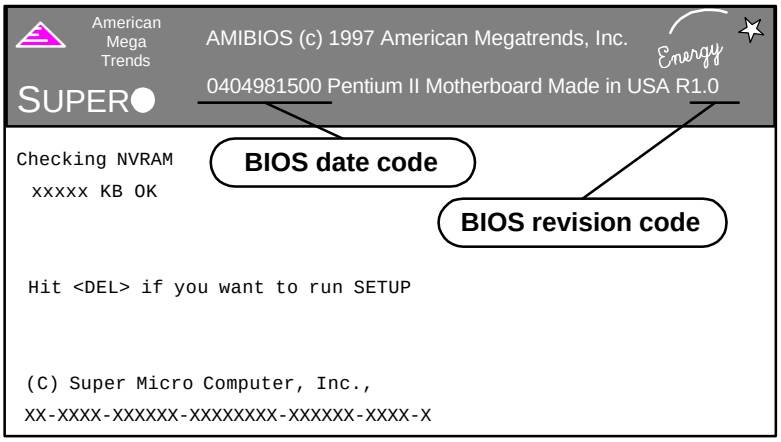
How Data Is Configured

AMIBIOS provides a setup utility in BIOS that is accessed by pressing <Del> at the appropriate time during system boot. Setup is used to configure the data in CMOS memory.

POST Memory Test

Normally, the only visible POST routine is the memory test. The screen that appears when the system is powered on is shown on the next page.

An AMIBIOS Identification string is displayed at the left bottom corner of the screen, below the copyright message.



4-2 BIOS Features:

- Supports Plug and Play v 1.0A and DMI 2.1
- Supports Intel PCI 2.1 (Peripheral Component Interconnect) local bus specification
- Supports Advanced Power Management (APM) specification v 1.1
- Supports xACP2
- Supports Flash ROM

AMIBIOS supports the LS120 drive made by Matsushita-Kotobuki Electronics Industries Ltd. The LS120 can be used as a boot device and is accessible as the next available floppy drive

AMIBIOS supports PC Health Monitoring chips. When the CPU temperature becomes too high, AMIBIOS can sound an alarm and turn on an overheat LED. The PC Health Monitoring chip monitors . . .

- CPU temperature
- chassis temperature
- the chassis intrusion detector
- five positive voltage inputs

- two negative voltage inputs
- three fan-speed monitor inputs

BIOS Configuration Summary Screen

AMIBIOS displays a screen that looks similar to the following when the POST routines complete successfully.

```
    AMIBIOS System Configuration (C) 1985-1997 American Megatrends Inc.,

 Main Processor      : Pentium(tm) II     Base Memory Size    : 640 KB
 Math Processor      : Built-In           Ext. Memory Size    : 64512 KB
 Floppy Drive A:     : 1.44 MB, 3 1/2     Display Type        : VGA/EGA
 Floppy Drive B:     : None               Serial Port(s)      : 3F8, 2F8
 AMI-BIOS Date       : 7/15/95            Parallel Port(s)    : 378
 Processor Clock     : 350MHz             External Cache      : 512 KB

 PCI Devices
 PCI Onboard PCI Bridge                   PCI Onboard Bridge Device
 PCI Onboard USB Controller               PCI Onboard IDE
 PCI Onboard SCSI, IRQ 10                 PCI Onboard SCSI, IRQ 10
 PCI Slot 4 VGA, IRQ 11
```

*Note: The picture above reflects a board equipped with SCSI, but may be taken as a general example.

AMIBIOS Setup

See the following page for examples of the AMIBIOS Setup screen, featuring options and settings. Figure 4-1 shows the Setup option highlighted. To highlight other options, use the arrow keys or the tab key to move to other option boxes. Figure 4-2 shows the settings for the Standard setup. Settings can be viewed by highlighting a desired option and pressing <Enter>. Use the arrow keys to choose a setting. Note: Optimal settings for all options can be set automatically. Go to the ***Optimal*** icon in the default box and press <Enter>. Use the arrow keys to highlight *Yes,* then press <Enter>.

Figure 4-1. Setup Option Highlighted

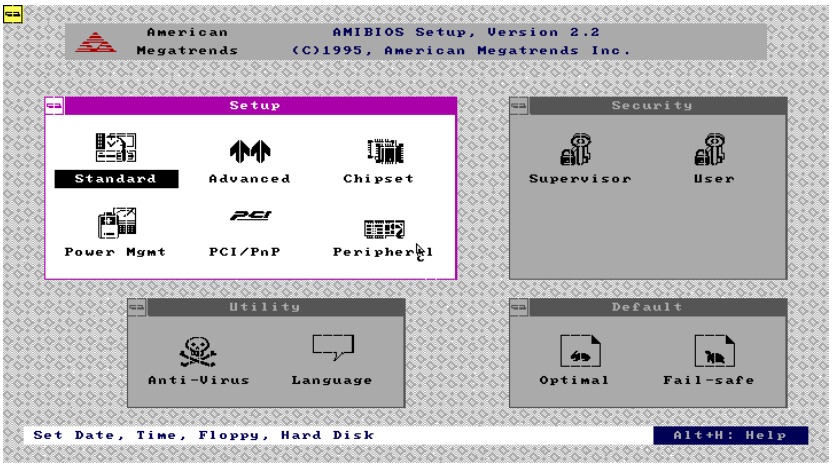
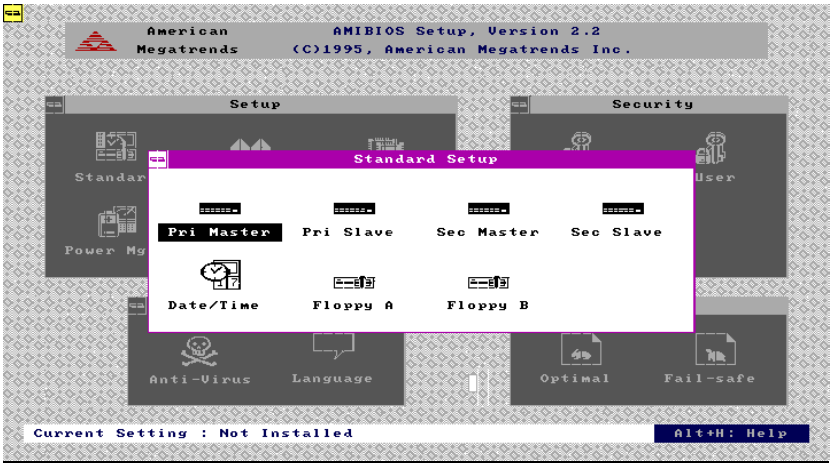


Figure 4-2. Settings for Standard Option



Chapter 5
Running Setup

The WinBIOS Setup options described in this section are selected by choosing the appropriate high-level icon from the Standard Setup screen. All icons displayed are described in this section, although the on-screen display is often all you need to understand how to set the options.

Optimal and Fail-Safe default settings are in bold text unless otherwise noted.

5-1 Setup

Standard Setup

Pri Master
Pri Slave
Sec Master
Sec Slave

Select these options to configure the drive specified in the option. Select *Auto Detect IDE* to let AMIBIOS automatically configure the drive. A screen with a list of drive parameters then appears. Click on *OK* to configure the drive.

Type	How to Configure
SCSI	Select *Type*. Select *Not Installed* on the drive parameter screen. The SCSI drivers provided by the SCSI manufacturer should allow you to configure the SCSI drive.
IDE	Select *Type*. Select *Auto* to let AMIBIOS determine the parameters. Click on *OK* when AMIBIOS displays the drive parameters. Select *LBA Mode*. Select *On* if the drive has a capacity greater than 540 MB. Select the *Block Mode*. Select *On* to allow block-mode data transfers. Select the *32-bit mode*. Select *On* to allow 32-bit data transfers. Select *PIO mode*. Select *On* to allow AMIBIOS to determine the PIO Mode. It

	is best to select *Auto* to allow AMIBIOS to determine the PIO mode. If you select a PIO mode that is not supported by the IDE drive, the drive will not work properly. If you are absolutely certain that you know the drive's PIO mode, select PIO mode 0-4, as appropriate.
CD ROM	Select *Type*. Select *CDROM*. Click on OK when AMIBIOS displays the drive parameters.

Entering Drive Parameters

You can also enter the hard disk drive parameters. The drive parameters are:

Parameter	Description
Type	The number of a drive with certain identification parameters.
Cylinders	The number of cylinders in the disk drive.
Heads	The number of heads.
Write Precompensation	The size of sectors get progressively smaller as the track diameter diminishes. Yet each sector must still hold 512 bytes. Write precompensation circuitry on the hard disk compensates for the physical difference in sector size by boosting the write current for sectors on inner tracks. This parameter states the track number where write precompensation begins.
Sectors	The number of sectors per track. MFM drives have 17 sectors per track. RLL drives have 26 sectors per track. ESDI drives have 34 sectors per track. SCSI and IDE drives may have even more sectors per track.
Capacity	The capacity of the formatted drive is (Number of heads) x (Number of cylinders) x (Number of sectors per track) x (512 bytes per sector)

Date and Time Configuration

Select the Standard option. Select the *Date/Time* icon. The current values for each category are displayed. Enter new values with the keyboard.

Floppy A
Floppy B

Choose the Floppy Drive A or B icon to specify the floppy drive type. The settings are *Not Installed, 360 KB 5¼ inch*, *1.2 MB 5¼ inch*, *720 KB 3½ inch*, *1.44 MB 3½ inch* or *2.88 MB 3½ inch*. ***Note: The Optimal and Fail-Safe settings for Floppy Drive A is 1.44 MB 3 1/2 inch and for Floppy Drive B is Not Installed***.

Advanced Setup

Quick Boot

The settings are ***Disabled*** or *Enabled*. Set to *Enabled* to permit AMIBIOS to boot quickly when the computer is powered on. This option replaces the old "Above 1 MB Memory Test Advanced Setup" option. The settings are:

Setting	Description
Disabled	AMIBIOS tests all system memory. AMIBIOS waits for up to 40 seconds for a READY signal from the IDE hard disk drive. AMIBIOS waits for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. AMIBIOS checks for a <Del> key press and runs AMIBIOS Setup if the key has been pressed.
Enabled	AMIBIOS does not test system memory above 1 MB. AMIBIOS does not wait for up to 40 seconds for a READY signal from the IDE hard disk drive. If a READY signal is not received immediately from the IDE drive, AMIBIOS does not configure that drive. AMIBIOS does not wait for .5 seconds after sending a RESET signal to the IDE drive to allow the IDE drive time to get ready again. In *Enabled,* the keyboard will be bypassed.

Pri Master ARMD Emulated as
Pri Slave ARMD Emulated as
Sec Master ARMD Emulated as
Sec Slave ARMD Emulated as
The options for Pri Master ARMD Emulated as, Pri Slave ARMD Emulated as, Sec Master ARMD Emulated as and Sec Slave ARMD Emulated as are ***Auto***, *Floppy* or *Hard disk*.

1st Boot Device
2nd Boot Device
3rd Boot Device
The options for the 1st Boot Device are *Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD,* ***Floppy****, ARMD-FDD, ARMD-HDD, ATAPI CD ROM, SCSI, Network* or *I_20*. The options for the 2nd Boot Device are *Disabled,* ***1st IDE-HDD****, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD* or *ATAPI CD ROM*. The options for the 3rd Boot Device are *Disabled, 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD, 4th IDE-HDD, Floppy, ARMD-FDD, ARMD-HDD* or ***ATAPI CD ROM***.

The 1st IDE-HDD, 2nd IDE-HDD, 3rd IDE-HDD and 4th IDE-HDD are the four hard disks that can be installed by the BIOS. The 1st IDE-HDD is the first hard disk installed by the BIOS, the 2nd IDE-HDD is the second hard disk, and so on. For example, if the system has a hard disk connected to the Primary Slave and another hard disk connected to the Secondary Master, then the 1st IDE-HDD will be referred to as the hard disk connected to the Primary Slave and the 2nd IDE-HDD will be referred to as the hard disk connected to the Secondary Master. The 3rd IDE-HDD and 4th IDE-HDD are not present. Note that the order of initializing the devices connected to the primary and secondary channels are Primary Master first, Primary Slave second, Secondary Master third and Secondary Slave fourth.

The BIOS will attempt to read the boot record from the 1st, 2nd, 3rd and 4th boot devices in the selected order until it is successful in reading the boot record. The BIOS will not attempt to boot from any device which is not selected as the boot device.

Try Other Boot Device
This option controls the action of the BIOS if all the selected boot devices failed to boot. The settings for this option are ***Yes*** or *No*. If *Yes* is selected and all the selected boot devices failed to boot, the BIOS will try to boot from the other boot devices (in a predefined sequence) which are present but not selected as boot devices in the setup (and hence have

not yet been tried for booting). If selected as *No* and all selected boot devices failed to boot, the BIOS will not try to boot from the other boot devices which may be present but not selected as boot devices in setup.

Initial Display Mode

This option determines the screen that the POST will display first. The settings for this option are ***BIOS*** or *Silent*. If selected as *BIOS,* the POST will start with the normal sign-on message screen. If *Silent* is selected, the POST will start with a silent screen.

Display Mode at Add-on ROM Init

This option determines the display mode during add-on ROM (except for Video add-on ROM) initialization. The settings for this option are ***Force BIOS*** or *Keep Current*. If selected as *Force BIOS,* the POST will force the display to be changed to BIOS mode before giving control to any add-on ROM. If no add-on ROM is found, then the current display mode will remain unchanged even if this setup question is selected as *Force BIOS.* If selected as *Keep Current,* then the current display mode will remain unchanged.

Floppy Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

Hard Disk Access Control

The settings for this option are ***Read-Write*** or *Read-Only*.

S.M.A.R.T. for Hard Disks

S.M.A.R.T. (Self-Monitoring, Analysis and Reporting Technology) is a technology developed to manage the reliability of hard disks by predicting future device failures. The hard disk must be S.M.A.R.T. capable. The settings for this option are ***Disabled*** or *Enabled*. ****Note: S.M.A.R.T. cannot predict all future device failures. S.M.A.R.T. should be used as a warning tool, not as a tool to predict device reliability***.

Boot Up Num-Lock

The settings for this option are ***On*** or *Off*. When this option is set to *On*, the BIOS turns on the Num Lock key when the system is powered on. This will enable the end user to use the number keys on the numeric keypad.

PS/2 Mouse Support

The settings for this option are ***Enabled*** or *Disabled*. When this option is set to *Enabled*, AMIBIOS supports a PS/2-type mouse.

Primary Display
This option specifies the type of display adapter card installed in the system. The settings are *Absent,* ***VGA/EGA***, *CGA40x25*, *CGA80x25* or *Mono*.

Password Check
This option enables the password check option every time the system boots or the end user runs WinBIOS Setup. If *Always* is chosen, a user password prompt appears every time the computer is turned on. If ***Setup*** is chosen, the password prompt appears if WinBIOS Setup is executed.

Boot to OS/2
If the DRAM size is over 64 MB, set this option to *Yes* to permit AMIBIOS to run with IBM OS/2. The settings are ***No*** or *Yes*.

Internal Cache
This option is for enabling or disabling the internal cache memory. The settings for this option are *Disabled* or ***WriteBack***.

System BIOS Cacheable
When set to *Enabled*, the contents of the F0000h system memory segment can be read from or written to cache memory. The contents of this memory segment are always copied from the BIOS ROM to system RAM for faster execution. The settings are *Enabled* or *Disabled*. ***Note: The Optimal default setting is Enabled and the Fail-Safe default setting is Disabled. Set this option to Enabled to permit the contents of the F0000h RAM memory segment to be written to and read from cache memory.***

CPU ECC
The settings for this option are ***Enabled*** or *Disabled*. This option enables the Pentium II L2 cache ECC function.

MPS Revision
The settings for this option are 1.1 or **1.4**.

C000, 16K Shadow
C400, 16K Shadow
These options specify how the 32 KB of video ROM at C0000h is treated. The settings are *Disabled*, *Enabled* or ***Cached***. When set to *Disabled,* the contents of the video ROM are not copied to RAM. When set to *Enabled,* the contents of the video ROM area from C0000h-C7FFFh are

copied (shadowed) from ROM to RAM for faster execution. When set to *Cached*, the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM, and can be written to or read from cache memory.

C800, 16K Shadow
CC00, 16K Shadow
D000, 16K Shadow
D400, 16K Shadow
D800, 16K Shadow
DC00, 16K Shadow

These options enable shadowing of the contents of the ROM area specified in the option. The ROM area not used by ISA adapter cards is allocated to PCI adapter cards. The settings are ***Disabled*****,** *Enabled* or *Cached*. When set to *Disabled,* the contents of the video ROM are not copied to RAM. When set to *Enabled,* the contents of the video ROM area from C0000h-C7FFFh are copied (shadowed) from ROM to RAM for faster execution. When set to *Cached,* the contents of the video ROM area from C0000h-C7FFFh are copied from ROM to RAM and can be written to or read from cache memory.

Chipset Setup

USB Function

The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the USB (Universal Serial Bus) functions.

USB KB/Mouse Legacy Support

The settings for this option are *Keyboard, Auto, Keyboard+Mouse* or ***Disabled***. Set this option to *Enabled* to enable the USB keyboard and mouse.

Port 64/60 Emulation

The settings for this option are *Enabled* or ***Disabled***.

SERR# (System Error)

The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the SERR# signal on the bus. GX asserts this signal to indicate a system error condition. SERR# is asserted under the following conditions:

- In an ECC configuration, the GX asserts SERR# for single bit (correctable) ECC errors or multiple bit (non-correctable) ECC errors if SERR# signaling is enabled via the ERRCMD control register. Any ECC errors received during initialization should be ignored.

- The GX asserts SERR# for one clock when it detects a target abort during a GX-initiated PCI cycle .
- The GX can also assert SERR# when a PCI parity error occurs during the address or data phase.
- The GX can assert SERR# when it detects a PCI address or data parity error on the AGP.
- The GX can assert SERR# upon the detection of access to an invalid entry in the Graphics Aperture Translation Table.
- The GX can assert SERR# upon detecting an invalid AGP master access outside of the AGP aperture and outside of the main DRAM range (i.e. in the 640k -1M range or above TOM).
- The GX can assert SERR# upon detecting an invalid AGP master access outside of the AGP aperture.
- The GX asserts SERR# for one clock when it detects a target abort during a GX-initiated AGP cycle.

PERR#

This option is to signal the occurrence of data parity errors on the PCI bus. The settings are *Enabled* or ***Disabled***. Set to *Enabled* to enable the PERR# signal.

WSC# Handshake (Write Snoop Complete)

This signal is asserted active to indicate that all the snoop activity on the CPU bus on behalf of the last PCI-DRAM write transaction is complete and that it is safe to send the APIC interrupt message. The settings for this option are ***Enabled*** or *Disabled*. Set to *Enabled* to enable handshaking for the WSC# signal.

USWC Write Post

The settings for this option are ***Enabled*** or *Disabled*. This option sets the status of USWC (Uncacheable, Speculative or Write-Combining) posted writes and is used to combine several partial writes to the frame buffer into a single write to reduce the data bus traffic. Set to *Enabled* to enable USWC posted writes to I/O. Set to *Disabled* to disable USWC posted writes to I/O.

BX/GX Master Latency Timer (CLKs)

This option specifies the master latency timings (in PCI clocks) for devices in the computer. It defines the number of PCI clocks a PCI master can own on the bus after the PCI central arbiter removes the grant signal. The settings are *Disabled*, *32*, ***64***, *96*, *128*, *160*, *192* or *224*.

Multi-Trans Timer (CLKs)

This option specifies the multi-trans latency timings (in PCI clocks) for devices in the computer. It is used to reduce overhead switching between different masters. The settings are *Disabled*, ***32***, *64*, *96*, *128*, *160*, *192* or *224*.

PCI1 to PCI0 Access

The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable access between two different PCI buses (PCI1 and PCI0).

Memory Autosizing Support

The BIOS can dynamically detect and size SDRAM and EDO in a system populated with memory that has no SPD information. Set to *Enable* for memory that does not have SPD information or to bypass the SPD. The settings for this option are ***Auto*** or *Enable*.

DRAM Integrity Mode

The settings for this option are ***None***, *EC* or *ECC Hardware*. ***Note: For ECC memory only. See the table below to set the type of system memory checking.*** (Note: New BIOS versions automatically detect this setting so the user does not need to set it.)

Setting	Description
None	No error checking or error reporting is done.
EC	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset. Corrected bits of data from memory are not written back to DRAM system memory.
ECC Hardware	Multibit errors are detected and reported as parity errors. Single-bit errors are corrected by the chipset and written back to DRAM system memory. If a soft (correctable) error occurs, writing the fixed data back to DRAM system memory will resolve the problem. Most DRAM errors are soft errors. If a hard (uncorrectable) error occurs, writing the fixed data back to DRAM system memory does not solve the problem. In this case, the second time the error occurs in the same location, a Parity Error is reported, indicating an uncorrectable error. If ECC is selected, AMIBIOS automatically enables the System Management Interface (SMI). If you do not want to enable power management, set the **Power Management/APM** option to *Disabled* and set all Power Management Setup timeout options to

Disabled. To enable power management, set **Power Management/APM** to *Enabled* and set the power management timeout options as desired.

DRAM Refresh Rate
This option specifies the interval between refresh signals to DRAM system memory. The settings for this option are ***15.6 us*** (microseconds), *31.2 us*, *62.4 us*, *124.8 us* or *249.6 us*.

Memory Hole
This option specifies the location of an area of memory that cannot be addressed on the ISA bus. The settings are ***Disabled***, *15 MB-16 MB* or *512 KB-640 KB*.

SDRAM CAS# Latency
This option regulates the column address strobe. The settings are 2 SCLKs, 3 SCLKs or ***Auto***.

SDRAM RAS# to CAS# Delay
This option specifies the length of the delay inserted between the RAS and CAS signals of the DRAM system memory access cycle if SDRAM is installed. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs* or *3 SCLKs*. ***Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs***.

SDRAM RAS# Precharge
This option specifies the length of the RAS precharge part of the DRAM system memory access cycle when Synchronous DRAM system memory is installed in the computer. The settings are *Auto* (AMIBIOS automatically determines the optimal delay), *2 SCLKs or 3 SCLKs*. ***Note: The Optimal default setting is Auto and the Fail-Safe default setting is 3 SCLKs.***

Power Down SDRAM
GX supports an SDRAM Power Down mode to minimize SDRAM power usage. The settings for this option are *Enabled* or ***Disabled***. The *Enabled* setting enables the SDRAM Power Down feature.

ACPI Control Register
The settings for this option are *Enabled* or ***Disabled***. Set this option to *Enabled* to enable the ACPI (Advanced Configuration and Power Interface) control register.

Gated Clock

Signal GCLKEN enables internal dynamic clock gating in the GX when an AGPset "IDLE" state occurs. This happens when the GX detects an idle state on all its buses. The settings for this option are ***Enabled*** or *Disabled*. The *Enabled* setting enables the gated clock.

Graphics Aperture Size

This option specifies the amount of system memory that can be used by the Accelerated Graphics Port (AGP). The settings are *4 MB*, *8 MB*, *16 MB*, *32 MB*, ***64 MB***, *128 MB* or *256 MB*.

Search for MDA (Monochrome Adapter) Range (B0000h-B7FFFh) Resources

Legacy support requires the ability to have a second graphics controller (monochrome) in the system. In an AGP system, accesses in the normal VGA range are forwarded to the AGP bus. Since the monochrome adapter may be on the PCI (or ISA) bus, the GX must decode cycles in the MDA range and forward them to PCI. The settings for this option are ***Yes*** or *No*. Set this option to *Yes* to let AMIBIOS search for MDA resources.

AGP Multi-Trans Timer (AGP CLKs)

This option sets the AGP multi-trans timer. The settings are in units of AGP clocks: ***32***, *64*, *96*, *128*, *160*, *192* or *224*.

AGP Low-Priority Timer

This option controls the minimum tenure on the AGP for low priority read and write data transactions. The settings are *Disabled, **32**, 64, 96, 128, 160, 192* or *224*.

AGP SERR (Advanced Graphic Port System Error)

GX asserts this signal to indicate an AGP system error condition. The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the AGP SERR# signal.

AGP Parity Error Response

The settings for this option are *Enabled* or ***Disabled***. Set to *Enabled* to enable the AGP (Accelerated Graphics Port) to respond to parity errors.

8-bit I/O Recovery Time
This option specifies the length of the delay inserted between consecutive 8-bit I/O operations. The settings are ***Disabled***, *1 SYSCLK*, *2 SYSCLKs*, *3 SYSCLKs*, *4 SYSCLKs*, *5 SYSCLKs*, *6 SYSCLKs*, *7 SYSCLKs* or *8 SYSCLKs*.

16-bit I/O Recovery Time
This option specifies the length of the delay inserted between consecutive 16-bit I/O operations. The settings are ***Disabled***, *1 SYSCLK*, *2 SYSCLKs*, *3 SYSCLKs*, *4 SYSCLKs*, *5 SYSCLKs*, *6 SYSCLKs*, *7 SYSCLKs* or *8 SYSCLKs*.

PIIX4 SERR#
This signal is asserted to indicate a PIIX4 System Error condition. The settings for this option are *Enabled* or ***Disabled***. The *Enabled* option enables the SERR# signal for the Intel PIIX4 chip.

USB Passive Release
GX releases the USB bus when idle to maximize USB bus usage. The settings for this option are ***Enabled*** or *Disabled*. Set this option to *Enabled* to enable passive release for USB.

PIIX4 Passive Release
This option functions similarly to the USB Passive Release. The settings for this option are ***Enabled*** or *Disabled*. Set to *Enabled* to enable passive release for the Intel PIIX4 chip.

PIIX4 Delayed Transaction
GX is capable of PIIX4 transactions to improve PIIX4 interrupt efficiency. The settings for this option are ***Enabled*** or *Disabled*. Set this option to *Enabled* to enable delayed transactions for the Intel PIIX4 chip.

Type F DMA Buffer Control1
Type F DMA Buffer Control2
These options specify the DMA channel where Type F buffer control is implemented. The settings are ***Disabled***, *Channel-0*, *Channel-1*, *Channel-2*, *Channel-3*, *Channel-4*, *Channel-5*, *Channel-6* or *Channel-7*.

DMA0 Type
DMA1 Type
DMA2 Type
DMA3 Type
DMA5 Type

DMA6 Type
DMA7 Type
These options specify the bus that the specified DMA channel can be used on. The settings are *PC/PCI*, *Distributed* or ***Normal ISA***.

Memory Buffer Strength
The settings for this option are ***Strong***, *Median* or *Auto*.

Manufacturer's Setting
Note: The user should always set this option to Mode 0. All other modes are for factory testing only.

Power Management

Power Management
The settings for this feature are ***APM***, *ACPI* or *Disabled*. Set to *APM* to enable the power conservation feature specified by Intel and Microsoft INT 15h Advance Power Management BIOS functions. Set to *ACPI* if your operating system supports Microsoft's Advanced Configuration and Power Interface (ACPI) standard.

Power Button Function
This option specifies how the power button mounted externally on the computer chassis is to be used. The settings are *Suspend* or ***On/Off***. When set to *On/Off*, pushing the power button turns the computer on or off. When set to *Suspend*, pushing the power button places the computer in Suspend mode or in Full-On power mode.

Green PC Monitor Power State
This option specifies the power state that the green PC-compliant video monitor enters when AMIBIOS places it in a power-saving state after the specified period of display inactivity has expired. The settings are *Standby*, *Suspend* or *Off*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe setting is Standby***.

Video Power Down Mode
This option specifies the power-conserving state that the VGA video subsystem enters after the specified period of display inactivity has expired. The settings are *Disabled*, *Standby* or *Suspend*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled***.

Hard Disk Power Down Mode
This option specifies the power conserving state that the hard disk drive enters after the specified period of hard drive inactivity has expired. The settings are *Disabled*, *Standby* or *Suspend*. ***Note: The Optimal default setting for this option is Suspend and the Fail-Safe default setting is Disabled***.

Hard Disk Timeout (Minutes)
This option specifies the length of a period of hard disk drive inactivity. When this length of time expires, the computer enters the power-conserving state specified in the Hard Disk Power Down Mode option. The settings are ***Disabled*** and *1 Min through 15 Min in 1 minute intervals*.

Power Saving Type
The settings for this option are ***Sleep***, *Stop Clock* or *Deep Sleep*.

Standby/Suspend Timer Unit
This allows you to set the standby timeout and suspend timeout timer unit. The settings are *32 secs*, *4 msecs*, ***4 min*** or *4 secs*.

Standby Timeout
This option specifies the length of a period of system inactivity while in the full power-on state. When this length of time expires, the computer enters the standby power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Suspend Timeout (Minutes)
This option specifies the length of a period of system inactivity while in standby state. When this length of time expires, the computer enters the suspend power state. The settings are ***Disabled*** and *4 Min through 508 Min in 4 minute intervals*.

Slow Clock Ratio
The value of the slow clock ratio indicates the percentage of time the STPCLK# signal is asserted while in the thermal throttle mode. The settings are *Disabled, 0-12.5%, 12.5-25%, 25-37.5%, 37.5-50%,* ***50-62.5%***, *62.5-75%* or *75-87.5%*.

Display Activity
This option specifies if AMIBIOS is to monitor display activity for power conservation purposes. When this option is set to *Monitor* and there is

no display activity for the length of time specified in the Standby Timeout (Minute) option, the computer enters a power-saving state. The settings are *Monitor* or ***Ignore***.

Device 6 (Serial port 1)
Device 7 (Serial port 2)
Device 8 (Parallel port)
Device 5 (Floppy disk)
Device 0 (Primary Master IDE)
Device 1 (Primary Slave IDE)
Device 2 (Secondary Master IDE)
Device 3 (Secondary Slave IDE)
When set to *Monitor*, these options enable event monitoring on the specified hardware interrupt request line. If set to Monitor and the computer is in a power-saving state, AMIBIOS watches for activity on the specified IRQ line. The computer enters the Full-On state if any activity occurs. AMIBIOS reloads the Standby and Suspend timeout timers if activity occurs on the specified IRQ line. ***Note: The Optimal default setting for each option is Ignore with the exception of Devices 0 (Primary Master IDE) and 6 (Serial Port 1), which should be set to Monitor. The Fail-Safe default for each option is Monitor.***

LAN Wake-Up
RTC Wake-UP
The options for LAN Wake-Up and RTC Wake-Up are ***Disabled*** or *Enabled*. When enabled, the **Hour** and **Minute** functions become available.

PCI/PnP Setup

Plug and Play-Aware OS
The settings for this option are ***No*** or *Yes*. Set this option to *Yes* if the operating system in the computer is aware of and follows the Plug and Play specifications. AMIBIOS only detects and enables PnP ISA adapter cards that are required for system boot. Currently, only Windows 95 and Windows 98 are PnP-Aware. Set this option to *No* if the operating system (such as DOS, OS/2 or Windows 3.x) does not use PnP. You must set this option correctly. Otherwise, PnP-aware adapter cards installed in the computer will not be configured properly.

PCI Latency Timer (PCI Clocks)
This option specifies the latency timings in the PCI clocks for all PCI devices. The settings are *32*, ***64***, *96*, *128*, *160*, *192*, *224* or *248*.

PCI VGA Palette Snoop
The settings for this option are ***Disabled*** or *Enabled.* When set to *Enabled,* multiple VGA devices operating on different buses can handle data from the CPU on each set of palette registers on every video device. Bit 5 of the command register in the PCI device configuration space is the VGA Palette Snoop bit (0 is disabled). For example, if there are two VGA devices in the computer (one PCI and one ISA) and this option is disabled, data read and written by the CPU is directed only to the PCI VGA device's palette registers. If enabled, data read and written by the CPU is directed to both the PCI VGA device's palette registers and the ISA VGA palette registers. This will permit the palette registers of both devices to be identical. This option must be set to *Enabled* if any ISA adapter card installed in the system requires VGA palette snooping.

PCI IDE Busmaster
The settings for this option are ***Disabled*** or *Enabled*. Set to *Enabled* to specify that the IDE Controller on the PCI bus has bus mastering capabilities. Under Windows 95, you should set this option to *Disabled* and install the Bus Mastering driver.

Offboard PCI IDE Card
This option specifies if an offboard PCI IDE controller adapter card is installed in the computer. The PCI expansion slot on the motherboard where the offboard PCI IDE controller is installed must be specified. If an offboard PCI IDE controller is used, the onboard IDE controller is automatically disabled. The settings are ***Auto*** (AMIBIOS automatically determines where the offboard PCI IDE controller adapter card is installed), *Slot 1*, *Slot 2*, *Slot 3*, *Slot 4, Slot 5* or *Slot 6*.

This option forces IRQ14 and IRQ15 to a PCI slot on the PCI local bus. This is necessary to support non-compliant ISA IDE controller adapter cards. If an offboard PCI IDE controller adapter card is installed in the computer, you must also set the Offboard PCI IDE Primary IRQ and Offboard PCI IDE Secondary IRQ options.

Offboard PCI IDE Primary IRQ
Offboard PCI IDE Secondary IRQ
These options specify the PCI interrupt used by the primary (or secondary) IDE channel on the offboard PCI IDE controller. The settings are ***Disabled***, *Hardwired*, *INTA*, *INTB*, *INTC* or *INTD*.

PCI Slot1 IRQ Priority
PCI Slot2 IRQ Priority
PCI Slot3 & 5 IRQ Priority
PCI Slot4 IRQ Priority
These options specify the IRQ priority for PCI devices installed in the PCI expansion slots. The settings are ***Auto****, (IRQ) 3, 4, 5, 7, 9, 10,* or *11, in priority order***.**

DMA Channel 0
DMA Channel 1
DMA Channel 3
DMA Channel 5
DMA Channel 6
DMA Channel 7
These DMA channels control the data transfer between the I/O devices and the system memory. The chipset allows the BIOS to choose which channels to do the job. The settings are ***PnP*** or *ISA/EISA.*

IRQ3
IRQ4
IRQ5
IRQ7
IRQ9
IRQ10
IRQ11
IRQ12
IRQ14
IRQ15
These options specify which bus the specified IRQ line is used on and allows you to reserve IRQs for legacy ISA adapter cards. If more IRQs must be removed from the pool, the end user can use these options to reserve the IRQ by assigning an *ISA/EISA* setting to it. The onboard I/O is configured by AMIBIOS. All IRQs used by the onboard I/O are configured as PCI/PnP.

IRQ14 and 15 will not be available if the onboard PCI IDE is enabled. If all IRQs are set to *ISA/EISA* and IRQ14 and 15 are allocated to the onboard PCI IDE, IRQ 9 will still be available for PCI and PnP devices. This is because at least one IRQ must be available for PCI and PnP devices. The settings are ***PCI/PnP*** or *ISA/EISA.*

Reserved Memory Size
This option specifies the size of the memory area reserved for legacy ISA adapter cards. The settings are ***Disabled***, *16K*, *32K* or *64K*.

Reserved Memory Address
This option specifies the beginning address (in hex) of the reserved memory area. The specified ROM memory area is reserved for use by legacy ISA adapter cards. The settings are *C0000*, *C4000*, ***C8000***, *CC000*, *D0000*, *D4000*, *D8000* or *DC000*.

PCI Device Search Order
This option specifies the direction the PCI buses will be scanned. The settings are ***First-Last*** and *Last-first.*

Default Primary Video
This feature supports multiple displays. The settings are ***AGP*** or *PCI*.

Peripheral Setup

Onboard SCSI
The settings for this option are ***Enabled*** or *Disabled*. When set to *Enabled,* this option enables the Adaptec 7896 BIOS.

Remote Power On
Microsoft's Memphis OS supports this feature that can wake-up the system from a SoftOff state through devices (such as an external modem) that are connected to COM1 or COM2. The settings are ***Disabled*** or *Enabled*.

CPU1 Current Temperature
The current temperature of CPU1 is displayed in this option.

CPU2 Current Temperature
The current temperature of CPU2 is displayed in this option.

CPU Overheat Warning
The settings for this option are *Enabled* or ***Disabled***. When set to *Enabled,* this option allows the user to set an overheat warning temperature.

CPU Overheat Warning Temperature
Use this option to set the CPU overheat warning temperature. The settings are *25°C through 75°C in 1°C intervals*. ***Note: The Optimal and Fail-Safe default settings are 55°C***.

H/W Monitor In0 (CPU 1)
H/W Monitor In1 (CPU 2)
H/W Monitor In2 (+3.3V)
H/W Monitor In3 (+5V)
H/W Monitor In4 (+12V)
H/W Monitor In5 (-12V)
H/W Monitor In6 (-5V)
CPU1 Fan
CPU2 Fan
Thermal Control Fan
The above features are for PC Health Monitoring. Motherboards with W83781D have seven onboard voltage monitors for the CPU core, the CPU I/O, +3.3V, +5V, -5V, +12V and -12V, and three fan-status monitors.

Onboard FDC
This option enables the FDC (Floppy Drive Controller) on the motherboard. The settings are *Auto* (AMIBIOS automatically determines if the floppy controller should be enabled), *Disabled* or ***Enabled***.

Onboard Serial PortA
This option specifies the base I/O port address of serial port 1. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, ***3F8h*/COM1**, *2F8h/COM2*, *3E8h/COM3* or *2E8h/COM4*.

Onboard Serial PortB
This option specifies the base I/O port address of serial port 2. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, *3F8h/COM1*, ***2F8h/COM2***, *3E8h/COM3* or *2E8h/COM4*.

Serial PortB Mode
The settings for this option are ***Normal***, *IrDA* or *ASK IR*. When set to *IrDA,* the IR Duplex Mode becomes available and can be set to either Half or Full. When set to *ASK IR,* the IrDA Protocol becomes available and can be set to 1.6 us or 3/16.

Onboard Parallel Port
This option specifies the base I/O port address of the parallel port on the motherboard. The settings are *Auto* (AMIBIOS automatically determines the correct base I/O port address), *Disabled*, ***378***, *278* or *3BC*.

Parallel Port Mode
This option specifies the parallel port mode. The settings are *Normal*, *Bi-Dir*, *EPP* or *ECP*. When set to *Normal,* the normal parallel port mode is used. Use *Bi-Dir* to support bidirectional transfers. Use *EPP* (Enhanced Parallel Port) to provide asymmetric bidirectional data transfer driven by the host device. Use *ECP* (Extended Capabilities Port) to achieve data transfer rates of up to 2.5 Mbps. ECP uses the DMA protocol and provides symmetric bidirectional communication. ***Note: The Optimal default setting for this option is ECP and the Fail-Safe setting is Normal***.

EPP Version
The settings are *1.7* or *1.9*. ***Note: The Optimal and Fail-Safe default settings are N/A***.

Parallel Port IRQ
This option specifies the IRQ to be used by the parallel port. The settings are ***Auto***, *5* or *7*.

Parallel Port DMA Channel
This option is only available if the setting of the parallel port mode option is *ECP*. The settings are *0*, *1*, *2*, *3*, *5*, *6* or *7*. ***Note: The option is N/A***.

Onboard IDE
This option specifies the onboard IDE controller channels to be used. The settings are *Disabled, Primary*, *Secondary* or ***Both***.

5-2 Security Setup

Supervisor/User

The system can be configured so that all users must enter a password every time the system boots or whenever the WINBIOS setup is executed. You can set either a Supervisor password or a User password. If you do not want to use a password, just press <Enter> when the password prompt appears.

The password check option is enabled in the Advanced Setup by choosing either *Always* or *Setup*. The password is stored in CMOS RAM. You can enter a password by typing the password on the keyboard or by selecting each letter via the mouse or a pen stylus. Pen access must be customized for each specific hardware platform.

When you select Supervisor or User, AMIBIOS prompts for a password. You must set the Supervisor password before you can set the User password. Enter a 1-6 character password. The password does not appear on the screen when typed. Retype the new password as prompted and press <Enter>. Make sure you write it down. If you forget it, you must clear CMOS RAM and reconfigure.

5-3 Utility Setup

Anti-Virus

When this icon is selected, AMIBIOS issues a warning when any program (or virus) issues a disk format command or attempts to write to the boot sector of the hard disk drive. The settings are *Enabled* or ***Disabled***.

Language

Note: The Optimal and Fail-Safe default settings for this option are English.

5-4 Default Settings

Every option in the WinBIOS Setup contains two default settings: a Fail-Safe default, and an Optimal default.

Optimal Default

The Optimal default settings provide optimum performance settings for all devices and system features.

Fail-Safe Default

The Fail-Safe default settings consist of the safest set of parameters. Use them if the system is behaving erratically. They should always work but do not provide optimal system performance characteristics.

Notes

Appendix A
BIOS Error Beep Codes & Messages

During the POST (Power-On Self-Test) routines, which are performed each time the system is powered on, errors may occur.

Nonfatal errors are those which, in most cases, allow the system to continue the boot-up process. The error messages normally appear on the screen.

Fatal errors are those which will not allow the system to continue the boot-up procedure. If a fatal error occurs, you should consult with your system manufacturer for possible repairs.

These fatal errors are usually communicated through a series of audible beeps. The numbers on the fatal error list, on the following page, correspond to the number of beeps for the corresponding error. All errors listed, with the exception of #8, are fatal errors.

Beeps	Error message	Description
1	Refresh Failure	The memory refresh circuitry on the motherboard is faulty.
2	Parity Error	A parity error was detected in the base memory (the first 64 KB block) of the system.
3	Base 64 KB Memory Failure	A memory failure occurred within the first 64 KB of memory.
4	Timer Not Operational	A memory failure was detected in the first 64 KB of memory, or Timer 1 is not functioning.
5	Processor Error	The CPU on the system board generated an error.
6	8042 - Gate A20 Failure	The keyboard controller (8042) contains the Gate A20 switch which allows the CPU to operate in virtual mode. This error means that the BIOS cannot switch the CPU into protected mode.
7	Processor Exception Interrupt Error	The CPU on the motherboard generated an exception interrupt.
8	Display Memory Read/Write Error	The system video adapter is either missing or its memory is faulty. ***Please Note:*** This is not a fatal error.
9	ROM Checksum Error	The ROM checksum value does not match the value encoded in the BIOS.
10	CMOS Shutdown Register Read/Write Error	The shutdown register for CMOS memory has failed.

Refer to the table on page A-3 for solutions to the error beep codes.

If it beeps...	**then ...**
1, 2, 3 times	reseat the DIMM memory. If the system still beeps, replace the memory.
6 times	reseat the keyboard controller chip. If it still beeps, replace the keyboard controller. If it still beeps, try a different keyboard, or replace the keyboard fuse, if the keyboard has one.
8 times	there is a memory error on the video adapter. Replace the video adapter, or the RAM on the video adapter.
9 times	the BIOS ROM chip is bad. The system probably needs a new BIOS ROM chip.
4, 5, 7, or 10 times	the motherboard must be replaced.

Error Message	Information
8042 Gate -- A20 Error	Gate A20 on the keyboard controller (8042) is not working. Replace the 8042.
Address Line Short!	Error in the address decoding circuitry on the motherboard.
C: Drive Error	Hard disk drive C: does not respond. Run the Hard Disk Utility to correct this problem. Also, check the C: hard disk type in Standard Setup to make sure that the hard disk type is correct.
C: Drive Failure	Hard disk drive C: does not respond. Replace the hard disk drive.
Cache Memory Bad	Cache memory is defective. Replace it. Do Not Enable Cache!
CH-2 Timer Error	Most ISA computers include two times. There is an error in time 2.
CMOS Battery State Low	CMOS RAM is powered by a battery. The battery power is low. Replace the battery.
CMOS Checksum Failure	After CMOS RAM values are saved, a checksum value is generated for error checking. The previous value is different from the current value. Run WINBIOS Setup or AMIBIOS Setup.
CMOS System Option Not Set	The values stored in CMOS RAM are either corrupt or nonexistent. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Display Type Mismatch	The video type in CMOS RAM does not match the type detected by the BIOS. Run WINBIOS Setup or AMIBIOS Setup.
CMOS Memory Size Mismatch	The amount of memory on the motherboard is different than the amount in CMOS RAM. Run WINBIOS Setup or AMIBIOS Setup.

Error Message	Information
CMOS Time and Date Not Set	Run Standard Setup to set the date and time in CMOS RAM.
D: Drive Error	Hard disk drive D: does not respond. Run the Hard Disk Utility. Also check the D: hard disk type in Standard Setup to make sure that the hard disk drive type is correct.
D: Drive Failure	Hard disk drive D: does not respond. Replace the hard disk.
Diskette Boot Failure	The boot disk in floppy drive A: is corrupt. It cannot be used to boot the computer. Use another boot disk and follow the screen instructions.
Display Switch Not Proper	Some computers require a video switch on the motherboard be set to either color or monochrome. Turn the computer off, set the switch, then power on.
DMA Error	Error in the DMA controller.
DMA #1 Error	Error in the first DMA channel.
DMA #2 Error	Error in the second DMA channel.
FDD Controller Failure	The BIOS cannot communicate with the floppy disk drive controller. Check all appropriate connections after the computer is powered down.
HDD Controller Failure	The BIOS cannot communicate with the hard disk drive controller. Check all appropriate connections after the computer is powered down.
INTR #1 Error	Interrupt channel 1 failed POST.
INTR #2 Error	Interrupt channel 2 failed POST.

Error Message	Information
Invalid Boot Diskette	The BIOS can read the disk in floppy drive A:, but cannot boot the computer. Use another boot disk.
Keyboard Is Locked... Unlock It	The keyboard lock on the computer is engaged. The computer must be unlocked to continue.
Keyboard Error	There is a timing problem with the keyboard. Set the *Keyboard* options in Standard Setup to *Not Installed* to skip the keyboard post routines.
KB/Interface Error	There is an error in the keyboard connector.
No ROM BASIC	Cannot find a bootable sector on either disk drive A: or hard disk drive C:. The BIOS calls INT 18h which generates this message. Use a bootable disk.
Off Board Parity Error	Parity error in memory installed in an expansion slot. The format is: OFF BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
On Board Parity Error	Parity error in motherboard memory. The format is: ON BOARD PARITY ERROR ADDR (HEX) = (XXXX) XXXX is the hex address where the error occurred. Run AMIDiag to find and correct memory problems.
Parity Error????	Parity error in system memory at an unknown address. Run AMIDiag to find and correct memory problems.

Appendix B

AMI BIOS POST Diagnostic Error Messages

This section describes the power-on self-test's (POST) port 80 codes for the AMI BIOS.

Check Point	Description
00	Code copying to specific areas is done. Passing control to INT 19h boot loader next.
03	NMI is Disabled. Next, checking for a soft reset or a power-on condition.
05	The BIOS stack has been built. Next, disabling cache memory.
06	Uncompressing the post code unit next.
07	Next, initializing the CPU init and the CPU data area.
08	The CMOS checksum calculation is done next.
0B	Next, performing any required initialization before the keyboard BAT command is issued.
0C	The keyboard controller I/B is free. Next, issuing the BAT command to the keyboard controller.
0E	The keyboard controller BAT command result has been verified. Next, performing any necessary initialization after the keyboard controller BAT command test.
0F	The initialization after the keyboard controller BAT command test is done. The keyboard command byte is written next.

Check Point	Description
10	The keyboard controller command byte is written. Next, issuing the pin 23 and 24 blocking and unblocking commands.
11	Next, checking if the <End or <Ins> keys were pressed during power on. Initializing CMOS RAM if the Initialize CMOS RAM in every boot AMIBIOS POST option was set in AMIBCP or if the <End> key was pressed.
12	Next, disabling DMA controllers 1 and 2 and interrupt controllers 1 and 2.
13	The video display has been disabled. Port B has been initialized. Next, initializing the chipset.
14	The 8254 timer test will begin next.
19	The 8254 timer test is over. Starting the memory refresh test next.
1A	The memory refresh test line is toggling. Checking the 15 second on/off time next.
23	Reading the 8042 input port and disabling the MEGAKEY Green PC feature next. Making the BIOS code segment writable and performing any necessary configuration before initializing the interrupt vectors.
24	The configuration required before the interrupt vector initialization has been completed. Interrupt vector initialization is done. Clearing the password if the POST DIAG switch is on.
25	Interrupt vector initialization is done. Clearing the password if the POST DIAG Switch is on.
27	Any initialization before setting the video mode will be done next.

Check Point	Description
28	Initialization before setting the video mode is complete. Configuring the monochrome mode and color mode settings next.
2A	Bus initialization system, static, and output devices will be done next, if present.
2B	Passing control to the video ROM to perform any required configuration before the video ROM test.
2C	All necessary processing before passing control to the video ROM is done. Looking for the video ROM next and passing control to it.
2D	The video ROM has returned control to BIOS POST. Performing any required processing after the video ROM had control.
2E	Completed post-video ROM test processing. If the EGA/VGA controller is not found, performing the display memory read/write test next.
2F	The EGA/VGA controller was not found. The display memory read/write test is about to begin.
30	The display memory read/write test passed. Look for retrace checking next.
31	The display memory read/write test or retrace checking failed. Performing the alternate display memory read/write test next.
32	The alternate display memory read/write test passed. Looking for alternate display retrace checking next.
34	Video display checking is over. Setting the display mode next.
37	The display mode is set. Displaying the power on message next.

Check Point	Description
38	Initializing the bus input, IPL and general devices next, if present.
39	Displaying bus initialization error messages.
3A	The new cursor position has been read and saved. Displaying the Hit <DEL> message next.
40	Preparing the descriptor tables next.
42	The descriptor tables are prepared. Entering protected mode for the memory test next.
43	Entered protected mode. Enabling interrupts for diagnostics mode next.
44	Interrupts enabled if the diagnostics switch is on. Initializing data to check memory wraparound at 0:0 next.
45	Data initialized. Checking for memory wraparound at 0:0 and finding the total system memory size next.
46	The memory wraparound test has completed. The memory size calculation has been completed. Writing patterns to test memory next.
47	The memory pattern has been written to extended memory. Writing patterns to the base 640 KB memory next.
48	Patterns written in base memory. Determining the amount of memory below 1 MB next.
49	The amount of memory below 1 MB has been found and verified. Determining the amount of memory above 1 MB next.
4B	The amount of memory above 1 MB has been found and verified. Checking for a soft reset and clearing the memory below 1 MB for the soft reset next. If this is a power on situation, going to checkpoint 4Eh next.

Check Point	Description
4C	The memory below 1 MB has been cleared via a soft reset. Clearing the memory above 1 MB next.
4D	The memory above 1 MB has been cleared via a soft reset. Saving the memory size next. Going to checkpoint 52h next.
4E	The memory test started, but not as the result of a soft reset. Displaying the first 64 KB memory size next.
4F	The memory size display has started. The display is updated during the memory test. Performing the sequential and random memory test next.
50	The memory below 1 MB has been tested and initialized. Adjusting the displayed memory size for relocation and shadowing next.
51	The memory size display was adjusted for relocation and shadowing. Testing the memory above 1 MB next.
52	The memory above 1 MB has been tested and initialized. Saving the memory size information next.
53	The memory size information and the CPU registers are saved. Entering real mode next.
54	Shutdown was successful. The CPU is in real mode. Disabling the Gate A20 line, parity, and the NMI next.
57	The A20 address line, parity and the NMI are disabled. Adjusting the memory size depending on relocation and shadowing next.
58	The memory size was adjusted for relocation and shadowing. Clearing the Hit <DEL> message next.
59	The Hit <DEL> message is cleared. The <WAIT> message is displayed. Starting the DMA and interrupt controller test next.

Check Point	Description
60	The DMA page register test passed. Performing the DMA Controller 1 base register test next.
62	The DMA Controller 1 base register test passed. Performing the DMA Controller 2 base register test next.
65	The DMA Controller 2 base register test passed. Programming DMA Controllers 1 and 2 next.
66	Completed programming DMA Controllers 1 and 2. Initializing the 8259 interrupt controller next.
7F	Extended NMI source enabling is in progress.
80	The keyboard test has started. Clearing the output buffer and checking for stuck keys. Issuing the keyboard reset command next.
81	A keyboard reset error or stuck key was found. Issuing the keyboard controller interface test command next.
82	The keyboard controller interface test completed. Writing the command byte and initializing the circular buffer next.
83	The command byte was written and global data initialization has been completed. Checking for a locked key next.
84	Locked key checking is over. Checking for a memory size mismatch with CMOS RAM data next.
85	The memory size check is done. Displaying a soft error and checking for a password or bypassing WINBIOS Setup next.
86	The password was checked. Performing any required programming before WINBIOS Setup next.

Check Point	Description
87	The programming before WINBIOS Setup has been completed. Uncompressing the WINBIOS Setup code and executing the AMIBIOS Setup or WINBIOS Setup utility next.
88	Returned from WINBIOS Setup and cleared the screen. Performing any necessary programming after WINBIOS Setup next.
89	The programming after WINBIOS Setup has been completed. Displaying the power-on screen message next.
8B	The first screen message has been displayed. The <WAIT...> message is displayed. Performing the PS/2 mouse check and extended BIOS data area allocation check next.
8C	Programming the WINBIOS Setup options next.
8D	The WINBIOS Setup options are programmed. Resetting the hard disk controller next.
8F	The hard disk controller has been reset. Configuring the floppy drive controller next.
91	The floppy drive controller has been configured. Configuring the hard disk drive controller next.
95	Initializing the bus option ROMs from C800 next.
96	Initializing before passing control to the adaptor ROM at C800.
97	Initialization before the C800 adaptor ROM gains control has been completed. The adaptor ROM check is next.
98	The adaptor ROM had control and has now returned control to BIOS POST. Performing any required processing after the option ROM returned control.

Check Point	Description
99	Any initialization required after the option ROM test has been completed. Configuring the timer data area and printer base address next.
9A	Set the timer and printer base addresses. Setting the RS-232 base address next.
9B	Returned after setting the RS-232 base address. Performing any required initialization before the coprocessor test next.
9C	Required initialization before the coprocessor test is over. Initializing the coprocessor next.
9D	Coprocessor initialized. Performing any required initialization after the coprocessor test next.
9E	Initialization after the coprocessor test is complete. Checking the extended keyboard, keyboard ID and Num Lock key next. Issuing the keyboard ID command next.
A2	Displaying any soft errors next.
A3	The soft error display has been completed. Setting the keyboard typematic rate next.
A4	The keyboard typematic rate is set. Programming the memory wait states next.
A5	Memory wait state programming is over. Clearing the screen and enabling parity and the NMI next.
A7	NMI and parity enabled. Performing any initialization required before passing control to the adaptor ROM at E000 next.
A8	Initialization before passing control to the adaptor ROM at E000h has been completed. Passing control to the adaptor ROM at E000h next.

Check Point	Description
A9	Returned from adaptor ROM at E000h control. Next, performing any initialization required after the E000 option ROM had control.
AA	Initialization after E000 option ROM control has been completed. Displaying the system configuration next.
AB	Building the multiprocessor table, if necessary. POST next.
B0	The system configuration is displayed.
AC	Uncompressing the DMI data and initializing DMI.
B1	Copying any code to specific areas.
D0h	The NMI is disabled. Power on delay is starting. Next, the initialization cade checksum will be verified.
D1h	Initializing the DMA controller. Performing the keyboard controller BAT test. Starting memory refresh and entering the 4 GB flat mode next.
D3h	Starting memory sizing next.
D4h	Returning to real mode. Executing any OEM patches and setting the stack next.
D5h	Passing control to the uncompressed code in shadow RAM at E000:0000h. The initialization code is copied to segment 0 and control will be transferred to segment 0.
D6h	Control is in segment 0. Next, checking if <Ctrl><Home>was pressed and verifying the system BIOS checksum.

If either <Ctrl><Home>was pressed or the system BIOS checksum is bad, the system will next go to checkpoint code E0h. Otherwise, it will go to checkpoint code D7h.