386DX MAIN BOARD
(33/40 MHz)

PT-311

USER'S MANUAL

SECTION 1

INTRODUCTION

1.1 Overview

PT-311 offers a 32-bit programming architecture compatible with the software base of the 386 microprocessor. It is a reliable main board using UMC chipset and multi-layers printed circuit board. The chipset consists of UM82C481 and UM82C482 which provides the most cost effective and high performance solution to 386 computer system.

The UM82C481 and UM8C482 chipes occupy I/O port addresses from 80AC to 80AF hex for special controls such as memory configuration, CPU speed change, shadow RAM for system and video BIOS, and even sleep mode for power management.

A block of 128K memory of the system DRAM is used for system and video shadow RAM to increase the system performance. The video shadow RAM consists of four 16K pages which can be enabled respectively.

To achieve maximum performance and value-added capabilities, it also includes a socket for Weitek 3167 or 80387 numeric co-processor.

1.2 Checklist

Please check your PT-311 package to ensure that it contains the following items :

- PT-311 Main board
- PT-311 User's manual

If any of these items are missed or damaged, please contact your local dealer or sales representative for assistance.

SECTION 2

SPECIFICATION

2.1 PT-311 System Board Specifications

* 100% IBM AT compatible.
* Apply High performance CMOS technology.
* Support up to 32MB memory on board.
* Mix 256K, 1M, and 4M SIMM Module DRAM memory
* Fast CPU reset and Fastgate A20 logic.
* Speed switching with hardware and software selection.
* Board size with 22cm by 22cm.
* Five 16-bit slots and two 8-bit slots.

2.2 Jumpers and Connectors

Jumpers / Connectors	Description
CN1, CN2	Power supply connectors
J1	Ext. battery connector
J2	Turbo LED connector
J3	Turbo switch connector
J4	Reset connector
J5	Speaker connector
J6	Keyborad lock & power LED connector
KB1	Keyboard connector
W1	CMOS power input select
W2	Display adapter select
W4 & W7	80387 co-processor select
W8-W15	Cache select
W16	Parity select

SECTION 2

SPECIFICATION

2.2 Jumpers and Connectors

CN1 : Power Supply Connector

Pin	Assignment
1	Power Good
2	+5V
3	+12V
4	-12V
5	Ground
6	Ground

CN2 :

Pin	Assignment
7	Ground
8	ground
9	-5V
10	+5V
11	+5V
12	+5V

J1 : External Battery Connector

Pin	Assignment
1	External battery Vdc (+6V DC)
2	NC
3	Ground
4	Ground

J2 : Turbo LED connector

Pin	Assignment
1	LED Cathode
2	LED Anode

J3 : Hardware Turbo Switch, Software Cache Switch

Open	Lower speed, (Ctrl)+(Alt)+(-)	Cache off
Short	Turbo Speed, (Ctrl)+(Alt)+(+)	Cache on

J4 : Reset Switch Connector

Open	Normal
Short	Reset

J5 : Speaker Connector

Pin	Assignment
1	Speaker Data
2	NC
3	Ground
4	Vcc +5V

SECTION 2

SPECIFICATION

2.2 Jumpers and Connector

J6 : Keyboard Lock & Power LED Connector
Pin Assignment

1	Vcc +5V
2	NC
3	Ground
4	Keyboard Lock
5	Ground

W1 : CMOS Power Input Select

Open	External Battery Power Input
Short	Main Board Battery Power Input

W2 : Display Type

Open	Mono	
Short	Color	<Default>

W4 & W7 : 80387 Mode

All Short = Enable 80387

W8, W9, W10, W11, W12, W13, W14, W15 Cache Size Select

Cache Size	32KB	64KB	128KB	256KB
W8	1-2	2-3	2-3	2-3
W9	1-2	1-2	2-3	2-3
W10	1-2	1-2	2-3	2-3
W11	1-2	2-3	2-3	2-3
W12	2-3	1-2	2-3	1-2
W13	1-2	1-2	1-2	2-3
W14	1-2	1-2	1-2	2-3
W15	OPEN	OPEN	1-2	2-3

W16 : Parity Select

1-2	Parity Disable	<Default>
2-3	Parity Enable	

SECTION 2

SPECIFICATION

2.3 Memory Configuration Table

Size	Bank 0	Bank 1
1 MB	256 KB SIMM	X
2 MB	256 KB SIMM	256 KB SIMM
4 MB	1 MB SIMM	X
5 MB	256 KB SIMM	1 MB SIMM
8 MB	1 MB SIMM	1 MB SIMM
16 MB	4 MB SIMM	X
17 MB	256 KB SIMM	4 MB SIMM
20 MB	1 MB SIMM	4 MB SIMM
32 MB	4 MB SIMM	4 MB SIMM

X	NOT FILL
Bank 0	SIMM 1 - SIMM 4
Bank 1	SIMM 5 - SIMM 8

2.4 Cache RAM Table

PT-311 80386 system board supports 32KB/64KB/128KB/256K Cache size.
For 32KB/128KB, only the first bank of Cache RAM is required (U17 - U20).

Size	Only the 1st bank installed
32KB	8Kx8 SRAM
128KB	32Kx8 SRAM

Size	Both bank installed
64KB	8Kx8 SRAM
256KB	32Kx8 SRAM

Note : Bank 0 (U17-U20), Bank 1 (U25-U28), Cache TAG (U21)
* 33Mhz system ,SRAM speed should be 25ns and TAG RAM 20ns.
* 40Mhz system ,SRAM speed should be 20ns and TAG RAM 15ns.

Refer to the Section 2 Jumper Configuration for jumper settings with different Cache sizes.

2.5 Installation of Co-processor

There is a 121-pin PGA socker U24 for 80387 DX or WEITEK 3167 Co-processor. Make sure the jumpers set up are correct when the Co-processor is installed.

* If any question is found, please contact your local dealer for assistance.

SECTION 3

INPUT / OUTPUT CHANNEL SLOTS

The input/output channel of PT-311 supports :

* Refresh of system memory from channel microprocessors
* Selection of data accesses (either 8-bit or 16-bit)
* Interrupt
* DMA channels
* I/O wait-state generation
* Open-bus structure (allowing multiple microprocessors to share the system's resources including memory)

3.1 I/O Address Map

Hex Range	Devices	Usage
000-01F	DMA Controller 1	System
020-03F	Interrupt Controller 1	System
040-05F	Timer	System
060-06F	8042 (Keyboard)	System
070-07F	Real Time Clock, NMI Mask	System
080-09F	DMA Page Register	System
0A0-0BF	Interrupt Controller 2	System
0C0-0DF	DMA Controller 2	System
0F0	Clear Math Co-processor Busy	System
0F1	Reset Math Co-porcessor	System
0F8-0FF	Math Co-processor	System
1F0-1F8	Fixed Disk	I/O
200-207	Game I/O	I/O
278-27F	Parallel Printer Port 2	I/O
2F8-2FF	Serial Port 2	I/O
300-31F	Prototype Card	I/O
360-36F	Reserved	I/O
378-37F	Parallel Printer Port 1	I/O
380-38F	SDLC, Bisynchronous 2	I/O
3A0-3AF	Bisynchronous 1	I/O
3B0-3BF	Monochrome Display and Printer Adapter	I/O
3C0-3CF	Reserved	I/O
3D0-3DF	Color/Graphic Monitor Adapter	I/O
3F0-3F7	Floppy Diskette Controller	I/O
3F8-3FF	Serial Port 1	I/O

3.2 62-Pin, 32-Pin I/O Bus

REAR PANEL

GND	B1	-	-	A1	-I/O CH CK
RESET DRV	B2	-	-	A2	SD7
+5V ED	B3	-	-	A3	SD6
IRQ9	B4	-	-	A4	SD5
-5V DC	B5	-	-	A5	SD4
DRQ2	B6	-	-	A6	SD3
-12VDC	B7	-	-	A7	SD2
DWS	B8	-	-	A8	SD1
+12VDC	B9	-	-	A9	SD0
GND	B10	-	-	A10	-I/O CH RDY
-SMEMW	B11	-	-	A11	AEN
-SMEMR	B12	-	-	A12	SA19
-LOW	B13	-	-	A13	SA18
-LOR	B14	-	-	A14	SA17
-DACK3	B15	-	-	A15	SA16
DRQ3	B16	-	-	A16	SA15
-DACK1	B17	-	-	A17	SA14
DRQ1	B18	-	-	A18	SA13
-REFRESH	B19	-	-	A19	SA12
CLK	B20	-	-	A20	SA11
IRQ7	B21	-	-	A21	SA10
IRQ6	B22	-	-	A22	SA9
IRQ5	B23	-	-	A23	SA8
IRQ4	B24	-	-	A24	SA7
IRQ3	B25	-	-	A25	SA6
-DACK2	B26	-	-	A26	SA5
T/C	B27	-	-	A27	SA4
BALE	B28	-	-	A28	SA3
+5VDC	B29	-	-	A29	SA2
OSC	B30	-	-	A30	SA1
GND	B31	-	-	A31	SA0

-MEM CS16	D1	-	-	C1	SBHE
-I/O CS16	D2	-	-	C2	LA23
IRQ 10	D3	-	-	C3	LA22
IRQ 11	D4	-	-	C4	LA21
IRQ 12	D5	-	-	C5	LA20
IRQ 15	D6	-	-	C6	LA19
IRQ 14	D7	-	-	C7	LA18
-DACK 0	D8	-	-	C8	LA17
DRQ 0	D9	-	-	C9	-MEMR
-DACK 5	D10	-	-	C10	-MEMW
DRQ 5	D11	-	-	C11	SD08
-DACK 6	D12	-	-	C12	SD09
DRQ 6	D13	-	-	C13	SD10
-DACK 7	D14	-	-	C14	SD11
DRQ 7	D15	-	-	C15	SD12
+5V DC	D16	-	-	C16	SD13
-MASTER	D17	-	-	C17	SD14
GND	D18	-	-	C18	SD15

SECTION 4

HARDWARE COMPATIBILITY

4.1 System Timers

The system has three programmable timer/counters controlled by an Intel 8254-2 timer/counter chip. These are channel 0 through 2, defined as follows :

Channel 0	System timer
GATE 0	Tied on
CLK IN 0	1.190Mhz OSC
CLK OUT 0	8259A IRQ 0

Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190Mhz OSC
CLK OUT 1	Request Refresh Cycle

* Note : Channel is programmed to generate a 15 microsecond period signal.

Channel 2	Tone Generation for speaker
GATE 2	Controlled by bit 0 of hex 61 PPI bit
CLK IN 2	1.190Mhz OSC
CLK OUT 2	Used to drive the speaker

4.2 System Interrupts

Sixteen levels of system interrupts are provided by the 80286 NMI & two 8259A interrupt controller chips. The following shows the various interrupt-level assignments in decreasing priority :

Level		Function
Microprocessor NMI		Parity or I/O channel check
Interrupt controllers		
CTLR 1	CTLR 2	
IRQ 0		Timer output 0
IRQ 1		Keyboard (Output buffer full)
IRQ 2		Interrupt from CTLR 2
	IRQ 8	Real time clock interrupt
	IRQ 9	Software redirected to INT 0AH(IRQ 2)
	IRQ 10	Reserved
	IRQ 11	Reserved
	IRQ 12	Reserved
	IRQ 13	Numeric co-processor
	IRQ 14	Fixed disk controller
	IRQ 15	Reserved
IRQ 3		Serial Port 2
IRQ 4		Serial Port 1
IRQ 5		Parallel Port 2
IRQ 6		Diskette controller
IRQ 7		Parallel port 1

4.3 Direct Memory Access

Each DMA channels are supported by the system. Two Intel 8237-5 DMA controller chips (Four channels in each chip) are used. DMA channels are assigned as follows :

CTLR 1	CTLR 2
Ch 0-Spare	Ch 4-Cascade for CTLR 1
Ch 1-SDLC	Ch 5-Spare
Ch 2-Diskette	Ch 6-Spare
Ch 3-Spare	Ch 7-Spare

Channels from 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB block throughout the 16-megabyte system address space.

Channels from 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfer of 16-bit data between 16-bit adapters and 16-bit system memory are then supported by channels 5, 6, & 7. DMA channels from 5 through 7 transfer data in 128K blocks throughout the 16-megabyte system address space.
These channels will not transfer data on odd-byte boundaries.

The address for the page register are as follows :

Page Register	I/O HEX address
DMA channel 0	0087
DMA channel 1	0083
DMA channel 2	0081
DMA channel 3	0082
DMA channel 5	008B
DMA channel 6	0089
DMA channel 7	008A
Refresh	008F

Address generation for the DMA channels is as follows :

For DMA channels 3 through 0 :

Source	DMA Page Registers 8237A-5	
Address	A23.....A16	A15.....A1

For DMA channels 7 through 5 :

Source	DMA Page Registers 8237A-5	
Address	A23.....A17	A16.....A0

Note : The BHE and A0 addressing signals are forced to a logic 0. DMA channel addressees do not increase or decrease through page boundaries (64KB for channels 0 through 3 and 128 KB for channels 5 through 7).

SECTION 4

HARDWARE COMPATIBILITY

4.4 Real Time Clock and Non-Volatile RAM

The real time clock and its 64 bytes of RAM information are backed up by 3.6V rechargeable DC battery (or 6V external battery). The internal clock circuitry uses 14 bytes while the rest is allocated to system configuration.

Real time clock address :

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic Status byte
0F	Shutdown
10	Diskette drive type byte-drive A and B
11	Reserved
12	Fixed disk type byte-drive C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte
19	Extended fixed disk type-driver C
1A	Extended fixed disk type-driver D
1B-2D	Reserved
2E-2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34-3F	Reserved