

# 386SX MAIN BOARD ( 25 MHz )

PT-308

## USER'S MANUAL

BEFORE INSTALLING THIS 386SX MAIN BOARD PLEASE READ  
THIS MANUAL COMPLETELY AND RETAIN IT FOR FUTURE REFERENCE

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- Note:**
1. For the first time installation with error message on the screen, please leave the system on for about 30-60 minutes to recharge the battery, then you can enter the system configuration.
  2. Leave your system on for about 24 hours to recharge the battery fully.
  3. If you have switched off the computer system for more than one week, you might be required to repeat step 2 to recharge the battery fully.

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- \* LIM EMS 4.0 is registered trademark of Lotus Development Corp., Intel Corp., and Microsoft Corp.

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SECTION 1

INTRODUCTION

1.1 Overview

PT-308 is a fully 386 SX compatible system board implemented with highly integrated VLSI single chip 82C311 (SCAMP) which support 16 MB on-board memory, system shadow RAM and Video shadow RAM either 8-bit or 16-bit Bios and 386 SX CPU at clock speed up to 25 MHz (Landmark 32.x Mhz)

PT-308 system board support MS-DOS, PC-DOS version 2.0 or above, XENIX, NOVELL Netware and all 386SX application Programs.

1.2 Checklist

Please check your PT-308 package to ensure that it contains the following items :

- PT-308 Main board
- PT-308 User's manual

If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

## SECTION 2

### SPECIFICATIONS

#### 2.1 System Board Specifications

- . Intel 80386x Microprocessor.
- . Socket for Optional 80387sx Coprocessor.
- . Page and Page Interleaved on board memory.
- . Up to 16MB of Memory on board by 4MB x 9, 1MB x 9 and 256KB x 9 SIMM Modules.
- . Up to 25MHz with 0 wait state memory access.
- . LIM EMS 4.0 compatibles.
- . Fast Gate A20 and Fast CPU Reset logic.
- . Speed switching with hardware and software selection.
- . Single-chip solution and low power consumption.
- . Programmable Shadow RAM Capability.
- . Optimized for OS/2 operation.
- . Rechargeable Battery Back-Up on Board.
- . Fully IBM PC/AT Compatible Bus Architecture 6 slots x 16-bit and 1 slots x 8 bit Bus.
- . Board size 22cm x 22cm.
- . 4-layers board to avoid the noise-rising.

#### 2.2 Jumpers and Connectors Descriptions

JP1	Pipeline Selector
J5	Speaker Connector
JP6	COMS SETUP Selector
J8	External Batt Connector
J9	Keyboard Connector
J10	Key-lock and Power-LED
JP11	Display Selector
J15	Reset Connector for Restart the system
JP9D	Parity Check Connector
TUR-SW	Turbo-Switch for Hi-Speed
TUR-LED	LED Connector for Speed-status
POW	Power Connector

#### 2.2 Jumpers and Connectors Descriptions

##### PIPELINE MODE (JP1)

PIN	DESCRIPTION
1-2 ON	Pipeline mode
1-2 OFF	Non Pipeline mode

##### SPEAKER CONNECTOR (J5)

PIN	DESCRIPTION
1	DATA OUT
2	Key
3	Ground
4	+ 5VDC

##### COMS SETUP SELECTOR (JP6)

PIN	DESCRIPTION
1-3 ON	Reset COMS Setup (Short once)
2-4 ON	Normally use

##### EXTERNAL BATTERY CONNECTOR (J8)

PIN	DESCRIPTION
1	3.6V/6V DC
2	Not Used
3	Ground
4	Ground

##### KEYBOARD CONNECTOR (J9)

PIN	DESCRIPTION
1	Keyboard Clock
2	Keyboard DATA
3	Spare
4	Ground
5	+5VDC



2.2 Jumpers and Connectors Descriptions

POWER LED and KEYLOCK CONNECTOR (J10)

PIN	DESCRIPTION
1	LED power
2	Key
3	Ground
4	Keyboard Inhibitor
5	Ground

DISPLAY SELECTOR (JP11)

PIN	DESCRIPTION
1-2 ON	Color Graphic display
1-2 OFF	Monochrome display

HARDWARE RESET (J15)

This jumper is to restart the system when you short the header once.

PARITY CHECK CONNECTOR (JP90)

PIN	DESCRIPTION
1-2 ON	Enable
1-2 OFF	Disable

2.2 Jumpers and Connectors Descriptions

TURBO SWITCH (TUR-SW)

PIN	DESCRIPTION
1-2 ON	HIGH-SPEED
1-2 OFF	LOW-SPEED

NOTE: You can also make the selection of Fast or Low Speed by pressing <CTRL>, <ALT> and <+> or <-> at the TUR-SW-OFF environment.

TURBO LED (TUR-LED)

This header is for the LED connector of cabinet and Speed Status. It will make LED Bright at Hi-Speed and Dark at Lo-speed.

POWER CONNECTOR (P0W)

PIN	DESCRIPTION
1	Power Good
2	+ 5V DC
3	+ 12V DC
4	- 12V DC
5	Ground
6	Ground
7	Ground
8	Ground
9	- 5V DC
10	+ 5V DC
11	+ 5V DC
12	+ 5V DC



### 2.3 MEMORY CONFIGURATIONS

#### DRAMS Configuration

BANK 0	BANK 1	BANK 2	BANK 3	TOTAL
256K	X	X	X	512KB
256K	256K	X	X	1MB
256K	256K	256K	X	1.5MB
256K	256K	256K	256K	2MB
1M	X	X	X	2MB
1M	1M	X	X	4MB
1M	1M	1M	X	5MB
1M	1M	1M	1M	8MB
4M	X	X	X	8MB
4M	4M	X	X	16MB
256K	256K	1M	X	3MB
256K	256K	1M	1M	5MB
1M	1M	4M	X	12MB

### 2.4 BIOS CONFIGURATION

#### 2.4.1 How to pop-up the Set-Up Menu

After your installation of the system and you need to make proper setting in the Set-Up menu. When the system is powered on or reset, the BIOS will display the logo of System BIOS and begin to run POST (Power On Self Test) and initialize and check the other interface cards those are match or not the Set-Up Menu. If the setting inside the Set-Up Menu is not the same Real interface Cards the BIOS will show the ERROR MESSAGE AND <F1> will be prompted.

Pressing the <F1> key is to enter the Set-Up menu for corrections of the current configurations.

In addition, you can also enter the Set-Up menu by press <DEL> key once before memory test completed.

### 2.4.2 Manufacturing Default BIOS Setting Table

The following Menu Table are for AMI CMOS SETUP settings and the Manufacturing default settings.

BIOS SETUP PROGRAM - ADVANCED CMOS SETUP (C) 1990 American Megatrends Inc., All Rights Reserved	
Typematic Rate Programming	: Disabled
Typematic Rate Delay (msec)	: 250
Typematic Rate (Chars/Sec)	: 30
Above 1 MB Memory Test	: Disabled
Memory Test Tick Sound	: Enabled
Memory Parity Error Check	: Enabled
Hit<DEL> Message Display	: Enabled
Hard Disk Type 47 RAM Area	: 0:300
Wait For <F1> If Any Error	: Enabled
Adaptor ROM Shadow C800, 16K	: Disabled
Adaptor ROM Shadow C000, 16K	: Disabled
Adaptor ROM Shadow D000, 16K	: Disabled
Adaptor ROM Shadow D400, 16K	: Disabled
Adaptor ROM Shadow D800, 16K	: Disabled
Adaptor ROM Shadow DC00, 16K	: Disabled
Adaptor ROM Shadow E000, 32K	: Disabled
Adaptor ROM Shadow E800, 32K	: Disabled
System ROM Shadow F000, 64K	: Disabled
DRAM Wait States	: 0 W/S
Global EMS Control	: Disabled
Turbo Video	: Enabled
Non-Turbo Mode CLK2 Divider	: CLK 2/2
Fast Clock Divider	: /2
Ext BUS Oscillator Control	: Fast
Slot Clock Divider	: /4

## 2.4 BIOS CONFIGURATION

### 2.4.3 How to configure the Set-Up MENU for AMI BIOS

After your installation of the system and you need to make proper setting in the Set-Up Menu.

When the system is powered on or reset, the BIOS will display the logo of system BIOS and begin to run POST (Power On Self Test) and initialize and check the other interlace cards those are match or not in the Set-Up Menu.

If the setting are not the same as the real interface cards, the BIOS will show the error messages what is not match with the settings and <F1> will prompt at the end-line.

In addition, you can also display the Set-Up Menu By pressing <DEL> key.

#### 1. STANDARD CMOS SETUP

In the Standard Setup Options Table, you can set the TIME, DATE, Floppy Disk Driver, Fixed Disk and Display Selections.

##### Diskette Drive(s) Selection

- . 5.25 Inch, 360KB
- . 5.25 Inch, 1.2MB
- . 3.5 Inch, 720KB
- . 3.5 Inch, 1.44MB

#### ADVANCED FEATURE CONTROL

##### Numlock

In the Advanced Feature Control Menu, you can set the Numlock Key ON or OFF when booting the system.

##### CPU Speed

In this entry, you can set the CPU Speed Fast or Slow when booting the system.

##### DRAMs Wait States

In this entry, you can configure the Memory Access Wait States "0" and "1" to meet the DRAM Speed. 0 Wait States needs the DRAM at 80ns.

##### Shadow System and Video BIOS

In this entry, you can set Enable if the system has 1 Megabyte memory size at least. Enabling the System and Video Shadow is that it read the contents of BIOS from Read Only Memory (ROM) and write and locate in the DRAM so that the system becomes faster because the DRAM Memory Access is more rapidly the ROM.

### 2.4.3 How to configure the set-up MENU for AMI BIOS

#### ADVANCED FEATURE CONTROL

##### Non - Turbo Mode CLK Divider

This supports the AT Bus performance control - Divided by two in faster than divided by four.

##### Turbo Video

This formative is to enhance the Video Graphics performance.

SECTION 3 I/O CHANNEL AND DIAGRAM

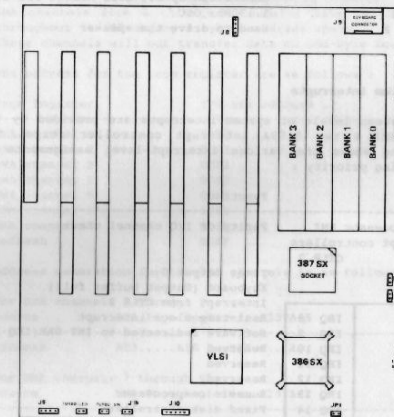
3.1 62 Pin I/O Bus

GND	B1	-	-	A1	-I/O CH CK
RESET DRV	B2	-	-	A2	SD7
+5V ED	B3	-	-	A3	SD6
IRQ9	B4	-	-	A4	SD5
-5V DC	B5	-	-	A5	SD4
DRQ2	B6	-	-	A6	SD3
-12VDC	B7	-	-	A7	SD2
DWS	B8	-	-	A8	SD1
+12VDC	B9	-	-	A9	SD0
GND	B10	-	-	A10	-I/O CH RDY
-SMEHW	B11	-	-	A11	AEN
-SHEMR	B12	-	-	A12	SA19
-LOW	B13	-	-	A13	SA18
-LOR	B14	-	-	A14	SA17
-DACK3	B15	-	-	A15	SA16
DRQ3	B16	-	-	A16	SA15
-DACK1	B17	-	-	A17	SA14
DRQ1	B18	-	-	A18	SA13
-REFRSSH	B19	-	-	A19	SA12
CLK	B20	-	-	A20	SA11
IRQ7	B21	-	-	A21	SA10
IRQ6	B22	-	-	A22	SA9
IRQ5	B23	-	-	A23	SA8
IRQ4	B24	-	-	A24	SA7
IRQ3	B25	-	-	A25	SA6
-DACK2	B26	-	-	A26	SA5
I/C	B27	-	-	A27	SA4
BALE	B28	-	-	A28	SA3
+5VDC	B29	-	-	A29	SA2
OSC	B30	-	-	A30	SA1
GND	B31	-	-	A31	SA0

3.2 36 Pin I/O Bus

-MEM CS16	D1	-	-	C1	SBHE
-I/O CS16	D2	-	-	C2	LA23
IRQ 10	D3	-	-	C3	LA22
IRQ 11	D4	-	-	C4	LA21
IRQ 12	D5	-	-	C5	LA20
IRQ 15	D6	-	-	C6	LA19
IRQ 14	D7	-	-	C7	LA18
-DACK 0	D8	-	-	C8	LA17
DRQ 0	D9	-	-	C9	-MEMR
-DACK 5	D10	-	-	C10	-MEMW
DRQ 5	D11	-	-	C11	SD08
-DACK 6	D12	-	-	C12	SD09
DRQ 6	D13	-	-	C13	SD10
-DACK 7	D14	-	-	C14	SD11
DRQ 7	D15	-	-	C15	SD12
+5V DC	D16	-	-	C16	SD13
-MASTER	D17	-	-	C17	SD14
GND	D18	-	-	C18	SD15

3.3 Board Outline





## SECTION 4

## HARDWARE COMPATIBILITY

## 4.1 System timers

The system has three programmable timer/counters controlled by an Intel 8254-2 timer/counter chip. These are channel 0 through 2, defined as follows :

Channel 0	System timer
GATE 0	Tied on
CLK IN 0	1.190Mhz OSC
CLK OUT 0	8259A IRQ 0
Channel 1	Refresh Request Generator
GATE 1	Tied on
CLK IN 1	1.190Mhz OSC
CLK OUT 1	Request Refresh Cycle
* Note : Channel is programmed to generate a 15 microsecond period signal.	
Channel 2	Tone Generation for speaker
GATE 2	Controlled by bit 0 of hex 61 PPI bit
CLK IN 2	1.190Mhz OSC
CLK OUT 2	Used to drive the speaker

## 4.2 System interrupts

Sixteen levels of system interrupts are provided by the 80286 NMI & two 8259A interrupt controller chips. The following shows the various interrupt-level assignments in decreasing priority :

Level	Function
Microprocessor NMI	Parity or I/O channel check
Interrupt controllers	
CTLR 1	CTLR 2
IRQ 0	Timer output 0
IRQ 1	Keyboard (Output buffer full)
IRQ 2	Interrupt from CTLR 2
	IRQ 8 Real time clock interrupt
	IRQ 9 Software redirected to INT 0AH(IRQ 2)
	IRQ 10 Reserved
	IRQ 11 Reserved
	IRQ 12 Reserved
	IRQ 13 Numeric co-processor
	IRQ 14 Fixed disk controller
	IRQ 15 Reserved
IRQ 3	Serial Port 2
IRQ 4	Serial Port 1
IRQ 5	Parallel Port 2
IRQ 6	Diskette controller
IRQ 7	Parallel port 1

## SECTION 4

## HARDWARE COMPATIBILITY

## 4.3 Direct memory access

Each DMA channels are supported by the system. Two Intel 8237-5 DMA controller chips (Four channels in each chip) are used. DMA channels are assigned as follows :

CTLR 1	CTLR 2
Ch 0-Spare	Ch 4-Cascade for CTLR 1
Ch 1-SDLC	Ch 5-Spare
Ch 2-Diskette	Ch 6-Spare
Ch 3-Spare	Ch 7-Spare

Channels from 0 through 3 are contained in DMA controller 1. Transfers of 8-bit data, 8-bit I/O adapters and 8-bit or 16-bit system memory are supported by these channels. Each of these channels will transfer data in 64KB block throughout the 16-megabyte system address space.

Channels from 4 through 7 are contained in DMA controller 2. To cascade channels 0 through 3 to the microprocessor, use channel 4. Transfer of 16-bit data between 16-bit adapters and 16-bit system memory are then supported by channels 5, 6 & 7. DMA channels from 5 through 7 transfer data in 128K blocks throughout the 16-megabyte system address space. These channels will not transfer data on odd-byte boundaries.

The address for the page register are as follows :

Page Register	I/O HEX address
DMA channel 0	C087
DMA channel 1	C083
DMA channel 2	C081
DMA channel 3	C082
DMA channel 5	C08B
DMA channel 6	C089
DMA channel 7	C08A
Refresh	C08F

Address generation for the DMA channels is as follows :

For DMA channels 3 through 0 :		
Source	DMA Page Registers 8237A-5	
Address	A23.....A16	A15.....A1
For DMA channels 7 through 5 :		
Source	DMA Page Registers 8237A-5	
Address	A23.....A17	A16.....A0

Note : The BHE and A0 addressing signals are forced to a logic 0. DMA channel addresses do not increase or decrease through page boundaries(64KB for channels 0 through 3 and 128KB for channels 5 through 7).

## SECTION 4

## HARDWARE COMPATIBILITY

## 4.4 Real time clock and non-volatile RAM

The real time clock and its 64 bytes of RAM information are backed up by 3.6V rechargeable DC battery (or 6V external battery). The internal clock circuitry uses 14 bytes while the rest is allocated to system configuration.

Real time clock address :

Address	Description
00	Seconds
01	Second alarm
02	Minutes
03	Minute alarm
04	Hours
05	Hour alarm
06	Day of week
07	Date of month
08	Month
09	Year
0A	Status register A
0B	Status register B
0C	Status register C
0D	Status register D
0E	Diagnostic Status byte
0F	Shutdown
10	Diskette drive type byte-drive A and B
11	Reserved
12	Fixed disk type byte-drive C and D
13	Reserved
14	Equipment byte
15	Low base memory
16	High base memory
17	Low expansion memory byte
18	High expansion memory byte
19	Extended fixed disk type-driver C
1A	Extended fixed disk type-driver D
1B-2D	Reserved
2E-2F	2 byte CMOS checksum
30	Low expansion memory byte
31	High expansion memory byte
32	Data century byte
33	Information flags (set during power on)
34-3F	Reserved