



Megaplex Server Chassis Guide

Preliminary DRAFT

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Revision History

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Preface

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The BBS requires no parity, eight data bits, and one stop bit. The BBS phone numbers is 770-246-8780.

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<http://www.ami.com>.

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Preface, Continued

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The following text describes the WARNINGS, CAUTIONS, and NOTES used throughout this document. Each description is followed by an example. You should become familiar with these procedures and always observe standard safety practices.

Warning Used to describe potential hazards to personnel. Follow directions carefully to avoid injury.

Warning

High voltage used in this equipment. To avoid injury or electrical shock, do not remove cover or reach into the unit when the power cord is connected.

Caution Used to describe hazards to equipment. Failure to comply with instruction may result in damage to the equipment.

Caution

Support the drive canister with both hands when removing it from the chassis. Failure to support the canister can result in the unit falling and striking the chassis causing damage to the canister or to the chassis.

Note: Provides information that will aid you in the interpretation of systems operations, procedures, or functions.

Note: Do not duplicate ID numbers within the same SCSI bus.

1 General Information

Introduction

This manual provides general installation and maintenance information, including drive installation and power supply replacement for the Megaplex Server Chassis. The material is arranged into the following sections.

Section 1 - General Information

This section provides a general description of the chassis. Specifications are included.

Section 2 – Installation

This section describes the procedures for installing drives into the Megaplex Server Chassis and for installing the chassis into a standard rack.

Section 3 - Field Replaceable Units

This section describes the replacement of Drives, Fans, and Power Supplies.

Section 4 - Display Panel

This section describes use, operation and programming of the display panel.

General Description of Chassis

The Megaplex rack-mount chassis supports up to twelve 3.50" SCA (Single Connector Attachment) Low Voltage Differential (LVD) 16-bit SCSI drives. SCA drives provide simple installation via pluggable canisters. The no cable design of SCA allows you to simply mount the drive into the canister and plug into the chassis.

System peripherals include mountings for:

- one 5.25" full-height DLT tape drive,
 - one 5.25" half-high CD-ROM drive,
 - one 3.5" floppy drive, and
 - one 3.5" DE (system drive).
-

Power Supplies The chassis is supported by three 600-watt hot-pluggable power supplies. The N+1 redundant arrangement allows the chassis to continue operation should one of the power supplies fail. The power supply is a modular, pluggable design, which is inserted into the rear of the chassis. Each power supply plugs into the chassis power distribution board via a blind mate connector. The power supplies are hot-pluggable units that can be removed and replaced while the system remains operational.

Cooling Cooling is front to rear. Five separate removable, modular fan assemblies are provided in the front of the chassis. Six blower-type fans (two per power supply assembly) exhaust the air from the rear of the chassis.

An LCD display board is in the front of the unit. The display panel is an intelligent data gathering and control module that monitors and reports environmental conditions in the enclosure. Items monitored include:

- power status from various power supplies,
 - module presence,
 - navigation switch,
 - and drive fault LED status.
-

Front of Chassis



Specifications

Installation:	Rack-Mount.
Dimensions:	17.00" W x 26.00" D x 26.25" H
Weight:	Approximately 200 lb.
Controller I/O:	Fourteen expansion slots, rear of chassis.
Power Supply:	Three hot pluggable 600-Watt power supply assemblies.
Each P/S Assembly:	
AC Input:	90 - 132 VAC @ 60 Hz (nominal 110 VAC) (Auto Switch), 14.0 Amps 180 - 265 VAC @ 50 Hz (nominal 220 VAC) (Auto Switch), 8.0 Amps
DC Output:	+5 VDC @ 60 Amps. +12 VDC @ 24 Amps. -5 VDC @ .6 Amps. -12 VDC @ .12 Amps.
Drives Supported:	Up to twelve 3.5" 16-bit single ended SCA drives, one 5.25" full-height DLT tape drive, one 5.25" half-height CD-ROM drive, one 3.5" floppy drive, one 3.5" IDE system drive.
Switches/LEDs:	IDE activity LED, power on LED, power on/off switch, reset switch, parameters buttons..up, down, enter, exit.
Cooling:	Five fan module assemblies provided in front of chassis. Six blower fans mounted inside the power supply assemblies.
Temperature:	Operating: 0°C to 40°C. Storage: -20°C to 75°C.
Humidity:	0% to 95% non-condensing.
Altitude	Operating: 0 feet to 10,000 feet. Storage: 0 feet to 40,000 feet.

2 Installation

Unpacking and Inspection

Unpack the Megaplex chassis and visually inspect it for damage that might have occurred during shipment. Retain the shipping carton in case reshipment is necessary.

Remove the top cover of the chassis and inspect for component damage. If any damage has occurred, notify American Megatrends immediately. See page ii of this manual for details.

Each shipping carton should contain the following:

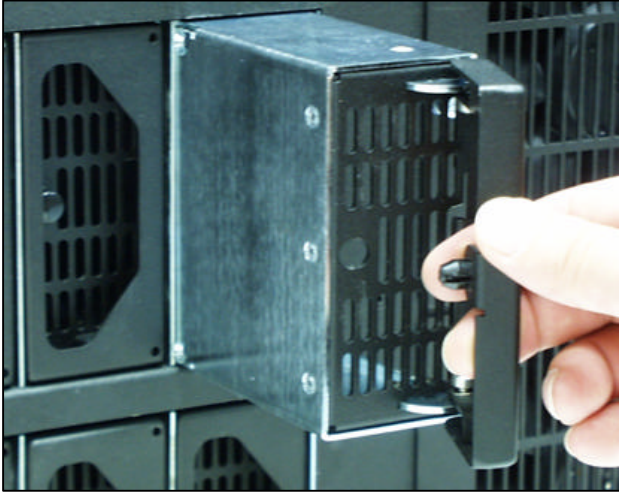
- a Megaplex server chassis,
 - 12 drive canisters,
 - this manual,
 - three power cords,
 - slides,
 - castors, and
 - mounting hardware
-

Drive Installation

Before installing drives make sure that the chassis is powered down.

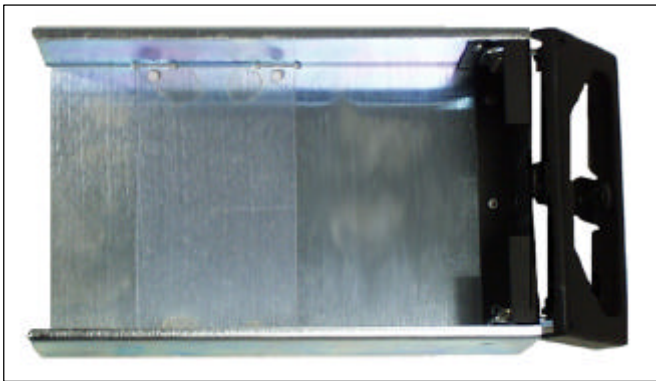
Step 1

Remove the module from the chassis. Pull the handle outward to release the cam action latch.



Step 2

A bag of hardware is inside each drive module. Use the four screws to secure the drive inside the module. The mountings are on the bottom of the module.



Rack-Mount Installation

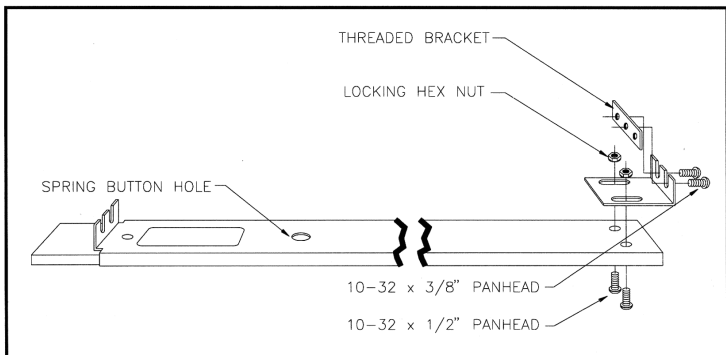
Before the unit is installed into a rack the following items should be taken into consideration:

- The maximum ambient temperature of this unit is 40°C. Internal temperatures of the rack assembly should be considered for safe operation.
 - Do not block power supply vents or otherwise restrict airflow when installing the unit into the rack.
 - Mechanical loading of the rack should be considered so that the rack remains stable and unlikely to tip.
 - Consideration to the overall loading of the branch circuit should be given before installing any equipment in a rack environment.
-

Installation Steps Use the following procedure to install the Megaplex chassis into a standard 19" RETMA rack and apply the AC input power.

Step 1 Remove the slides from the chassis by sliding the slides out until the rear retaining spring buttons engage. Depress the buttons and slip the slides completely free from the chassis. Set the chassis aside.

Step 2 Remove the small claw brackets from the package and loosely fasten them, with the teeth facing out, to the front and rear of the outer slides using 10-32 x 1/2" screws. Notice that the bracket has slotted holes for adjustment. Use the locking hex nuts provided to secure the screws.



Cont'd

Rack-Mount Installation, Continued

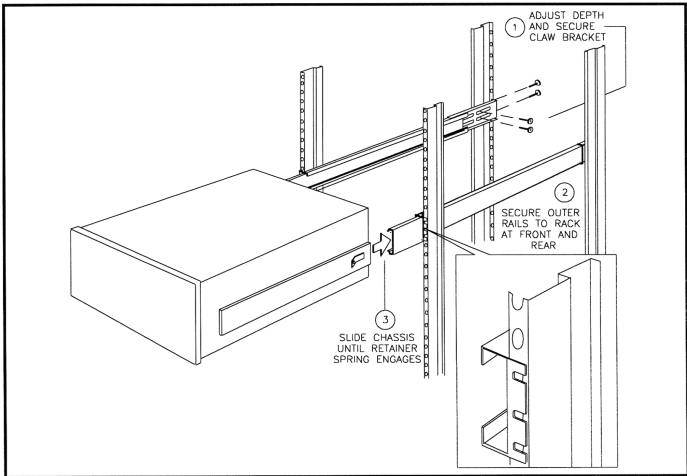
Step 3 Position the outer rails in the rack, adjusting the claw brackets and marking the intended position of the mounting holes both on the front and rear of the rack. Tighten the screws on the claw brackets.

Step 4 Bolt the front of the slides into place using 10-32 x 1/2" pan head screws. Flat head screws are also provided for racks with countersunk holes.

Step 5 Bolt the rear of the slides to the rack side rails using four 10-32 x 3/8" screws. A threaded bracket is provided in case the rack does not have threaded holes. Hex nuts are often difficult to use at the rear of a rack to secure screws.

Step 6 Install the chassis slides into the outer slides in the rack. Push the chassis into the rack until the rear retaining spring engages. Then press the retaining buttons and push the chassis the rest of the way into the rack.

Step 7 Plug the AC power cord into the AC receptacle on the power supply module.



Internal Cabling

The Megaplex Server Chassis provides a removable access panel . The SCSI bus can be arranged into various configurations via the access panel.

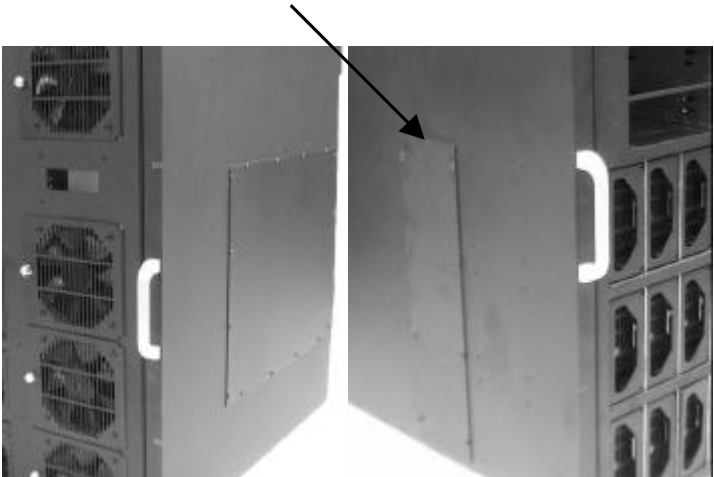
Step 1

Remove the screws securing the access panels.

Step 2

With the access panel removed, the SCSI bus cabling will be accessible and easily reached providing for various configurations.

Access Panels



3 Field Replaceable Units

The field replaceable subassemblies within the Megaplex Server Chassis are described below. The subassemblies in this section are:

- the power supply assemblies and
- the fan module assemblies.

These assemblies can be ordered as spares from AMI.

Power Supply Modules Three 600 watt power supplies support the Megaplex server chassis. The power supplies are located at the rear of the chassis. Each power supply has a power sharing board, which interfaces to the power distribution board located internally in the chassis. DC power is distributed from the power supply module to the power distribution board inside the enclosure and throughout the chassis. Each power supply has two integrated fans.

These fans along with the additional chassis fans provide cooling for the chassis. Only the chassis mounted fans are replaceable. Failure of a power supply fan requires replacement of the affected power supply. To replace a power supply follow the procedure below.

Replacing a Power Supply

The power supply module is hot pluggable. You do not have to shut down the system to replace a power supply.

Step 1

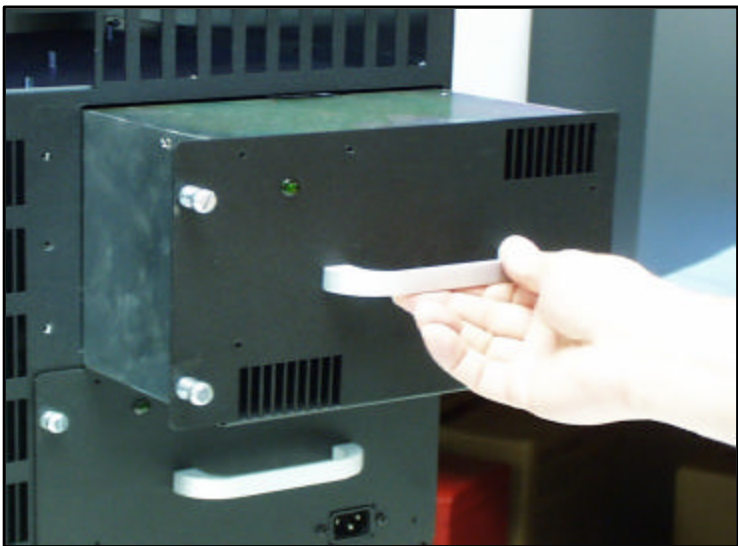
Unplug the AC power cord connected to the failed power supply module.

Step 2

Loosen the thumbscrews that secure the power supply module.

Step 3

Using the handle, remove the power supply module from the chassis.



Step 4

Replace the failed power supply module with a new power supply module and tighten the thumbscrews.

Step 5

Plug in the AC power cord.

Replacing a Fan Module

The chassis mounted fan assembly is easily removed and replaced. Should the fan assembly need replacement use the following procedure. The fan assembly is hot pluggable. You do not have to shut down the system to replace a fan.

Step 1 Loosen the thumb screw that secures the fan module.

Step 2 Slowly remove the fan module from the chassis.



Step 3 Insert the fan module into the chassis, tighten the thumbscrews.

4 Display Panel

The Display Panel module is described below. Included are details of the communications interface for both the standard Inter-Integrated Circuit (I²C) bus interface and Diagnostic Port asynchronous serial line.

The Display Panel is an intelligent data gathering and control module that monitors and reports environmental conditions within the Megaplex enclosure. A 4-line-by-20-character LCD panel provides a medium for the Internal Chassis Computer (ICC) to display information. Four switches are mounted on the Display Panel to provide the ICC with user input for display navigational control. Power and ICC Reset switches are also mounted on the display panel and connect directly with the power supplies and ICC respectively.

Items monitored include power from the various power supplies, module presence, navigation switch and drive fault LED. The LCD information and drive fault LED status are passed from the ICC through the Display Panel I²C interface.

Each enclosure contains one ICC single-board computer with various peripheral devices and SCSI controller connected by a passive backplane capable of interfacing up to twelve SCSI disk drives. Three dual-section supplies power the enclosure, and the Display Panel monitors enclosure conditions and displays messages from the ICC.

Primary communications with the ICC is through a dedicated I²C bus interface. Specifications for the I²C bus can be found in Data Handbook IC20 from Philips Semiconductors. Diagnostic and maintenance functions are implemented on the Display Panel through a single asynchronous serial line interface, which uses the RS232 standard as detailed in the ANSI specifications.

I²C Communications with Display Panel

The ICC communicates with the Display Panel over the common I²C bus in the Megaplex enclosure. The I²C bus is a standard developed by Philips Semiconductors for three-wire serial communications. The self-clocking I²C data pattern is capable of generating Start, Stop, Acknowledge and Not-Acknowledge states that define the data transfer protocol. Data is transferred bi-directionally in eight bit bytes.

J1 I²C Jumper J1 is a four-pin I²C interface. The J1 pinout is:

Pin	Description
1	SCL - Serial Clock
2	Signal Ground
3	SDA - Serial Data
4	Signal Ground

Display Panel Restrictions The Display Panel I²C communications operate under the following restrictions:

- Slave mode only.
 - Maximum transfer rate of 100K bits-per-second.
 - Eight bit addressing only.
 - Does not implement “General Call” functions.
-

I²C Communications Protocol

I²C communications with the Display Panel are achieved by transferring packets of information between the ICC and Display Panel. Packets are divided into write and read class and can contain from four to twenty-four bytes of data. The general packet form for reading and writing data to the Display Panel is shown below.

Write Class Packet Protocol

Byte	Description
Byte 0	Destination Address (always 74h)
Byte 1	Packet ID
Byte 2	Byte Count (2 thru 20) / Data Byte 1

Read Class Packet Protocol

Byte	Description
Byte 0	Destination address (always 74h)
Byte 1	Packet ID
Byte 2	Optional byte count
Byte 2 / 3	Destination address (always 74h)
Byte 3 / 4	Data byte 1
:	
Data byte n	Data byte n

I²C Address The first byte in each packet is the I²C address assigned to the Display Panel.

The first byte is always the hexadecimal 74 address fixed in the Display Panel.

Packet Bytes in Second Byte The second byte defines the nature of the following packet bytes. The following IDs are valid:

ID	Name
01	Report Switch States
02	Report Enclosure Status
03	Enclosure Control
04	LCD Control
05	LCD Status
06	Write LCD Data
07	Read LCD Data

Cont'd

I²C Communications Protocol, Continued

Byte Count A fixed byte count is implied by all but the Write LDC Data and Read LCD Data packets. For these packets only, a byte count follows the ID byte. The value for this byte count must be between 1 to 20. All other packets will not have a byte count since it is presumed that the byte count is a fixed value. If the implied number of bytes are not transferred, an error condition will be generated on the I²C bus.

Data Bytes Write class data packets will include the data bytes following either the ID byte or the Byte count. Read class data packets, however, are divided into two distinct I²C operations using a repeat-start condition. The first operation writes the packet ID and/or a byte count for the number of expected data bytes. It then sends a repeat-start followed by the Display Panel address with a read bit. This signals the Display Panel to return the data indicated by the ID byte and optional byte count.

Command Packets

01 - Report Switch Read Class

This packet returns information on the four Navigation switches on the Display Panel. After a switch pressed state is detected and the status is set internally, it remains until the ICC reads this packet. Following a Report Switch States read, any pressed states are cleared to the Not Pressed state until a pressed condition is again detected.

Byte	Hex Value	Description
0	74 (w)	Display Panel I ² C Address + Write
1	01	Report Switch States ID
2	75 (r)	Display Panel I ² C Address + Read
3		Navigation Switches (1 = Presses, 0 = Not Pressed) Bit 0 Switch 1 Bit 1 Switch 2 Bit 2 Switch 3 Bit 3 Switch 4 Bit 4 Bit 5 Bit 6 Bit 7

Cont'd

Command Packets, Continued

02 - Report Enclosure Status Read Class

This packet returns information on the condition of power and drives in the enclosure.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	02	Report Enclosure Status ID
2	75 (r)	Display Panel PC Address + Read
3		Drive Present Bus A&B (1 = Installed, 0 = Removed) Bit 0 Drive A0 (top-leftmost) Bit 1 Drive A1 (top-left-center) Bit 2 Drive A2 (top-right-center) Bit 3 Drive A3 (top-rightmost) Bit 4 Drive B0 (middle-leftmost) Bit 5 Drive B1 (middle-left-center) Bit 6 Drive B2 (middle-right-center) Bit 7 Drive B3 (middle-rightmost)
4		Drive Present Bus C (1 = Installed, 0 = Removed) Bit 0 Drive C0 (bottom-leftmost) Bit 1 Drive C1 (bottom-left-center) Bit 2 Drive C2 (bottom-right-center) Bit 3 Drive C3 (bottom-rightmost) Bits 4-7 Not used (returns 0)
5		Power Supply Present (1 = Installed, 0 = Removed) Bit 0 Supply 0 Bit 1 Supply 1 Bit 2 Supply 2 Bits 3-7 Not used (returns 0)
6		Power Supply Status (1 = Fault, 0 = Good) Bit 0 Supply 0 - Section A Bit 1 Supply 0 - Section B Bit 2 Not Used (returns 0) Bit 3 Supply 1 - Section A Bit 4 Supply 1 - Section B Bit 5 Not Used (returns 0) Bit 6 Supply 2 - Section A Bit 7 Supply 2 - Section B
7		Power Supply Fan Status (1 = Fault, 0 = Good) Bit 0 Fan A - Supply 0 Bit 1 Fan B - Supply 0 Bit 2 Not Used (returns 0) Bit 3 Fan A - Supply 1 Bit 4 Fan B - Supply 1 Bit 5 Not Used (returns 0) Bit 6 Fan A - Supply 2 Bit 7 Fan B - Supply 2

Command Packets, Continued

03 - Enclosure Control Write Class

This packet controls the drive fault LEDs for bus A, B and C.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	03	Enclosure Control ID
2		Drive Fault LED Bus A&B (1 = On, 0 = Off) Bit 0 Drive A0 (top-leftmost) Bit 1 Drive A1 (top-left-center) Bit 2 Drive A2 (top-right-center) Bit 3 Drive A3 (top-rightmost) Bit 4 Drive B0 (middle-leftmost) Bit 5 Drive B1 (middle-left-center) Bit 6 Drive B2 (middle-right-center) Bit 7 Drive B3 (middle-rightmost)
3		Drive Fault LEDs Bus C (1 = On, 0 = Off) Bit 0 Drive C0 (bottom-leftmost) Bit 1 Drive C1 (bottom-left-center) Bit 2 Drive C2 (bottom-right-center) Bit 3 Drive C3 (bottom-rightmost) Bits 4-7 Not used (returns 0)

04 - LCD Control Write Class

This packet sends commands defined by the LCD display vendor to the LCD.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	04	LCD Control ID
2		LCD Defined command (1 byte). See the <i>LCD Programming</i> section on page 34 for command details.

Cont'd

Command Packets, Continued

05 - LCD Status Read Class

This packet reads status of the LCD as defined by the LCD display vendor.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	05	LCD Status ID
2	75 (r)	Display Panel PC Address + Read
3		LCD Defined Status (1 byte). See the <i>LCD Programming</i> section on page 34 for status details.

06 - Write LCD Write Class

This packet sends data defined by the LCD display vendor to the LCD.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	06	Write LCD Data ID
2	1 – 14	Byte count (1 through 20 bytes)
3 – 23		LCD Data (1 byte). See the <i>LCD Programming</i> section on page 34 for status details.

07 - Read LCD Data Read Class

This packet reads LCD Data as defined by the LCD display vendor.

Byte	Hex Value	Description
0	74 (w)	Display Panel PC Address + Write
1	07	Read LCD Data ID
2	1 – 14	Byte count (1 through 20 bytes)
3	75 (r)	Display Panel PC Address + Read
4 – 24		LCD Data (1 byte). See the <i>LCD Programming</i> section on page 34 for status details.

Diagnostic Port Interface

The Display Panel Diagnostic Port communicates over an asynchronous serial line at RS232-specified levels. The serial line is programmed for 9600 baud, 8 data bits, no parity, and 1 stop bit (8, N, 1) format.

P1 Serial Line Pinout P1 is a 10-pin Serial Line interface. The P1 pinout is:

Pin	Description
1	No connection
2	No connection
3	Received Data (RS232 equivalent of BB)
4	No Connection
5	Transmitted Data (RS232 equivalent of BA)
6	No connection
7	No connection
8	No connection
9	Signal Ground (RS232 equivalent of AB)
10	No connection

Diagnostic Port/Command Interface The Diagnostic Port interface and command language interface uses a common half-duplex communications device.

All communications use ASCII characters to form words, abbreviations, numbers, or control characters. Command and information lines received by the Display Panel must be terminated by a carriage-return to be recognized. Characters sent to the Display Panel are not echoed.

Cont'd

Diagnostic Port Interface, Continued

Command Language In general, the interface uses a mnemonic command language. Commands are encoded in a mnemonic followed by optional data strings, separated by a space. The command structure is

```
cmd [nn [nn]... [nn]]‡
```

where:

cmd is a printable ASCII character command.

Nn is an optional data string.

All entries on the command line must be separated by a space. Additional spaces are ignored. Tabs are not recognized and generate an error. The command line must not exceed 50 characters and must be terminated with a carriage return (shown by the ‡ character). With the exception of the *time* and *stime* commands, data strings must always be in hexadecimal format. Hexadecimal values must be in the range 0 to FF.

Starting and Stopping The Xon and Xoff characters are used to control data transmission. An Xoff character received by the Display Panel causes suspension of any data being transmitted. Data transmission resumes when the Display Panel receives an Xon character. Likewise, the Display Panel transmits an Xoff character to suspend receiving data. Once it can receive additional data, it sends the Xon character. This protocol prevent overrunning the small (60 character) buffers.

Cont'd

Diagnostic Port Interface, Continued

Receiving Commands When the Display Panel has initialized, it transmits the > prompt to indicate it is able to receive commands. This will happen only on the Diagnostic Port. When the Display Panel receives a command on the Diagnostic Port, it returns the prompt character (>) to indicate it has completed the operation and is able to receive commands. The prompt character is actually a string consisting of a line-feed, carriage-return, and the > character followed by a space.

After a command is issued, only the Xon/Xoff sequence and Escape character are accepted until the command has completed execution, as indicated by the returned prompt. Sending the Escape character during command execution will abort the command in progress, and cause the prompt to be returned. The time required and resulting action when aborting a command depends on the state of the command at the time the Escape character is received.

Syntax Errors The command parser checks for exact input and rejects anything it cannot understand with a coded error response. The command parser does not allow corrections (backspace, etc.). If you type an incorrect character or you simply wish to abort the input, press <Esc> to kill the input string.

Display Panel Returns In response to a received command, the Display Panel returns one of the following:

- The requested data (in hexadecimal byte format).
- An encoded error message.

The prompt (>) follows to indicate completion of the command and readiness to accept another.

Diagnostic Port Commands

The Diagnostic Port commands in the Display Panel are:

Command	Description
chstat	Get enclosure status
drvled <dat> <dat>	Change drive fault LEDs
echo	Echo I ² C communications
enq	Retrieve enclosure ID and firmware version information
help	Displays a help screen showing the commands and syntax
i2c	Displays the status of I ² C bus
lcdcmd <dat>	Send a command to the LCD controller
lcdat <n> <dat>.. <dat>	Send a number of data bytes to the LCD controller
lcdstat	Read the LCD status
lcdtest	Initiate a test of the LCD display
ledtest	Test Drive Fault LEDs
mode	Show the current mode (real or simulated)
mute	Return Diagnostic Port from echo mode
rdlcd <n>	Read LCD a number of data bytes
real	Set real world mode
setcan <dat> <dat>	Set simulated CANIN status registers
setfanstat <dat>	Set simulated fan status register
setpsi <dat>	Set simulated power supply installed register
setpsstat <dat>	Set simulated power supply status register
Sim	Simulate input registers
Stime <hr> <min> <sec>	Set current time
Switches	Display the current switch states
Time	Show current time of day

Legend

- <dat> Data byte (range 0 to 0FF).
 - <n> Number of data bytes for LCD (range 0 to C).
 - <hr> Current hour (24 hour time (0 to 23)).
 - <min> Current minute (0 to 59).
 - <sec> Optional second value (0 to 59). If not given, time will be set to 0 seconds.
-

Command Responses

The Display Panel generates two classes of response to a received command:

- completion or
- error

The successful completion of a command that returns information will produce the expected data in two character hexadecimal pairs. Multiple data pairs will be separated by a single space. For example, the status command might look like the following:

```
>chstat ff 0f 07 00 00  
>
```

If the command could not complete successfully, an error code is returned. This response is in the form “EC: nn”, where

EC: indicates that this is an error code and

nn represents the unique hexadecimal code for a specific error.

Error Codes The following error responses are possible:

Code	Meaning
01	The received command was not recognized.
02	The accompanying argument is invalid.
03	An error occurred during command execution.
10	The serial buffer overflowed on input.

Alarm Codes

In addition to responses solicited by a command, there are a number of possible unsolicited messages that may be sent over the Asynchronous Serial line. These messages occur when an alarm condition is sent to the Display Panel. Alarm messages take the form “AC: nn”, where “AC:” indicates this is an alarm message and “nn” represents the hexadecimal code for the alarm. The following alarm codes are possible:

Code	Description
F0	A cannister state (in/out) has changed.
F1	A navigation switch has been pressed.
F2	An error occurred while communicating on the external I ² C bus.
F3	A canister state has changed (either in or out).
F4	A power supply state has changed (either in or out).
F6	The I ² C bus has failed.
FF	An unidentifiable alarm has occurred.

Diagnostic Port Commands

This section describes in detail the commands used to interface with the Display Panel. Commands are listed in alphabetical order for easier reference.

Chstat

Get Enclosure Status

This command emulates the I²C packet Report Enclosure Status. It retrieves the five-byte status of this enclosure. The definition of each status data byte is:

Drive Present Bus A&B (Byte 1): (1 = Installed, 0 = Removed).

- Bit 0 (LSB): Drive A0 (top-leftmost)
- Bit 1: Drive A1 (top-left-center)
- Bit 2: Drive A2 (top-right-center)
- Bit 3: Drive A3 (top-rightmost)
- Bit 4: Drive B0 (middle-leftmost)
- Bit 5: Drive B1 (middle-left-center)
- Bit 6: Drive B2 (middle-right-center)
- Bit 7 (MSB): Drive B3 (middle-rightmost)

Drive Present Bus C (Byte 2): (1 = Installed, 0 = Removed).

- Bit 0 (LSB): Drive C0 (bottom-leftmost)
- Bit 1: Drive C1 (bottom-left-center)
- Bit 2: Drive C2 (bottom-right-center)
- Bit 3: Drive C3 (bottom-rightmost)
- Bit 4: Not used (returns 0)
- Bit 5: Not used (returns 0)
- Bit 6: Not used (returns 0)
- Bit 7 (MSB): Not used (returns 0)

Power Supply Present (Byte 3) (1 = Installed, 0 = Removed)

- Bit 0 (LSB): Supply 0
- Bit 1: Supply 1
- Bit 2: Supply 2
- Bit 3: Not used (returns 0)
- Bit 4: Not used (returns 0)
- Bit 5: Not used (returns 0)
- Bit 6: Not used (returns 0)
- Bit 7 (MSB): Not used (returns 0)

Cont'd

Diagnostic Port Commands, Continued

Chstat Get Enclosure Status, cont'd

Power Supply Status (Byte 4)(1 = Fault, 0 = Good):

Bit 0 (LSB): Supply 0 - Section A
Bit 1: Supply 0 - Section B
Bit 2: Not used (returns 0)
Bit 3: Supply 1 - Section A
Bit 4: Supply 1 - Section B
Bit 5: Not used (returns 0)
Bit 6: Supply 2 - Section A
Bit 7 (MSB): Supply 2 - Section B

Power Supply Fan Status (Byte 5) (1 = Fault, 0 = Good):

Bit 0 (LSB): Supply 0 - Section A
Bit 1: Supply 0 - Section B
Bit 2: Not used (returns 0)
Bit 3: Supply 1 - Section A
Bit 4: Supply 1 - Section B
Bit 5: Not used (returns 0)
Bit 6: Supply 2 - Section A
Bit 7 (MSB): Supply 2 - Section B

drvled <dat> <dat>

This command emulates the Enclosure Control I²C packet, and sets or resets drive fault LEDs.

Drive Fault LED Bus A&B (Byte 1): (1 = On, 0 = Off).

Bit 0 (LSB): Drive A0 (top-leftmost)
Bit 1: Drive A1 (top-left-center)
Bit 2: Drive A2 (top-right-center)
Bit 3: Drive A3 (top-rightmost)
Bit 4: Drive B0 (middle-leftmost)
Bit 5: Drive B1 (middle-left-center)
Bit 6: Drive B2 (middle-right-center)
Bit 7 (MSB): Drive B3 (middle-rightmost)

Drive Fault LED Bus C (Byte 2): (1 = On, 0 = Off).

Bit 0 (LSB): Drive C0 (bottom-leftmost)
Bit 1: Drive C1 (bottom-left-center)
Bit 2: Drive C2 (bottom-right-center)
Bit 3: Drive C3 (bottom-rightmost)
Bit 4: Not used (returns 0)
Bit 5: Not used (returns 0)
Bit 6: Not used (returns 0)
Bit 7 (MSB): Not used (returns 0)

Cont'd

Diagnostic Port Commands, Continued

Echo

Echo I²C Communications

This command sets the Diagnostic port to output the equivalent byte values for all I²C communications as they occur. I²C input to the Display Panel is sent over the Diagnostic Port preceded by the “<-“ character string. I²C output from the Display Port is sent preceded by the “->” string. To return the Diagnostic Port to normal operations use the mute command.

Enq

Enquire about Enclosure ID and Firmware Version

This command returns information about the enclosure and the firmware version in the following string:

```
AMI MegaPlex  
Firmware Revision x.x
```

The “x.x” portion represents the current firmware major and minor version number.

Help

Show Help Screen

This command returns one or more screens of information summarizing the command set available to the Diagnostic Port.

I2C

Display Internal I²C Device Status

The status of the I²C bus is returned with this command. This is used exclusively for diagnostic purposes.

lcdcmd <dat

Send Command to the LCD

This function sends the command byte contained in the <dat> field to the LCD controller. See *LCD Programming* section on page 34 for details on the LCD command set.

Cont'd

Diagnostic Port Commands, Continued

lcdat <n> <dat>.<dat> Send Command to right LCD

This function sends “n”(1 to 20) data bytes to the LCD controller. See the *LCD Programming* section on page 34 for details on the LCD data.

Lcdstat Read the LCD Status

This command returns one byte representing the status of the LCD controller. See the *LCD Programming* section on page 34 for details on the LCD status.

Lcdtest Test the LCD

This command writes four lines of incrementing numeric data to the LCD display. The first line begins with 1. Each following line begins with the line number and increments to 0. The incrementing pattern is repeated for the remainder of the line.

Ledtest Test Drive Fault LEDs

This command initiates a 10 second test of the drive fault LEDs. Beginning with the top-leftmost LED (drive A0), each led is in-turn illuminated and extinguished.

Mode Display Current Mode

This command reads and displays the current, real or simulated, echo or mute, mode of operation.

Mute End the Echo Mode

This command returns the Diagnostic Port to normal mode of operation from the echo mode.

rdlcd <n> Read LCD Data

This command reads and displays “n” (1 to 20) bytes of data from the LCD controller. See the *LCD Programming* section on page 34 for details on the LCD data.

Cont'd

Diagnostic Port Commands, Continued

Real Set Real World Mode

This command restores the Display Panel normal operation mode where all input is taken from actual registers in the system. For details on simulated register mode see the sim command description.

setcan <dat> <dat> Set Simulated Cannister Registers

This command sets the simulated cannister register values.

Drive Present Bus A&B (Byte 1): (0 = Installed, 1 = Removed).

Bit 0 (LSB): Drive A0 (top-leftmost)
Bit 1: Drive A1 (top-left-center)
Bit 2: Drive A2 (top-right-center)
Bit 3: Drive A3 (top-rightmost)
Bit 4: Drive B0 (middle-leftmost)
Bit 5: Drive B1 (middle-left-center)
Bit 6: Drive B2 (middle-right-center)
Bit 7 (MSB): Drive B3 (middle-rightmost)

Drive Present Bus C (Byte 2): (0 = Installed, 1 = Removed).

Bit 0 (LSB): Drive C0 (bottom-leftmost)
Bit 1: Drive C1 (bottom-left-center)
Bit 2: Drive C2 (bottom-right-center)
Bit 3: Drive C3 (bottom-rightmost)
Bits 4-7: Not used (returns 0)

setfanstat <dat> Set Simulated Fan Status Register

This command sets the simulated fan status register values.

Power Supply Fan Status (1 = Fault, 0 = Good):

Bit 0 (LSB): Supply 0 - Section A
Bit 1: Supply 0 - Section B
Bit 2: Not used (returns 0)
Bit 3: Supply 1 - Section A
Bit 4: Supply 1 - Section B
Bit 5: Not used (returns 0)
Bit 6: Supply 2 - Section A
Bit 7 (MSB): Supply 2 - Section B

Cont'd

Diagnostic Port Commands, Continued

setpsi <dat> Set Simulated Power Supply Installed Register

This command sets the simulated power supply installed register values.

- Power Supply Present_ (0 = Installed, 1 = Removed)
- Bit 0 (LSB): Supply 0
- Bit 1: Supply 1
- Bit 2: Supply 2
- Bit 3: Not used (returns 0)
- Bit 4: Not used (returns 0)
- Bit 5: Not used (returns 0)
- Bit 6: Not used (returns 0)
- Bit 7 (MSB): Not used (returns 0)

setpsstat <dat> Set Simulated Power Supply Status Register

This command sets the simulated power supply status register values.

- Power Supply Status (Byte 4)(1 = Fault, 0 = Good):
 - Bit 0 (LSB): Supply 0 - Section A
 - Bit 1: Supply 0 - Section B
 - Bit 2: Not used (returns 0)
 - Bit 3: Supply 1 - Section A
 - Bit 4: Supply 1 - Section B
 - Bit 5: Not used (returns 0)
 - Bit 6: Supply 2 - Section A
 - Bit 7 (MSB): Supply 2 - Section B
-

Sim Use Simulated Register

This command allows the Display Panel to operate without being connected to enclosure outputs. This is useful for simulating various conditions to test operations that might be difficult to originate. The CANIN, Power Supply Status, Power Supply Installed, Power Supply Fan and Switch registers are simulated internally, and values can be set by Diagnostic Port commands. To return to real input use the real command.

Cont'd

Diagnostic Port Commands, Continued

time <hr> <min> <sec> Set Time of Day

This command sets the current time of day in the enclosure Display Panel. The format for the time is standard 24 hour Military style time. The values passed are in decimal format for ease of reading. The data bytes passed are:

<hr>	Hour (0 to 23)
<min>	Minutes (0 to 59)
<sec>	Seconds (0 to 59)

Time Display Current Time

This command retrieves the three byte current time from the enclosure Display Panel. The values passed are in decimal format for ease of reading. Time bytes are defined as:

Hour (Byte 1)	0 to 23
Minute (Byte 2)	0 to 59
Second (Byte 3)	0 to 59

LCD Programming

The Display Panel has a Liquid Crystal Display (LCD) that can display four lines of twenty characters each. Four registers define the virtual interface for the display:

- command register,
 - Status register,
 - write data register, and
 - read data register.
-

LCD Character Font A character font (5x7) is provided in an internal character generator ROM. You can program a new font in the Character Generator (CG) RAM. Characters are indexed from either the CG RAM or a selected character generator ROM font to the display cursor position by the Data Display (DD) RAM.

Cont'd

LCD Programming, Continued

Passing Commands and Data Commands, status, and data are passed directly to and from the LCD via either the appropriate I²C packet or using the Diagnostic Port command. Timing and command and data accuracy are the programmer's responsibility. Great care must be taken to make sure that LCD execution times are not violated to ensure proper LCD operation.

LCD ROM The LCD panel internal ROM holds 192 characters in a 5x7 dot matrix. Each character block is addresses separately and can form alphanumeric characters and a limited number of symbols. Characters are mapped in an expanded ASCII format. See the Character Font Codes on page 46 for detailed information.

LCD Instructions

Introduction Intelligent dot matrix liquid crystal display modules have onboard controller and LSI drivers, which display alpha numerics, Japanese Kata Kana characters and a wide variety of other symbols in a 5 x 7 dot matrix.

INSTRUCTION CODES

Instruction	Set		Instruction Code								Description	Execution Time (when f_{CP} or f_{OSC} is 250 kHz)	
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0			
Clear Display	0	0	0	0	0	0	0	0	0	0	1	Clears all display memory and returns the cursor to the home position (Address 0).	82 μ s - 1.64ms
Return Home	0	0	0	0	0	0	0	0	0	1	*	Returns the cursor to the home position (Address 0) shifted to the original position. DD RAM contents remain unchanged.	40 μ s - 1.6ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/O	S	Sets the cursor move direction and specifies to or not to shift the display. These operations write and read.	40 μ s - 1.64ms
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	(D) is display ON/OFF control; memory remains unchanged in OFF condition. (C) cursor ON/OFF (B) blinking cursor.	40 μ s
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*		Moves the cursor and shifts the display without changing DD RAM contents.	40 μ s
Function Set	0	0	0	0	1	DL	N	F	*	*		Sets interface data length (DL), number of display lines (N), and character font (F).	40 μ s
Set CG RAM Address	0	0	0	1	A_{CG}							Sets the CG RAM address. CG RAM data is sent and received after this setting.	40 μ s
Set DD RAM Address	0	0	1	A_{DD}							Sets the DD RAM address. DD RAM data is sent and received after this setting.	40 μ s	
Read Busy Flag & Address	0	1	BF	AC							Reads Busy Flag (BF) indicating internal operation is being performed and reads address counter contents.	1 μ s	
Write Data to CG or to DD RAM	1	0	Write Data							Writes data into DD RAM or CG RAM.	40 μ s		
Read Data from CG or DD RAM	1	1	Read Data							Reads data from DD RAM or CG RAM.	40 μ s		

* Doesn't matter

DD RAM: Display data RAM

CG RAM: Character generator RAM

A_{CG} : CG RAM address

A_{DD} : DD RAM address corresponds to cursor address

A_C : Address counter used for both DD RAM and CG RAM address

I/D = 1: Increment

I/D = 0: Decrement

S = 1: Display shift

S = 0: No display shift

D = 1: Display ON

D = 0: Display OFF

C = 1: Cursor ON

C = 0: Cursor OFF

B = 1: Blink ON

B = 0: Blink OFF

S/C = 1: Display shift

S/C = 0: Cursor movement

BF = 1: Internal operation in progress

BF = 0: Instruction can be accepted

R/L = 1: Right shift

R/L = 0: Left shift

DL = 1: 8 bits

DL = 0: 4 bits

N = 1: 2 lines (L1671)

F = 0: 5 x 7 dot matrix

Execution times in the above table indicate the minimum values when operating frequency is 250 kHz.

When f_{OSC} is 270 kHz: $40\mu s \times 250/250 = 37\mu s$

D = 5.0VW5%, V SS = 0V, T A = 0

Cont'd

LCD Programming, Continued

Address Counter (AC) The counter specifies an address when data is written into DD RAM or CG RAM and the data stored in DD RAM or CG RAM is read out. If an Address Set instruction (for DD RAM or CG RAM) is written in the IR, the address information is transferred from the IR to the AC. When display data is written into or read from DD RAM or CG RAM, the AC is automatically incremented or decremented by one according to DB0 to DB6. See the Register Selection Table section on page 41 for when RS = 0 and R/W = 1.

Clear Display

	DB7 _DB0							
Code	0	0	0	0	0	0	0	1

This command clears all display memory and returns the cursor to the home position. The cursor returns to the first character block on the first line on all 1-, 2-, and 4-line character modules.

Cursor Home

	DB7 _DB0								
Code	0	0	0	0	0	0	1	*	

* Does not matter

This command returns the cursor to the home position. The first line first character blocks on all 1, 2 and 4 line are displayed. The contents of DD RAM remain unchanged.

Cont'd

LCD Programming, Continued

Restrictions on Display Clear and Cursor Home Instructions

Conditions of use	Restrictions
When executing the Display Clear or Cursor Home instruction when the display is shifted (after execution of Display Shift instruction).	<p>The Cursor Home instruction should be executed again immediately after the Display Clear or Cursor Home instruction is executed. Do not leave an interval of a multiple of $400/f_{OSC}$ * second after the first execution.</p> <ul style="list-style-type: none"> • L4052: $f_{OSC} = 250$ kHz • The other modules: $f_{OSC} = 270$ kHz <p>*f_{OSC} : Oscillation frequency</p>
When 23H , 27H , 63H , or 67H is used as a DD RAM address to execute Cursor Home instruction.	<p>Before executing the Cursor Home instruction, the data of the four DD RAM addresses given at the left should be read and saved. After execution, write the data again in DD RAM. (This restriction is necessary to prevent the contents of the DD RAM addresses from being destroyed after the Cursor Home instruction has been executed.)</p>

Entry Mode Set

Code	DB7	_	DB0							
	0	0	0	0	0	0	1	I/D	S	

Code	Description
I/D	Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by one block when writing or reading a character code from DD Ram or CG RAM. The cursor automatically moves to the right when incremented by one or to the left if decremented by one.
S	Shifts the entire display to either the right or left. When S = 1 (high). When S = 1 and I/D = 1 the display shifts one position to the left. When S = 1 (high). When S = 1 and I/D = 0 the display shifts one position to the right. This right or left shift occurs after each data write to DD RAM. Display is not shifted when reading from DD RAM. Display is not shifted when S = 0.

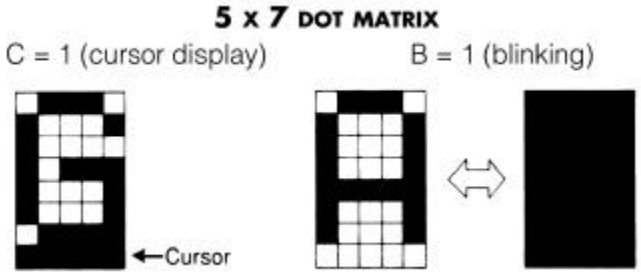
Cont'd

LCD Programming, Continued

Display and Cursor ON/OFF Control

Code	DB7	_	DB0	0	0	0	0	1	D	C	B
------	-----	---	-----	---	---	---	---	---	---	---	---

Code	Description
D	Display is turned ON when D = 1 and OFF when D = 0. When display is OFF, display data in DD RAM remains unchanged. Information returns immediately when D = 1 is entered.
C	Cursor is displayed when C = 1 and not displayed when C = 0. If the cursor disappears, function of I/D etc. does not change during data write. In a 5 x 7 dot matrix there is an eighth line which functions as the cursor.
B	1 the character at the cursor position starts blinking. 0 the cursor does not blink. The blink is done by stitching between the all-black dot matrix and displayed character at 0.4 second intervals. The cursor and the blink can be set at the same time (fosc = 250 kHz).



Cursor or Display Shift

Code	DB7	DB6	DB5	DB4	S/C	R/L	*	*
*	0	0	0	1	S/C	R/L	*	*

* Does not matter

The Cursor/Display Shift command moves the cursor or shifts the display without changing the DD RAM contents.

The cursor position and the AC contents match. This instruction is available for display correction and retrieval because the cursor position or display can be shifted without writing or reading display data.

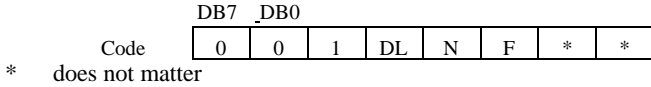
With a two-line display, the cursor is shifted from character block 40 of line 1 to character 1 of line 2. Displays of lines 1 and 2 are shifted at the same time. In case of a 4-line display, the cursor does not move continuously from line 2 to line 3. The cursor is shifted from character block 40 of line 3 to character block 1 of line 4. Displays of lines 3 and 4 are shifted at the same time. The display pattern of line 2 or 4 is not shifted to line 1 or 3.

S/C	R/L	Operation
0	0	The cursor position is shifted to the left (the AC decrements one)
0	1	The cursor position is shifted to the right (the AC increments one)
1	0	The entire display is shifted to the left with the cursor
1	1	The entire display is shifted to the right with the cursor

Cont'd

LCD Programming, Continued

Function Set

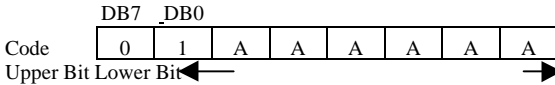


The Function Set command sets the interface data length, the number of display lines and the character font.

Parameter	Description
DL	Interface data length. 1 data length is set at 8 bits (DB7 to DB0). 0 data length is set at 4 bits (DB7 to DB4). The upper 4 bits are transferred first, then the lower 4 bits follow.
N	Number of display lines
F	Sets the character font

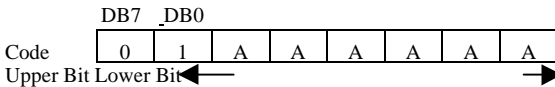
The Function Set instruction must be executed prior to all other instructions except for Busy Flag/Address Read. If another instruction is executed first, no function instruction except changing the interface data length can be executed.

CG RAM Address Set



CG RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in CG RAM is written from or read to the MPU.

DD RAM Address Set

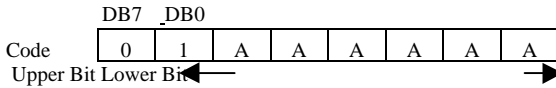


DD RAM addresses, expressed as binary AAAAAA, are set to the AC. Then data in DD RAM is written from or read to the MPU.

Cont'd

LCD Programming, Continued

Busy Flag / Address Read



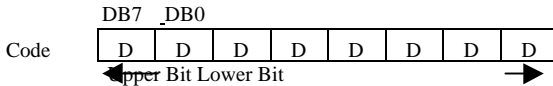
The BF signal can be read to verify if the controller is indicating that the module is working on a current instruction.

When BF = 1, the module is working internally and the next instruction cannot be accepted until the BF value becomes 0.

When BF = 0, the next instruction can be accepted.

Therefore, make sure that BF = 0 before writing the next instruction. The AC values of binary AAAAAA are read out at the same time as reading the busy flag. The AC addresses are used for both CG RAM and DD RAM but the address set before execution of the instruction determines which address is to be used.

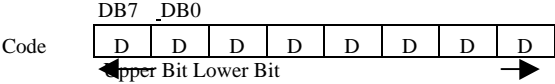
Data Write to CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. After the write operation, the address and display shift are determined by the entry mode setting.

Cont'd

Data Read from CG RAM or DD RAM



Binary eight-bit data DDDDDDDD is read from CG RAM or DD RAM. The CG RAM Address Set instruction or the DD RAM Address Set instruction before this instruction selects either RAM. In addition, either instruction is executed immediately before this instruction. If no Address Set instruction is executed before a read instruction, the first data read becomes invalid. If read instructions are executed consecutively, data is normally read from the second time. However, if the cursor is shifted by the Cursor Shift instruction when reading DD RAM, there is no need to execute an address set instruction because the Cursor Shift instruction does this.

After the read operation, the address is automatically incremented or decremented by one according to the entry mode, but the display is not shifted.

The AC is automatically incremented or decremented by one according to the entry mode after a write instruction is executed to write data in CG RAM or DD RAM. However, the data of the RAM selected by the AC are not read out even if a read instruction is executed immediately afterwards.

5 x 7 + Cursor

The relationships between CG RAM addresses, character codes (DD RAM), and character patterns (CG RAM data 5 x 7 dot matrix) are shown below:

Character code (DD RAM data)							CG RAM address							Character pattern (CG RAM data)													
7	6	5	4	3	2	1 0	5	4	3	2	1	0	7	6	5	4	3	2	1	0							
Upper bit				Lower bit R			Upper bit				Lower bit R			Upper bit				Lower bit R									
0 0 0 0 * 0 0 0							0 0 0							0	0	0	*	*	*	1	1	1	1	0	Example of character pattern (R)		
														0	0	1				1	0	0	0	1			
														0	1	0				1	0	0	0	1			
														0	1	1				1	1	1	1	0			
														1	0	0				1	0	1	0	0			
														1	0	1				1	0	0	1	0			
														1	1	0				1	0	0	0	1			
														1	1	1				*	*	*	0	0		0	0
0 0 0 0 * 0 0 1							0 0 1							0	0	0	*	*	*	1	0	0	0	1	Example of character pattern (W)		
														0	0	1				0	1	0	1	0			
														0	1	0				1	1	1	1	1			
														0	1	1				0	0	1	0	0			
														1	0	0				1	1	1	1	1			
														1	0	1				0	0	1	0	0			
														1	1	0				0	0	1	0	0			
														1	1	1				*	*	*	0	0		0	0
0 0 0 0 * 1 1 1							1 1 1							1	0	0											
														1	0	1											
														1	1	0											
														1	1	1				*	*	*					

In CG RAM data, 1 corresponds to Selection and 0 to Non-selection on the display. Character code bits 0 to 2 and CG RAM address bits 3 to 5 correspond with each other (three bits, eight types). CG RAM address bits 0 to 2 specify a line position for a character pattern. Line 8 of a character pattern is the cursor position where the logical sum of the cursor and CG RAM data is displayed. Set the data of line 8 to 0 to display the cursor. If the data is changed to 1, one bit lights, regardless of the cursor.

The character pattern column position corresponds to CG RAM data bits 0 to 4 and bit 4 comes to the left end. CG RAM data bits 5 to 7 are not displayed but can be used as general data RAM. When reading a character pattern from CG RAM, set to 0 all of character code bits 4 to 7. Bits 0 to 2 determine which pattern will be read out. Since bit 3 is not valid, 00_H and 08_H select the same character.

Programming the Character Generator RAM (CGRAM)

The character generator RAM (CG RAM) allows you to create up to eight custom 5 x 7 characters + cursor (5 x 8). After it is programmed, the custom characters or symbols are accessed exactly as if they were in ROM. However since the RAM is a volatile memory, power must be continually maintained. Otherwise, the custom characters/symbols must be programmed into non-volatile external ROM and sent to the display after each display initialization. All dots in the 5 x 8 dot matrix can be programmed, which includes the cursor position.

Types of CG RAM The modules RAM are divided into two parts:

- data display RAM (DD RAM) and
 - custom character generator RAM (CG RAM).
-

Programming CG ROM This activity is not to be confused programming the custom character generator RAM with the 192 character generator ROM.

CG RAM Location The CG RAM is located between hex 40 and 7F and is contiguous. Locations 40 thru 47 hold the first custom character (5 x 8), 48 thru 4F hold the second custom character, 50 thru 57 hold the third CG, and so forth to 78 thru 7F for the eighth CG character/symbol.

If during initialization the display was programmed to automatically increment, only the single initial address, 40, need be sent. Consecutive row data will automatically appear at 41, 42, etc. until the completed character is formed. All eight custom CG characters can be programmed in 64 consecutive “writes” after sending the single initial 40 address.

Cont'd

Programming CGRAM, Continued

CG RAM Width The CG RAM is 8 bits wide. Only the rightmost 5 bits are used for a custom CG character row. The leftmost dot of programming the CG RAM character corresponds to D4 in the most significant nibble (xxxD4) of the data bus code. The remaining four dots in the row correspond to the least significant nibble (D3 thru D0). D0 is the rightmost dot. 1Fh equals all dots on. 00h equals all dots off. 15h (10101) equals 3 dots on. 0Ah (01010) equals two dots on. The key 5 bits of the 8-bit code program one row of a custom CG character. When all 7 or 8 rows are programmed, the character is complete. The RS R/W Data Display Description is shown below:

RS	R/W	Data	Display	Description
0	0	40	-	Addresses 1st row, 1st CG character
1	0	11	**	Result of 11, 1 st row
1	0	0A	**	Result of 0A, 2 nd row
1	0	1F	*****	Result of 1F, 3 rd row
1	0	04	*	Result of 04, 4 th row
1	0	1F	*****	Result of 1F, 5 th row
1	0	04	*	Result of 04, 6 th row
1	0	04	*	Result of 04, 7 th row
1	0	00	-	Result of 00, 8 th row (cursor position)
1	0	15	***	1st row, 2nd CG character. Addressing not now required. Hex 48 is next in the sequence.

Address Locations L2034-Series (20 characters x 4 lines)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
Line 1	80	81	82	83	84	85	86	87	88	89	8A	8B	8C	8D	8E	8F	90	91	92	93
Line 2	C0	C1	C2	C3	C4	C5	C6	C7	C8	C9	CA	CB	CC	CD	CE	CF	D0	D1	D2	D3
Line 3	94	95	96	97	98	99	9A	9B	9C	9D	9E	9F	A0	A1	A2	A3	A4	A5	A6	A7
Line 4	D4	D5	D6	D7	D8	D9	DA	DB	DC	DD	DE	DF	E0	E1	E2	E3	E4	E5	E6	E7

Programming CGRAM, Continued

CHARACTER FONT CODES (5 x 7 DOT MATRIX)

Upper 4 Bit Hexadecimal

Lower 4 Bit Hexadecimal

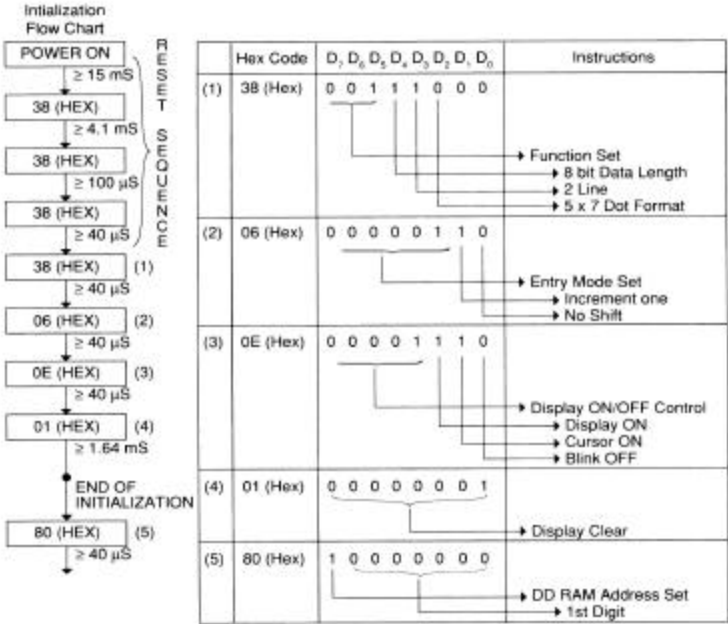
Lower 4 bits Upper 4 bits	0000 (0)	0010 (2)	0011 (3)	0100 (4)	0101 (5)	0110 (6)	0111 (7)	1010 (A)	1011 (B)	1100 (C)	1101 (D)	1110 (E)	1111 (F)
CG RAM (1)			0	a	P	`	p		-	9	E	o	p
	(2)	!	1	A	Q	a	q	a	7	7	4	ä	q
	(3)	"	2	B	R	b	r	r	イ	ウ	×	ß	ø
	(4)	#	3	C	S	c	s	l	ウ	7	E	e	o
	(5)	\$	4	D	T	d	t	\	I	ト	†	µ	ø
	(6)	%	5	E	U	e	u	.	†	†	1	ç	ü
	(7)	&	6	F	V	f	v	7	h	ニ	ヨ	ρ	Σ
	(8)	'	7	G	W	g	w	7	†	7	7	g	π
	(9)	(8	H	X	h	x	イ	o	7	ウ	r	ã
	(A))	9	I	Y	i	y	ウ	7	7	7	ı	y
	(B)	*	:	J	Z	j	z	±	コ	h	7	j	¶
	(C)	+	;	K	[k	[†	ウ	ヒ	o	°	¶
	(D)	,	<	L	¥	l	ı	†	シ	7	7	¢	¶
	(E)	-	=	M]	m]	ı	ズ	^	7	t	÷
	(F)	.	>	N	^	n	+	ヨ	ヒ	7	7	ñ	
	(F)	/	?	O	_	o	+	ウ	7	7	7	ö	■

Example of 8-Bit Data Transfer Operation

Display Initialization Each time the module is turned on or reset, an initialization procedure must be executed. The procedure consists of sending a sequence of hex codes from the microprocessor or parallel I/O port. The initialization sequence turns on the cursor, clears the display, and sets the module onto an auto-increment mode.

The initial hex code 30, 34, or 38 is sent two or more times to ensure the module enters the 8-bit mode.

EXAMPLE FOR THE MODULE WITH 5 x 7 Character Format Under 8-Bit Data Transfer



Note:

Both the RS and R/W terminals are “0” in this sequence. RS, R/W and Data are latched at the falling edge of the Enable signal. The falling edge is typically 10 ns. The maximum is 25 ns.

LCD Interface Problems and Possible Solutions

Although the following problems and possible solutions are not all inclusive, they do represent the most common problems experienced, not only by the first-time user, but also experienced users. If you have a problems please review the following:

Problem Symptoms	Possible Solutions
<p>The display is blank after power is turned on and the system is initialized.</p>	<p>Check the +5 VDC and ground lines and connections.</p> <p>A variable resistor or fixed resistor must be used on the V_{LC} pin for all LCD modules. The V_{LC} voltage range is: 0~ .7 volts (ref: Contrast Adjustent Circuit).</p> <p>Data is being transmitted too fast. Wait 4.5 ms after power on or until V_{DD} reaches 4.5 volts. Wait more than 15 ms after V_{DD} reaches 4.5 volts. Allow 1.6 ms after entering hexadecimal 01 or 02 at the end of the initialization sequence, then enter data. The time interval between other data entries should be 50 μs or greater.</p> <p>Failure to properly initialize the display. Check initialization examples. Enter the first hexadecimal entry at least twice in the initialization sequence.</p> <p>The LCD input is assumed to be configured as an IC. This is not correct. Check the time interval on the falling edge of the enable pulse. It should not exceed 25 ns (its is typically 10 ns).</p>
<p>Incorrect information is displayed</p>	<p>Data is being transmitted too fast. Wait 4.5 ms after power on or until V_{DD} reaches 4.5 volts. Wait more than 15 ms after V_{DD} reaches 4.5 volts. Allow 1.6 ms after entering hexadecimal 01 or 02 at the end of the initialization sequence, then enter data. The time interval between other data entries should be 50 μs or greater.</p> <p>Failure to properly initialize the display. Check initialization examples. Enter the first hexadecimal entry at least twice in the initialization sequence.</p> <p>Check the time interval on the falling edge of the enable pulse. It should not exceed 25 ns. It is typically 10 ns. The enable pulse width is shorter than 450 ns. More than one external bus is being selected. Check the data bus connection. The signal levels are too low. Make sure that $V(1H)$ is more than 2.4 volts.</p>

Problem Symptoms	Possible Solutions
Incorrect information is being displayed and multiple components are tied to the data bus.	More than one external bus being selected. Check the data bus connection. The signal levels are too low. Make sure that V(1H) is more than 2.4 volts. All data bus components do not have TTL type outputs.
The ICs are hot.	Check +5 VDC and ground lines and connections. The V _{DD} and V _{SS} pins are reversed. Too much voltage on V _{DD} – (Max. 7 VDC). The load is being put on data lines when power is off on the V _{DD} pin.
Cannot enter information to the 2 nd , 3 rd , or 4 th lines.	Failure to properly initialize the display. Check initialization examples. Enter the first hexadecimal entry at least twice in the initialization sequence. Check the address locations for the first position on the second line for each two lines (ref: Address Location Chart).

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