82430HX PCIset

P55-TH

ISA PCI MotherBoard

with Onboard PCI IDE and Super Multi-I/O.

The specification is subject to change without notice.

Contents

Chapter 1
Introduction

The P55-TH motherboard is a high performance system hardware based on Intel Pentium® processor and is equipped with four PCI slots, four standard ISA slots, Super Multi-I/O controller and dual ports PCI-IDE connectors for the future expansion. The hardware dimension is 220mm x 280mm with four layer design technology.

Specification

- Intel **Pentium®** Processor operating at **50/75, 60/90, 66/100, 60/120, 66/133, 60/150, 66/166 MHz** and **P54C/P54CTB/P55C** with **321 ZIF socket 7** and scalability to accept faster Pentium® Processors in the feature.
- Supports up to 512 MegaBytes DRAM(minimum of 8 MB) on board(72 Pins SIMM x 4), and BIOS auto DRAM/EDO RAM configuration.(Refer to Chapter 2-3 System Memory Configuration)
- Supports both Fast Page DRAM or **EDO** DRAM SIMM. Optional DRAM Parity or Error Checking and Correction (ECC) with 72-bit Wide memory.
- Intel 82430HX PCIset chipset.
- Supports Onboard Pipelined burst synchronous and the **COAST(v2.0) or later Version** solusion L2 **Write Back** Cache. The cache memory combination could be 256KB/512KB (32KB*32 or 64KB*32 SRAM respectively).
- Support four 16 bits ISA slots, four 32 bits PCI slots, and provides two independent high performance PCI IDE interface capable of supporting **PIO Mode 3 and Mode 4** devices. The **P55-TH** supports four PCI Bus Masters and a jumperless PCI INT# control scheme which reduces configuration confusion when plug in PCI I/O controller card(s).
- Supports **ATAPI** (e.g. **CD-ROM**) devices on both IDE interface.
- Supports 1 floppy port(up to 2.88 MB), 1 parallel port (EPP,ECP port), and 2 serial port (16550 Fast UART compatible).
- Supports a **PS/2** style mouse and standard AT style keyboard connectors.
- Support Award Plug & Play BIOS . The BIOS is stored in Flash EPROM form. It provides better upgradeability for the system.
- Supports CPU Hardware sleep and SMM (System Management Mode).
- **P55-TH** utilizes Lithium battery which provides environmental protection and longer life time.

P55-TH Layout

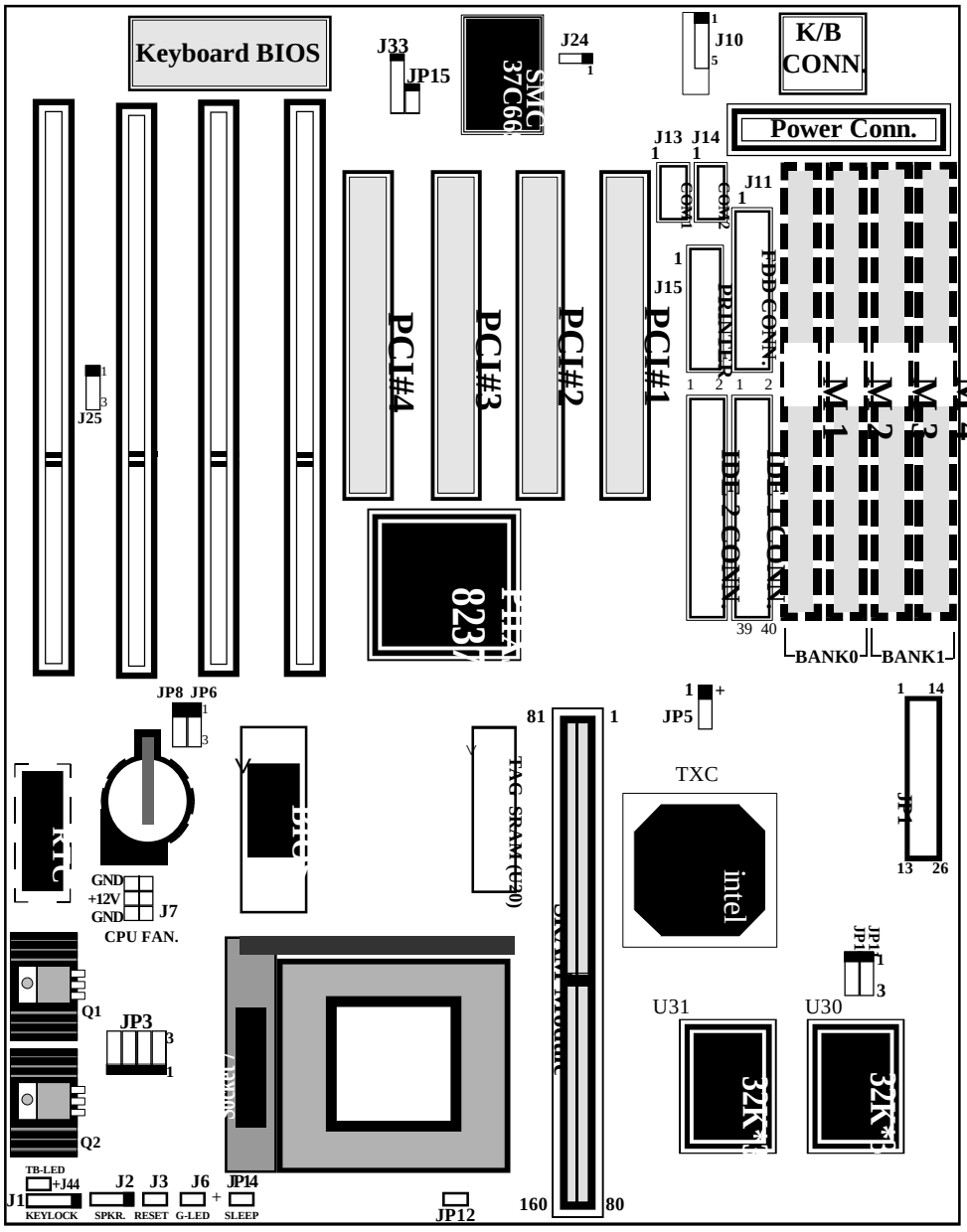


Figure 1-1

Chapter 2
Hardware design

2-1 Motherboard Layout

The P55-TH is designed with Intel 82430HX PCIset chipset which is developed by INTEL Corporation to fully support Intel Pentium® processor PCI/ISA system. The Intel 82430HX PCIset chipset prpovides increased integration and improved performance designs. The 82430HX chipset provides an integrated IDE controller with two high performance IDE interfaces for up to four IDE devices (hard devices, CD-ROM device, etc). The SMC (STANDARD MICROSYSTEMS CORPORATION) FDC37C669 Super I/O controller provides the standard PC I/O function: floppy interface (up to 2.88 MB), two 16 Byte FIFO serial ports and EPP/ECP capable parallel port. The **P55-TH** layout is shown in previous page (left page) for user's reference. **Care must be taken** when inserting memory modules, inserting Intel **P54C/P54CT/P54CST** processor, or even plugging PCI card into associated slots to avoid damaging any circuits or sockets on board. A cooling fan is strongly recommended when installing P54C/P54CT/P54CST processor due to possible overheat.

The P55-TH supports minimum of 8MB of System Memory and maximum of 512MB while L2 Cache can be 256KB/512KB synchronous SRAM Onboard with the **COASt 2.0 or later Version**"**C**ache-**O**n-**A**-**ST**ick" solution to increase system performance.(refer to **Page 2-5 Cache Memory Configuration** for the details.)

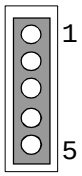
The P55-TH support standard Fast Page or EDO (Extended Data Out or Hyper Page Mode) DRAM. The EDO DRAM is designed to improve the DRAM read performance (When L2 Cache is installed). **The P55-TH** provides four 72-pins SIMM sites for memory expansion. The socket support 1M x 32(4MB), 2M x 32(8MB), 4M x 32(16MB), 8M x 32(32MB) and 16MB x 32(64MB) single-sided or double-sided SIMM modules. The memory timing requires 70 nS Fast page devices or 60 nS EDO DRAM. Memory parity generation and checking or ECC (Error Checking and Correction) are supported. (DRAM Modules may be parity[x 72] or non-parity[x 64] or ECC[x72]. The BIOS will automaticlly detct which DRAM has installed in SIMM sites.

The P55-TH supports **Onboard two PCI IDE** connectors, and detects IDE harddisk type by BIOS utility automatic.

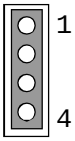
The P55-TH supports Award Plug & Play BIOS for the ISA and PCI cards. The BIOS can be located in Flash EPROM. The advantage of having Flash EPROM is much easier to replace BIOS code if necessary.

2-2 Connectors and Jumpers

This section describes all of the connectors and jumpers equipped in the motherboard. Please refer to **Figure 1-1** for actual location of each connector and jumper.

J1 

KeyLock - Keyboard lock switch & Power LED connector.
1.Power LED(+)
2.N/C
3.GND
4.Keylock
5.GND

J2 

Speaker - connect to the system's speaker for beeping.
1. Speaker
2. N/C
3. GND
4. GND

J3 

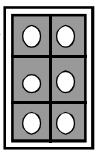
Reset - Close to restart system.

J44 

Turbo LED indicator - LED ON when higher speed is selected by a BIOS hot key<CTRL><ALT><+>and also brings system to a slower speed while a hot key<CTRL><ALT><->.

J6 

Power Saving LED indicator(Green-LED) LED ON when system is in any Saving mode.

J7 

The Power supply of the CPU cooling fan
1,2 GND
3,4 +12v
5,6 GND

JP5 

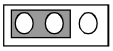
IDE LED indicator - LED ON when Onboard PCI IDE Harddisks activites.

JP14 

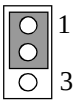
Sleep/Resume switch : Close to enter sleep mode.
A keystrobe or mouse movement (the mouse driver exists). The systemwill instantly "wake up".

J24 

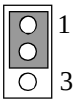
Onboard SMC's chip select :
Open: Normal operation.(Default)
Close: Disable the Onboard SMC chip.

JP15 

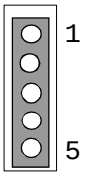
Keyboard Operation Clock Select :
1-2 The clock rate is depend on the system AT CLOCK(J25).(Default)
2-3 The clock rate is 12MHz.

JP6 

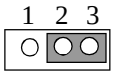
EPROM BIOS Select :
1-2 for 5V Flash EPROM.
2-3 for 12V Flash EPROM.
Note: The JP6 setting is depand on which EPROM type was attach board.

JP8 

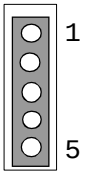
BIOS FLASH MODE:
1-2 for normal flash mode. (Default)
2-3 for 12V Flash EPROM to do BOOT BLOCK Flash Mode.

J10 

PS/2 MOUSE CONNECTOR:
1.RED wire
2.BLUE wire
3.GREEN wire
4.NC

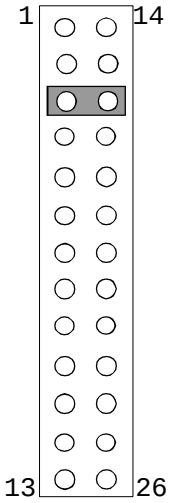
J25 

System AT BUS CLOCK Select:
1-2 ATCLK is devided **PCICLK*** by 3.
2-3 ATCLK is devided **PCICLK*** by 4.(Default)
*** PCICLK =** System Clock / 2
If system is operating at 66/100 MHz, than **PCICLK** is 33MHz.

J33 

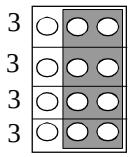
IrDA/ASK IR CONNECTOR:
1.VCC
2.NC
3.IRRX
4.GND
5.IRTX

JP1:**CPU Clock Rate Select.**



	Pentium® Processor	Cyrix 6x86 Processor
1-14	50/75MHz	
2-15	60/90MHz	
3-16	66/100MHz	(Default)
4-17	60/120MHz	6x86-P150+(120MHz)
5-18	66/133MHz	6x86-P166+(133MHz)
6-19	60/150MHz	
7-20	66/166MHz	
8-21	60/180MHz	
9-22	66/200MHz	
10-23		6x86-P120+(100MHz)
11-24		
12-25		
13-26		

JP3



CPU Install:

1-2: for Intel Pentium® Processor (P54C/P54CS/ P54CT/P54CTB) and Cyrix 6x86(Note)

2-3: Intel Pentium® Processor P55C.

Note: When Cyrix's CPU installed on board. Please take special care on the CPU cooling fan to avoid Cyrix CPU overheat problem.

2-3 System Memory Configuration

The **P55-TH** supports different type of settings for the system memory. There is no jumper nor connector needed for memory configuration. Following figures provides all possible memory cominations.

M1,M2(BANK 0)	M3,M4(BANK 1)	Total Size
1M x 32 (4 MB)	Empty	8MB
1M x 32 (4 MB)	1M x 32 (4 MB)	16MB
1M x 32 (4 MB)	2M x 32 (8 MB)	24MB
1M x 32 (4 MB)	4M x 32 (16 MB)	40MB
1M x 32 (4 MB)	8M x 32 (32 MB)	72MB
2M x 32 (8 MB)	Empty	16MB
2M x 32 (8 MB)	1M x 32 (4 MB)	24MB
2M x 32 (8 MB)	2M x 32 (8 MB)	32MB
2M x 32 (8 MB)	4M x 32 (16 MB)	48MB
2M x 32 (8 MB)	8M x 32 (32 MB)	80MB
4M x 32 (16 MB)	Empty	32MB
4M x 32 (16 MB)	1M x 32 (4 MB)	40MB
4M x 32 (16 MB)	2M x 32 (8 MB)	48MB
4M x 32 (16 MB)	4M x 32 (16 MB)	64MB
4M x 32 (16 MB)	8M x 32 (32 MB)	96MB
8M x 32 (32 MB)	Empty	64MB
8M x 32 (32 MB)	1M x 32 (4 MB)	72MB
8M x 32 (32 MB)	2M x 32 (8 MB)	80MB
8M x 32 (32 MB)	4M x 32 (16 MB)	96MB
8M x 32 (32 MB)	8M x 32 (32 MB)	128MB
16M x 32 (64MB)-S	16M x 32 (64MB)-S	256MB
16M x 32 (64MB)-D	16M x 32 (64MB)-D	512MB

NOTE : 1. P55-TH support both Fast Page DRAM or EDO DRAM SIMMs, but they cannot be mixed within the same memory bank.

2. SIMMs may be parrity (x 72) or non parity (x 64) or ECC(x 72).

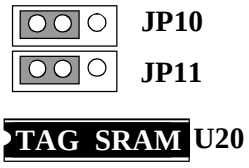
3. The 70nS Fast Page Mode or 60ns EDO DRAM is necessary.

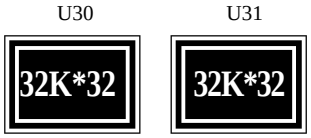
4. "BANK"=64 Bit=M1, M2 = M3, M4

5. "-S" denotes signal-sided SIMM's, "-D" denotes double-sided SIMM's.

2-4 Cache Memory Configuration

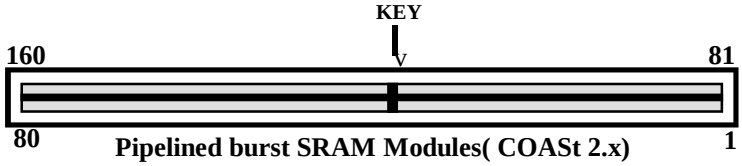
The second level (L2) of cache is installed in the motherboard to increase the system performance. The **P55-TH** supports different type of combinations for the cache installation. The **COASt 2.0 or later Version**(**C**ache-**O**n-**A-ST**ick. **The cache modules has a TAG SRAM.**) solution provides Onboard flexibility, allowing Onboard and modules to accommodate 256KB/512KB piplined burst synchronous SRAM. Jumper JP10 and JP11 settings is used to Onboard's synchronous SRAM for differential such combinations. Please refer to following configurations for the details.





DATA SRAM

SYN.CACHE Size	On Board (U30,U31)	On Module (SRM1)	Jumper Setting	
			JP10	JP11
256KB	256KB	None	1-2	1-2
256KB	None	256KB	1-2	2-3
512KB	256KB	256KB (Extended)	1-2	1-2
512KB	512KB	None	2-3	1-2
512KB	None	512KB	1-2	2-3



Pipelined burst SRAM Modules(COASt 2.x)

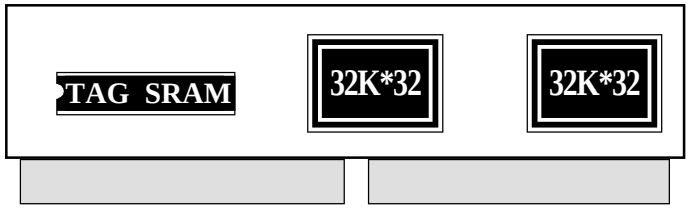


Figure 2-1 COAST MODULE

Your **P55-TH** may have come with an optinal **COAST** Module(Ref. Figure 2-1) to extend the cache size from 256KB to 512KB (When your **P55-TH** had mounted 256 KB (32K*32x2 synchronous SRAM)).

Note :

When you have a cache module to plug into a 160 pin daul readout connector. You must made sure that cache modules is followed Intel COASt 2.0 or later version. Please contact the modules supplier to avoid not working properly or damaging and modules circuits.

2-5 Integrated PCI Bridge

The **P55-TH** utilizes **Intel's 82430HX PCIset** chipset to support Intel Pentium® P54C/P54CTB Processor PCI/ISA system. The Intel 82430HX PCIset chipset consists of the 82439HX **(324 Pin BGA Packing Chipset)** system controller (TXC), and one 82371SB PCI ISA/IDE Accelerator (PIIX3) bridge chip. It provides an interface which translates CPU cycle into PCI bus cycle, and PCI burst read/write capability. In addition, it provides high performance PCI arbitor to support four PCI Masters, Rotating Priority Mechanism, and Hidden Arbitration Scheme Minimizes Arbitration Overhead.

There are four interrupts in each PCI slot : INTA#, INTB#, INTC#, and INTD#. Since the **P55-TH** adapts the PCI auto-configuration with the system BIOS Setup utility. When the system is turned on after adding a PCI add-in card, the BIOS automatically configure interrupts, DMA channels, I/O space, and other paramaters. You do not have to configures jumpers or worry potential resource conflicts. Because PCI cards use the same interrupt resource as ISA cards, you must specify the interrupt used by ISA add-in cards in the BIOS Setup utility.

If however, a "Legacy card" (such as plug paddle card and cable into the ISA slot.) is plugged in the system, modification in the **ROM SETUP UTILITY** become necessary. First, enter **PNP/PCI CONFIGURATION SETUP**utility from **ROM SETUP UTILITY** main menu to set the "**IRQ X or DMA X assigned to: legacy ISA or PCI/ISA PNP**'cards.

Second, you must be enter **CHIPSET FEATURES SETUP UTILITY**from **ROM SETUP UTILITY** main menu and set the "**Onboard Primary PCI IDE: Disabled** and **Onboard Secondary PCI IDE: Disabled**." When you plugged the PCI/ISA IDE card into the system. You will **Disabled Onboard Primary and Secondary PCI IDE** from **CHIPSET FEATURES SETUP UTILITY**too.

Some "Legacy card" (no paddle card and cable.) you can set the system interrupt request (IRQ) on the "Legacy card" (refer to user's manual of the card) to a proper system IRQ level (in general, card's Primary assigned to INTA and Secondary assigned to INTB). If the card is plugged into slot 1(marked PCI#1), you can not use second slot (marked PCI#2) because the Secondary INT signal takes INTB from the slot (refer to Page 3-12 for circuit diagram). The user then enter **PNP/PCI CONFIGURATION SETUP** utility from **ROM SETUP UTILITY** main menu and set the "**IRQ X or DMA X assigned to : Legacy ISA or PCI/ISA PNP**"(depend on which IRQ X or DMA X was used to Legacy card that is plugged into ISA or PCI slot.

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CHAPTER 3
AWARD BIOS SETUP

Award's ROM BIOS provides a built-in Setup program which allows user modify the basic system configuration and hardware parameters. The modified data will be stored in a battery-backed CMOS RAM so data will be retained even when the power is turned off. In general, the information saved in the CMOS RAM stay unchanged unless there is configuration change in the system, such as hard drive replacement or new equipment is installed.

It is possible that CMOS had a battery failure which cause data lose in CMOS_RAM. If so, re_enter system configuration parameters become necessary.

To enter Setup Propgram

Power on the computer and press <**Del**> key immediately will bring you into BIOS **CMOS SETUP UTILITY**.

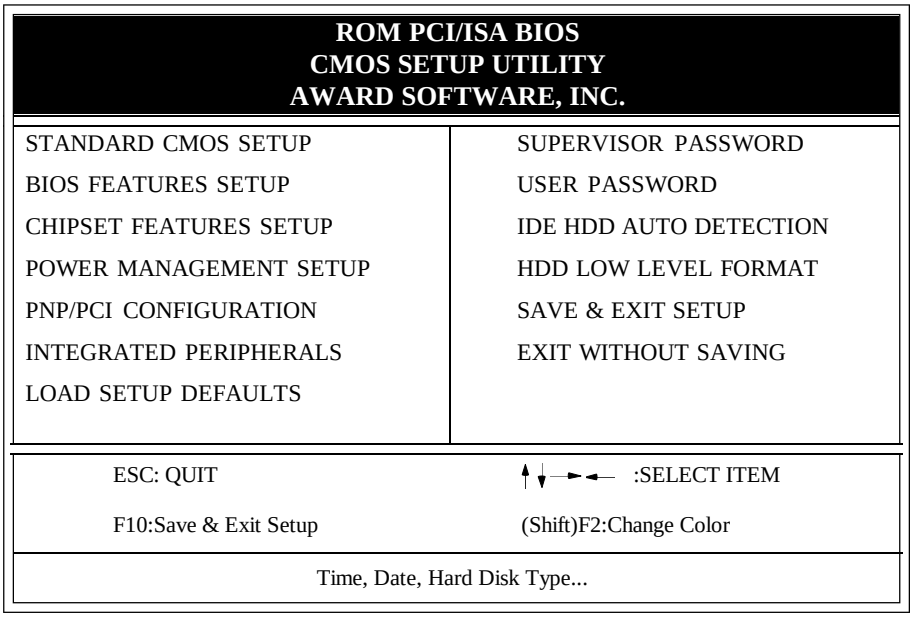


Figure 3-1 CMOS SETUP UTILITY

The menu displays all the major selection items and allow user to select any one of shown item. The selection is made by moving cursor (press any direction key) to the item and press 'Enter' key. An on_line help message is displayed at the bottom of the screen as cursor is moving to various items which provides user better understanding of each function. When a selection is made, the menu of selected item will appear so the user can modify associated configuration parameters.

3-1 STANDARD CMOS SETUP

Choose "**STANDARD CMOS SETUP**" in the **CMOS SETUP UTILITY** Menu (Fig.3-1). The **STANDARD CMOS SETUP** allows user to configure system setting such as current date and time, type of hard disk drive installed in the system, floppy drive type, and the type of display monitor. Memory size is auto_detected by the BIOS and displayed for your reference. When a field is highlighted (direction keys to move cursor and <Enter> key to select), the entries in the field will be changed by pressing <PgDn> or <PgUp> keys or user can enter new data directly from the keyboard.

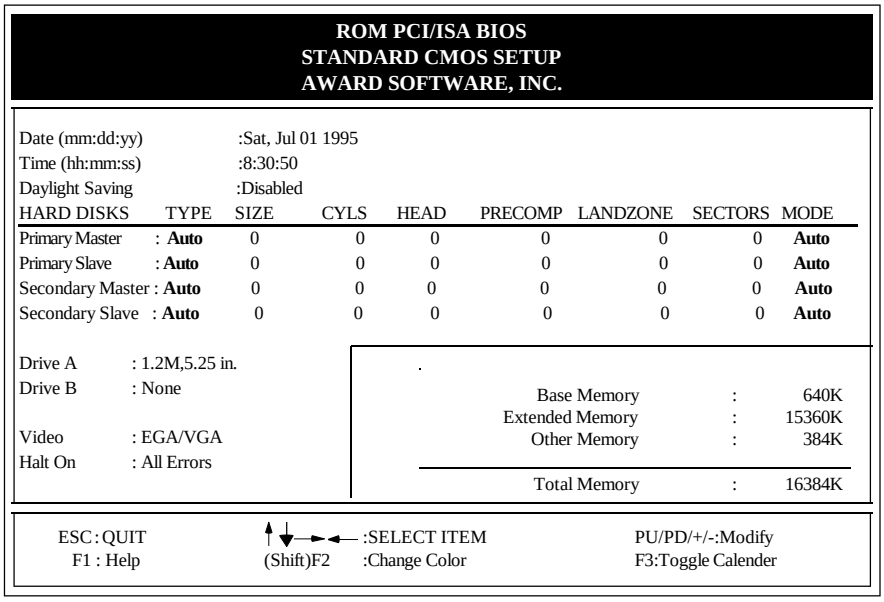


Figure 3-2 STANDARD CMOS SETUP

NOTE: If hard disk Primary Master/Slave and Secondary Master/Slave were used Auto, than the hard disk size and model will be auto-detect on display during POST.

NOTE: The "**Halt On :**" field is to determine when to halt the system by the BIOS if error occurred during **POST**.

3-2 BIOS FEATURES SETUP

Select the "**BIOS FEATURES SETUP**" option in the **CMOS SETUP UTILITY** menu allows user to change system related parameters in the displayed menu. This menu shows all of the manufacturer's default values of P55-TH. Again, user can move the cursor by pressing direction keys and <PgDn> or <PgUp> keys to modify the parameters. Pressing [F1] key to display help message of the selected item.

This setup program also provide 2 convinent ways to load the default parameter data from BIOS[F6] or CMOS[F7] area if shown data is corrupted. This provide the system a capability to recover from any possible error.

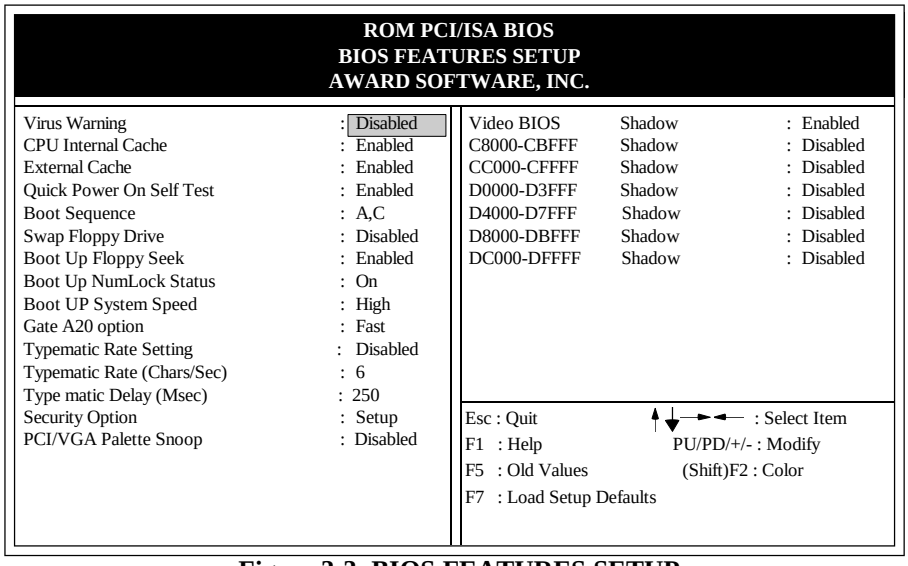


Figure 3-3 BIOS FEATURES SETUP

Note: The **Security Option** contians "**setup**" and "**system**". The "**setup**" indicates that the password setting is for CMOS only while the "**system**" indicates the password setting is for both CMOS and system boot up procedure.

- **Virus Warning:** This category flashes on the screen. During and after the system boots up, any attempt to write to the boot sector or partition table of the hard disk drive will halt the system and the following error message will appear, in the mean time, you can run an anti-virus program to locate the problem. Default value is Disabled

  ***Enabled* :** Activates automatically when th e system boots up causing a warning message to appear when anything attempts to access the boot sector or hard disk partition table.

  ***Disabled*:** No warning message to appear when anything attempts to access the boot sector or hard disk partition table.

- **CPU Internal Cache / External Cache:**These two categories speed up memory access. However, it depends on CPU/chipset design. The default value is Enable. If your CPU without Internal Cache then this item "CPU Internal Cache" will not be show.

  ***Enabled*:** Enable cache.

  ***Disable* :** Disable cache.

- **Quick Power On Self Test:** This category speeds up Power On Self Test (POST) after you power on the computer. If it is set to Enable, BIOS will shorten or skip some check items during POST.
  Enabled **:** Enable quick POST.
  Disabled**:** Normal POST.

- **Boot Sequence:** This category determines which drive computer searches first for the DOS(Disk Operating System). Default value is A,C.
  A,C **:**System will first search for floppy disk drive then hard disk drive.
  C,A **:**System will first search for hard disk drive then floppy disk drive.
  CDROM,C,A: System will first search for the CDROM driver (If the CDROM has a bootable CD title.) and second search hard disk driver then flopp disk driver.
  C,CDROM,A: System will first search for the hard disk driver and second search the CDROM driver (If the CDROM has a bootable CD title.) then floppy disk driver.

- **Swap Floppy Drive:** The swap floppy drive. Default value is Disabled.
  Enabled **:** Floppy A & B will be swapped under the DOS.
  Disabled**:** Floppy A & B will be not swap.

- **Boot Up Floppy Seek:** During POST,BIOS will determine if the floppy disk drive installed is 40 or 80 tracks. 360K type is 40 tracks while 760K, 1.2M and 1.44M are all 80 tracks. The default value is Enabled.
  Enabled **:** BIOS searches for floppy disk drive to determine if it is 40 or 80 tracks, Note that BIOS can not tell from 720K, 1.2M or 1.44M drive type as they are all 80 tracks.
  Disabled**:** BIOS will not search for the type of floppy disk drive by track number. Note that there will not be any warning message if the drive installed is 360K.

- **Boot Up NumLock Status:** The default value is On.
  On **:** Keypad is number keys.
  Off **:** Keypad is arrow keys.

- **Boot UP System Speed**: It selects the default system speed, the speed that the system will run at immediately after power up.
  High: Set the speed to high.
  Low : Set the speed to low.

- **Gate A20 Option:** The default value is Fast.
  Normal**:** The A20 signal is controlled by keyboard controller or chipset hardware.
  Fast **:** Default : Fast.The A20 signal is controlled by Port 92 or chipset specific method.

- **Typematic Rate Setting:** This determines the typematic rate.
  Enabled **:** Enable typematic rate and typematic delay programming.
  Disabled**:** Disable typematic rate and typematic delay programming. The system BIOS will use default value of this 2 items and the default is controlled by keyboard.

- **Typematic Rate(Chars/Sec):**

6 : 6 characters per second.	**8 : 8 characters per second.**
10: 10 characters per second.	**12: 12 characters per second.**
15: 15 characters per second.	**20: 20 characters per second.**
24: 24 characters per second.	**30: 30 characters per second.**

- **Typematic Delay(Msec):** When holding a key, the time between the first and second character displayed.
  250 : 250msec.
  500 : 500 msec.
  750 : 750 msec.
  1000: 1000 msec.

- **Security Option:** This category allows you to limit access to the system and Setup, or just to Setup. The default value is Setup.
  System**:** The system will not boot and access to Setup will be denied if the correct password is not entered at the prompt.
  Setup **:** The system will boot, but access to Setup will be denied if the incorrect password is not entered at the prompt.

- **PCI/VGA Palette Snoop:** This filed controls the ability of a primary PCI VGA controller to share a common palette(When a snoop write cycles) with an ISA video card. The default value is Disabled.
  Enabled: If an ISA card connects to a PCI VGA card via the VESA connector and that ISA card connects to VGA monitor and that ISA card uses the RAMDAC of PCI card.
  Disabled: Disabled the VGA card Palette snoop function.

- **Video BIOS Shadow:** It determines whether video BIOS will be copied to RAM, however, it is optional from chipset design. Video Shadow will increase the video speed.
  Enabled **:** Video shadow is enabled.
  Disabled**:** Video shadow is disabled.

- **C8000 - CBFFF Shadow :**
  CC000 - CFFFF Shadow:
  D0000 - D3FFF Shadow:
  D4000 - D7FFF Shadow:
  D8000 - DBFFF Shadow:
  DC000 - DFFFF Shadow:

  These categories determine whether optional ROM will be copied to RAM by 16K byte or 32K byte per/unit and the size depends on chipset.
  ***Enabled* :** Optional shadow is enabled.
  ***Disabled*:** Optional shadow is disabled.

3-3 CHIPSET FEATURES SETUP

Choose the "**CHIPSET FEATURES SETUP**" in the **CMOS SETUP UTILITY** menu to display following menu.

ROM PCI/ISA BIOS
CHIPSET FEATURES SETUP
AWARD SOFTWARE, INC.

Auto Configuration	: Enabled	Single Bit Error Report	:Enabled
DRAM Timing	:70 ns	L2 Cache Cacheable Size	: 64MB
DAM RAS# Precharge Time	:4	Chipset NA# Asserted	: Enabled
DAM R/W Leadoff Timing	7/6		
Fast RAS# to CAS# Delay	: 3		
DAM Read Burst Timing	: x333		
DRAM Write Burst Timing	: x333		
Turbo Read Leadoff	: Disabled		
DRAM Speculative Leadoff	: Enabled		
Turn-Around Insertion	: Disabled		
System BIOS Cacheable	: Disabled		
Video BIOS Cacheable	: Enabled		
8 Bit I/O Recovery Time	: 1		
16 Bit I/O Recovery Time	: 1		
Memory Hole At 15M-16M	: Disabled	ESC: Quit	:select Item
Peer Concurrency	: Enabled	F1 : Help PU/PD/+/-	:Modify
Chipset Special Features	: Enabled	F5 : Old Values (Shift)F2	:Color
DRAM ECC/PARITY Select	: ECC	F7 : Load Setup Defaults	
Memory Parity/ECC Check	: Auto		

Figure 3-4 CHIPSET FEATURES SETUP

- **Auto Configuration:** This Category allows you to setting the DRAM timing. The default value is Enabled. When disabled this field. You can select the different DRAM's timing that supports by chipset below item.

Note: When you insert a slower memery modules in the system and set a faster timing. Maybe have the system hang up.

- **DRAM Timing:** The default value is 70ns.
  ***60ns* :** 2 (faster) Burst Wait State, for 60~70ns Fast Page Mode/EDO DRAM.
  ***70ns* :** 3 (slower) Burst Wait State, for 70ns Fast Page Mode/EDO DRAM.

- **Video BIOS Cacheable:** The default value is Enabled.
  ***Enabled* :** This field Enabled the Video BIOS Cacheable to speed up the VGA Performance.
  ***Disabled*:** Disabled the Video BIOS Cacheable function.

- **8/16 Bit I/O Recovery Time:** The default value is 1.
  ***8 Bit I/O Recovery Time*:** This field defines the recovery time from 1 to 8 for 8-bit I/O.
  ***16 Bit I/O Recovery Time*:** To define the recovery time from 1 to 4 for 16-bit I/O.

- **Memory Hole at 15M-16M:** The default value is Disabled.
  ***Disabled*:** Normal Setting.
  Enabled : This field enableds the main memory (15~16MB) remap to ISA BUS.

- **Peer Concurrency:**The default value is Enabled.

- **DRAM ECC/PARITY Select:**The default value is ECC. This field defines the DRAM is parity or ECC properly if all DRAs are 72-bit wide. A system with a mixture of 64-bit and 72-bit wide should disable PARITY and ECC.

- **Memory Parity/ECC Check:**The default value is Auto. That will Auto detect the DRAM is none parity parity or ECC.

- **Single Bit Error Report:**The default value is Enabled. When yuou insert 72-bit wide DRAMs. The BIOS will show a warning message on display before the single-bit detected/corrected errors.

- **L2 Cache Cacheable Size:**The default value is 64MB. This board's L2 cache cacheable DRAM size were 64MB.

- **Chipset NA# Asserted:**The default value is Enabled. This is to enabled the L2 Cache's performance.

3-4 POWER MANAGEMENT SETUP

Choose the "**POWER MANAGEMENT SETUP**" in the **CMOS SETUP UTILITY** to display the following screen. This menu allows user to modify the power management parameters and IRQ signals. In general, these parameters should not be changed unless it's absolutely necessary.

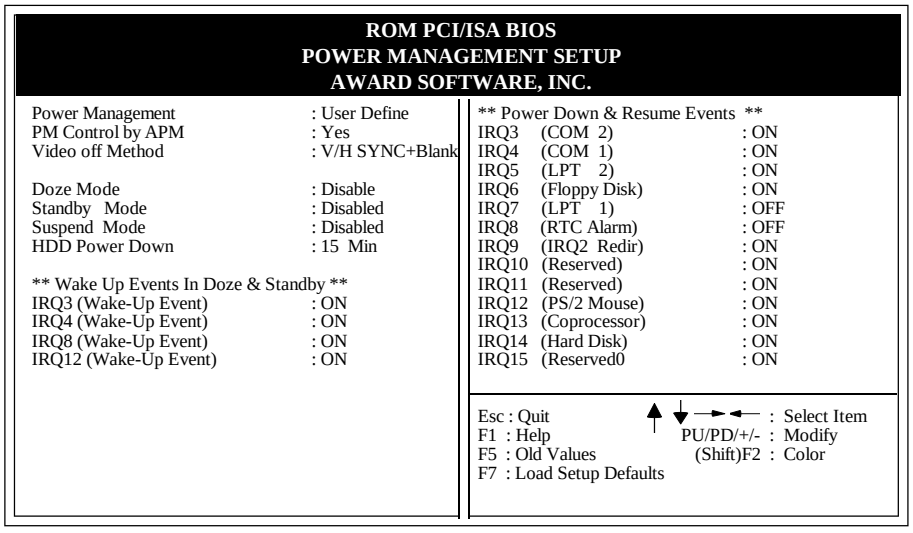


Figure 3-5 POWER MANAGEMENT SETUP

Again, user can move the cursor by pressing direction keys to the field need to be modified and press <PgDn> or <PgUp> to alter item selection. You can only change the content of **Doze Mode**, **Standby Mode**, and **Suspend Mode** when the **Power Management** is set to '**User Define**'.

3-4-1 The Description of the Power Management

A. Power Management mode selection :

Disabled : The system operates in NORMAL conditions (Non-GREEN), and and the Power Management function is disabled.

Max.saving: This mode will maximize the power saving capability.

Min.saving: This mode will minimize the power saving capability.

User define: Allow user to define timeout parameters to control power saveing timing. Refer item B shown below.

B. Timeout parameters :

HDD Standby
HDD Standby timer can be set from 1 to 15 minute(s).

System Doze
The "System Doze" mode timer starts to count when there is no "PM events" occurred. The valid timeout setting is from 1 minute up to 1 hour.

System Standby
The "Standby" mode timer starts to count when "System Doze" mode timer timed out and no "PM events" occurred. Valid range is from 1 minute up to 1 hour.

System Suspend
This function works only when the Pentium® Procssor is installed. The timer starts to count when "System Standby" mode timer timed out and no "PM Events" occurred. Valid range is from 1 minute up to 1 hour.

3-4-2 Description of the Green Functions

The P55-TH supports HDD Power Down, Doze and standby power saving functions when Intel Pentium® Processor is installed. In addition, the suspend function is supported when the JP14 (sleep ref. Figure1-1) be close to enter the green function. The detail description of these functions are provided in next page.

HDD Standby Mode
When system stop reading or wiriting HDD, the timer starts to count. The system will cut off the HDD power when timer ran out of time. The system will not resume operation until either a read from or a wirte to HDD command is executed again.

Doze Mode
The system hardware will drop down CPU clock from nomal working speed when Doze mode timeout occurred.

Standby Mode
When the system standby mode timer ran out, it will enter the standby mode and retain CPU at slow working speed. The screen will be blanked out.

Suspend Mode
When the system suspend timer time out, the system will enter the suspend mode and the chipset will stop CPU clock immediately. The power consunption in Suspend Mode is lower than in standby mode. The screen is also blanked out.

PM Events:
AWARD BIOS defines 15 PM Events in the power management mode (Doze, standby & suspend). The user can initial any PM Events to be "Enable" or "Disable". When the system detects all of the enabled events do not have any activity, it will start the system Doze timer first if the "Power Management" isn't "Disabled". Once the system Doze timer timed out, it will process doze power saving procedure by starting the system standby timer. When the standby timer ran out and all of the "Enabled" events remains silent, the system will enter the standby mode. By now, the system will not only process the standby power saving procedures but also start the system suspend timer. When the suspend timer time out , all of the CPU clock will be stopped by dropping system clock down to zero and remains this way until any one of the "Enabled" event occurred.

3-5 PNP/PCI CONFIGURATION

The PNP/PCI configuration program is for the user to modify the PCI/ISA IRQ signals when various PCI/ISA cards are inserted in the PCI or ISA slots.

WARNING : Any misplacing IRQ could cause system can't pick out the rescouces.

ROM PCI/ISA BIOS
PNP/PCI CONFIGURATION
AWARD SOFTWARE, INC.

Resources Controlled By		: Manual	PCI IRQ Actived By		: Level
Reset Configuration Data		: Disabled	PCI IDE IRQ Map To		: PCI-AUTO
			Primary	IDE INT#	: A
IRQ-3	assigned to	: Legacy ISA	Secondary	IDE INT#	: B
IRQ-4	assigned to	: Legacy ISA			
IRQ-5	assigned to	: PCI/ISA PnP			
IRQ-7	assigned to	: Legacy ISA			
IRQ-9	assigned to	: PCI/ISA PnP			
IRQ-10	assigned to	: PCI/ISA PnP			
IRQ-11	assigned to	: PCI/ISA PnP			
IRQ-12	assigned to	: PCI/ISA PnP			
IRQ-14	assigned to	: Legacy ISA			
IRQ-15	assigned to	: Legacy ISA			
DMA-0	assigned to	: PCI/ISA PnP	ESC : Quit		: Select Item
DMA-1	assigned to	: PCI/ISA PnP	F1 : Help	PU/PD/+/-	: Modify
DMA-3	assigned to	: PCI/ISA PnP	F5 : No Change	(Shift) F2	: Color
DMA-5	assigned to	: PCI/ISA PnP	F7 : Load Setup Defaults		
DMA-6	assigned to	: PCI/ISA PnP			
DMA-7	assigned to	: PCI/ISA PnP			

Figure 3-6 PCI CONFIGURATION SETUP

- **Resource Controlled By:** The default value is Manual.
  Manual: The field defines that the PNP Card's resource controlled by manual. You can set which IRQ-X and DMA-X assigned to PCI/ISA PNP or Legacy ISA Cards.
  Auto: If your ISA card or PCI card are all PNP cards. To set this field Auto. The bios will be assigned the resource automatically.

- **Reset Configuration Data:** The default value is Disabled
  Disabled: Normal Setting
  Enabled: If you had plugged some Legacuy cards in the system and there were record into ESCD(Extended System Configuration Data). You can set this field to Enabled and to clear ESCD one time. When some Legacy cards were removed.

- **PCI IDE IRQ Map To:** The default value is PCI-AUTO
  When you have true PCI card(s) plugged into the system, you will not need to change any thing here in the **SETUP** program. However, if you do not know whether you have true PCI card or not, please refer to your PCI card user's manual for the details.

  When you have a Legacy card (describbed in section 2-5) to be plugged into the system,a proper setting is extremely important or it may cause the system hang up. The diagram shown below tells you how the Rotating Priority Mechanism is designed.

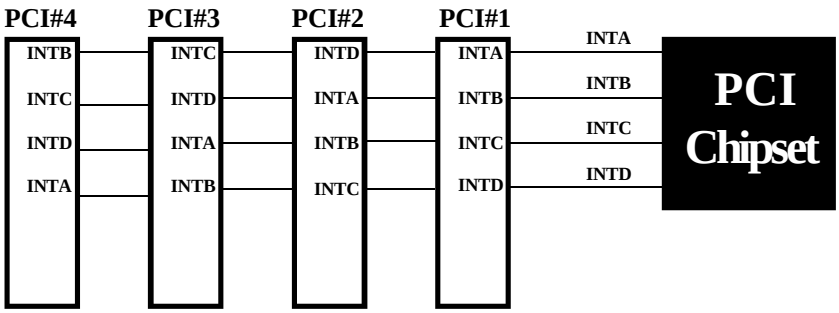
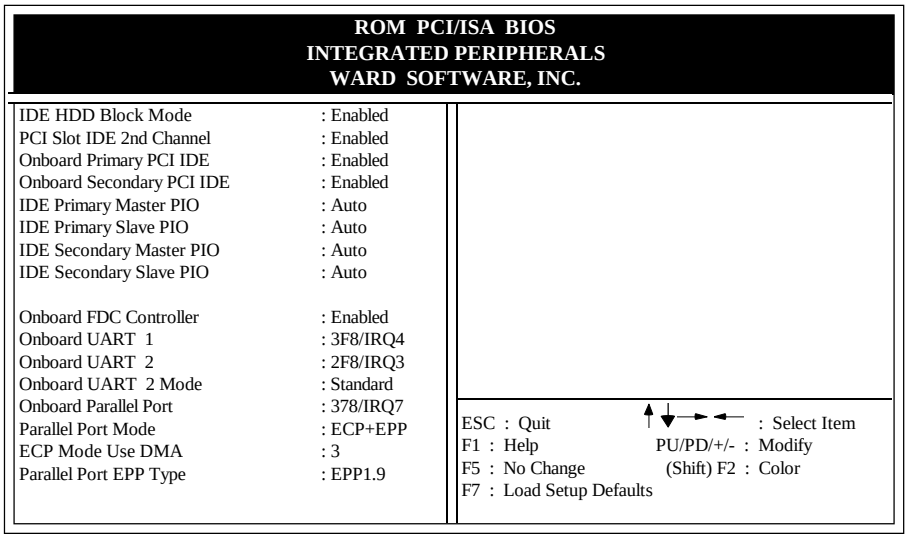


Figure 3-7 The Combination of PCI INT# lines

3-6 INTEGATED PERIPHERALS



Note: If you don't use the Onboard IDE connector, than use On-card (PCI or ISA card) IDE connector. You will set Onboard Primary PCI IDE: Disabled and Onboard Secondary PCI IDE: Disabled from CHIPSET FEATURES SETUP UTILITY.
The Onboard PCI IDE cable should be equal to or less than 18 inches (45 cm.).

- **IDE HDD Block Mode:** The default value is Enabled.
  ***Enabled* :** Enabled IDE HDD Block Mode. The HDD transfer rate is better than Disable.
  ***Disabled*:** Disable IDE HDD Block Mode.

- **PCI Slot IDE 2nd Channel:** The default value is Enabled.
  ***Enabled* :** Enable secondary IDE port and BIOS will assign IRQ15 for this port.
  ***Disabled* :** Disable secondary IDE port and IRQ15 is available for other device.

- **Onboard Primary PCI IDE:** The default value is Enabled.
  ***Enabled* :** Enable Onboard 1st channel IDE port.
  ***Disabled* :** Disable Onboard 1st channel IDE port. When use On-card (PCI or ISA card) IDE connector.

- **Onboard Secondary PCI IDE:** The default value is Enabled.
  ***Enabled* :** Enable Onboard 2nd channel IDE port.
  ***Disabled* :** Disable Onboard 2nd channel IDE port When use On-card (PCI or ISA card) IDE connector.

- **IDE Primary Master PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Primary Master PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Primary Slave PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Primary Slave PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Secondary Master PIO:** The default value is Auto.
  Auto **:** BIOS will automatically detect the Onboard Secondary Master PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **IDE Secondary Slave PIO:** The default value is
  Auto **:** BIOS will automatically detect the Onboard Secondary Slave PCI IDE HDD Accessing mode.
  Mode0~4 **:** Manually set the IDE Accessing mode.

- **Onboard FDC Controller:** The default value Enabled.
  Enabled **:** Enable the Onboard SMC CHIP's floppy drive interface controller.
  Disabled **:** Disable the Onboard SMC CHIP's floppy drive interface controller. When use On-card ISA FDC's controller.

- **Onboard UART 1:** This fields allow the user to sellect the serial port. The default value is 3F8H/IRQ4.
  COM1**:** Enable Onboard Serial port 1 and address is 3F8H/IRQ4.
  COM2**:** Enable Onboard Serial port 1 and address is 2F8H/IRQ3.
  COM3**:** Enable Onboard Serial port 1 and address is 3E8H/IRQ4.
  COM4**:** Enable Onboard Serial port 1 and address is 2E8H/IRQ3.
  Disabled**:** Disable Onboard SMC CHIP's Serial port 1.

- **Onboard UART 2:** This fields allow the user to sellect the serial port. The default value is 2F8H/IRQ3.
  COM1**:** Enable Onboard Serial port 2 and address is 3F8H/IRQ4.
  COM2**:** Enable Onboard Serial port 2 and address is 2F8H/IRQ3.
  COM3**:** Enable Onboard Serial port 2 and address is 3E8H/IRQ4.
  COM4**:** Enable Onboard Serial port 2 and address is 2E8H/IRQ3.
  Disabled**:** Disable Onboard SMC CHIP's Serial port 2.

- **Onboard UART 2 Mode:** The default value is standard. This fields allow the User to select the COM2 port that can supports a serial Infrared Interface.
  standard: Support a Serial Infrared Interface IrDA.
  HPSIR: Support a HP Serial Infrared Interface formats.
  ASKIR: Support a Sharp Serial Infrared Interface formats.

- **Onboard Parallel port:** This fields allow the user to sellect the LPT port. The default value is 378H/IRQ7.
  378H **:** Enable Onboard LPT port and address is 378H and IRQ7
  278H **:** Enable Onboard LPT port and address is 278H and IRQ5.
  3BCH **:** Enable Onboard LPT port and address is 3BCH and IRQ7.
  Disabled **:** Disable Onboard SMC CHIP's LPT port.

  NOTE**: Parallel Port address is 378H/3BCH that selects the rounting of IRQ7 for LPT1. Parallel Port address is 278H that selects the rounting of IRQ5 for LPT1.**

- **Parallel port Mode:** This fields allow the user to sellect the parallel port mode. The default value is ECP+EPP.
  Normal **:** Standard mode. IBM PC/AT Compatible bidirectional parallel port.
  EPP **:** Enhanced Parallel Port mode.
  ECP **:** Extended Capabilities Port mode.
  EPP+ECP **:** ECP Mode & EPP Mode.

  ECP Mode USE DMA: This fields allow the user to sellect DMA1 or DMA3 for the ECP mode. The default value is DMA3.
  DMA1 **:** The filed selects the rounting of DMA1 for the ECP mode.
  DMA3 **:** The filed selects the rounting of DMA3 for the ECP mode.

3-7 LOAD SETUP DEFAULTS

The "**LOAD SETUP DEFAULTS**" function loads the system default data directly from ROM and initialize associated hardware properly. This function will be necessary only when the system CMOS data is corrupted.

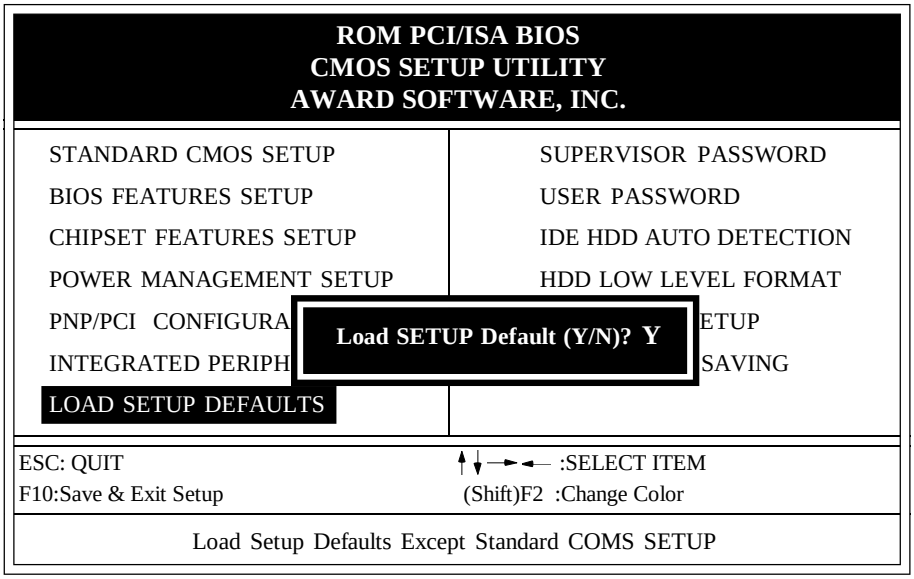


Figure 3-8 LOAD SETUP DEFAULT

3-8 CHANGE SUPERVISOR or USER PASSWORD

To change the password, choose the "**SUPERVISOR PASSWORD or USER PASSWORD** " option from the **CMOS SETUP UTILITY** menu and press [Enter].

NOTE : Either "**Setup**" or "**System**" must be selected in the "**Security Option**" of the **BIOS FEATURES SETUP** menu (Refer to Figure 3-3 for the details).

1. If CMOS is corrupted or the option was not used, a default password stored in the ROM will be used. The screen will display the following message:

   Enter Password:

   Press the [Enter] key to continue after proper password is given.

2. If CMOS is corrupted or the option was used earlier and the user wish to change default password, the **SETUP UTILITY** will display a message and ask for a confirmation.

   Confirm Password:

3. After pressing the [Enter] key (ROM password if the option was not used) or current password (user-defined password), the user can change the password and store new one in CMOS RAM. A maximum of 8 characters can be entered.

3-9 IDE HDD AUTO DETECTION

The "IDE HDD AUTO DETECTION" utility is a very useful tool especially when you do not know which kind of hard disk type you are using. You can use this utility to detect the correct disk type installed in the system automatically. **But now** you can set **HARD DISK TYPE** to **Auto** in the **STANDARD CMOS SETUP**. You don't need the "IDE HDD AUTO DETECTION" utility. The BIOS will Auto-detect the hard disk size and model on display during POST.

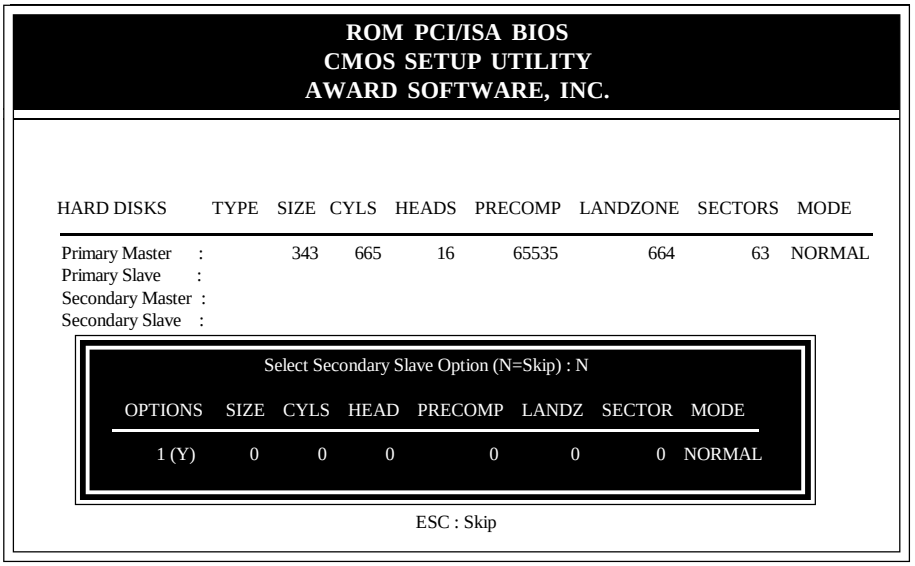


Figure 3-9 IDE HDD AUTO DETECTION

NOTE: HDD Modes

The Award BIOS supports 3 HDD modes : NORMAL, LBA & LARGE

NORMAL mode

Generic access mode in which neither the BIOS nor the IDE controller will make any transformations during accessing.

The maximum nunber of cylinders, head & sectors for NORMAL mode are. 1024, 16 & 63.

	no. Cyclinder	(1024)
x	no. Head	(16)
x	no. Sector	(63)
x	no. per sector	(512)
		528 Megabytes

If user set his HDD to NORMAL mode, the maximum accessible HDD size will be 528 Megabytes even though its physical size may be greater than that!

LBA (Logical Block Addressing) mode

A new HDD accessing method to overcome the 528 Megabyte bottleneck. The number of cylinders, heads & sectors shown in setup may not be the number physically contained in the HDD.

During HDD accessing, the IDE controller will transform the logical address described by sector, head & cylinder into its own physical address inside the HDD.

The maximum HDD size supported by LBA mode is 8.4 Gigabytes which is obtained by the following formula:

	no. Cyclinder	(1024)
x	no. Head	(255)
x	no. Sector	(63)
x	bytes per secttor	(512)
	8.4 Gigabytes	

LARGE mode

Extended HDD access mode supported by Award Software.

Some IDE HDDs contain more than 1024 cylinder without LBA support (in some cases, user do not want LBA). The Award BIOS provides another alternative to support these kinds of LARGE mode:

CYLS.	HEADS	SECTOR	MODE
1120	16	59	NORMAL
560	32	59	LARGE

BIOS tricks DOS (or other OS) that the number of cylinders is less than 1024 by dividing it by 2. At the same time, the number of heads is nultiplied by 2. Areverse transformation process will be made inside INT 12h in order to access the right HDD address the right HDD address!

Maximum HDD size:

	no. Cyclinder	(1024)
x	no. Head	(32)
x	no. Sector	(63)
x	bytes per sector	(512)
	1 Gigabytes	

Note:

To support LBA or LARGE mode of HDDs, there must be some softwares involved. All these softwares are located in the Award HDD Service Routine (1NT 13h). It may be failed to access a HDD with LBA (LARGE) mode selected if you are running under a Operating System which replaces the whole 1NT 13h.
UNIX operating systems do not support either LBA or LARGE and must utility the Standard mode. UNIX can support drives larger than 528MB.

3-10 HDD LOW LEVEL FORMAT

Interleave

Slect the interleave number of the hard disk drive you wish to perform low level format. You may select from 1 to 8. Check the documentation that came with the drive for the correct interleave number, or select 0 for utility automatic detection.

Auto scan bad track

This allows the utility to scan first then format by each track.

Start

Press<Y>to start low level format.

3-11 SAVE & EXIT SETUP

The "**SAVE & EXIT SETUP**" option will bring you back to boot up procedure with all the changes you just made which are recorded in the CMOS RAM.

3-12 EXIT WITHOUT SAVING

The "**EXIT WITHOUT SAVING**" option will bring you back to normal boot up procedure without saving any data into CMOS RAM. All of the old data in the CMOS will not be destroyed.

Chapter 4
Technical Information

4-1 I/O & MEMORY MAP

MEMORY MAP

Address Range	Size	Description
[00000-7FFFF]	512K	Conventional memory
[80000-9FBFF]	127K	Extended Conventional memory
[9FC00-9FFFF]	1K	Extended BIOS data area if PS/2 mouse is installed
[A0000-C7FFF]	160K	Available for Hi DOS memory
[C8000-DFFFF]	96K	Available for Hi DOS memory and adapter ROMs
[E0000-EEFFF]	60K	Available for UMB
[EF000-EFFFF]	4K	Video service routine for Monochrome & CGA adaptor
[F0000-F7FFF]	32K	BIOS CMOS setup utility
[F8000-FCFFF]	20K	BIOS runtime service routine (2)
[FD000-FDFFF]	4K	Plug and Play ESCD data area
[FE000-FFFFF]	8K	BIOS runtime service routine (1)

I/O MAP

[000-01F]	DMA controller.(Master)
[020-021]	INTERRUPT CONTROLLER.(Master)
[022-023]	CHIPSET control registers. I/O ports.
[040-05F]	TIMER control registers.
[060-06F]	KEYBOARD interface controller.(8042)
[070-07F]	RTC ports & CMOS I/O ports.
[080-09F]	DMA register.
[0A0-0BF]	INTERRUPT controller.(Slave)
[0C0-0DF]	DMA controller.(Slave)
[0F0-0FF]	MATH COPROCESSOR.
[1F0-1F8]	HARD DISK controller.
[278-27F]	PARALLEL port 2.
[2B0-2DF]	GRAPHICS adapter controller.
[2F8-2FF]	SERIAL port 2.
[360-36F]	NETWORK ports.
[378-37F]	PARALLEL port 1.
[3B0-3BF]	MONOCHROME & PARALLEL port adapter.
[3C0-3CF]	EGA adapter.
[3D0-3DF]	CGA adapter.
[3F0-3F7]	FLOPPY DISK controller.
[3F8-3FF]	SERIAL port 1.

4-2 TIME & DMA CHANNELS MAP

TIME MAP: TIMER Channel 0 System timer interrupt.
TIMER Channel 1 DRAM REFRESH request.
TIMER Channel 2 SPEAKER tone generator.

DMA CHANNELS : DMA Channel 0 Available.
DMA Channel 1 Onboard ECP (Option).
DMA Channel 2 FLOPPY DISK (SMC CHIP).
DMA Channel 3 Onboard ECP (default).
DMA Channel 4 Cascade for DMA controller 1.
DMA Channel 5 Available.
DMA Channel 6 Available.
DMA Channel 7 Available.

4-3 INTERRUPT MAP

NMI: Parity check error.

IRQ (H/W):
0 System TIMER interrupt from TIMER 0.
1 KEYBOARD output buffer full.
2 Cascade for IRQ 8-15.
3 SERIAL port 2.
4 SERIAL port 1.
5 PARALLEL port 2.
6 FLOPPY DISK (SMC CHIP).
7 PARALLEL port 1.
8 RTC clock.
9 Available.
10 Available.
11 Available.
12 PS/2 Mouse.
13 MATH coprocessor.
14 Onboard HARD DISK(IDE1) channel.
15 Onboard HARD DISK(IDE2) channel.

4-4 RTC & CMOS RAM MAP

RTC & CMOS :	00	Seconds.
	01	Second alarm.
	02	Minutes.
	03	Minutes alarm.
	04	Hours.
	05	Hours alarm.
	06	Day of week.
	07	Day of month.
	08	Month.
	09	Year.
	0A	Status register A.
	0B	Status register B.
	0C	Status register C.
	0D	Status register D.
	0E	Diagnostic status byte.
	0F	Shutdown byte.
	10	FLOPPY DISK drive type byte.
	11	Reserve.
	12	HARD DISK type byte.
	13	Reserve.
	14	Equipment type.
	15	Base memory low byte.
	16	Base memory high byte.
	17	Extension memory low byte.
	18	Extension memory high byte.
	19-2d	
	2E-2F	
	30	Reserved for ectension memory low bytw.
	31	Reserved for extension memory high byte.
	32	DATE CENTURY byte.
	33	INFORMATION FLAG.
	34-3F	Reserve.
	40-7F	Reserved for CHIPSET SETTING DATA.

APPENDIX A: POST CODES

ISA POST codes are typically output to port address 80h.

POST(hex)	DESCRIPTION
01-02	Reserved.
C0	Turn off OEM specific cache, shadow.
03	1.Initialize EISA registers (EISA BIOS only). 2.Initialize all the standard devices with default values Standard devices includes. -DMA controller (8237). -Programmable Interrupt Controller (8259). -Programmable Interval Timer (8254). -RTC chip.
04	Reserved
05	1.Keyboard Controller Self-Test. 2.Enable Keyboard Interface.
06	Reserved.
07	Verifies CMOS's basic R/W functionality.
C1	Auto-detection of onboard DRAM & Cache.
C5	Copy the BIOS from ROM into E0000-FFFFF shadow RAM so that POST will go faster.
08	Test the first 256K DRAM.
09	OEM specific cache initialization. (if needed)
0A	1.Initialize the first 32 interrupt vectors with corresponding Interrupt handlers Initialize INT no from 33-120 with Dummy (Suprious) Interrupt Handler. 2.Issue CPUID instruction to identify CPU type. 3.Early Power Management initialization. (OEM specific)
0B	1.Verify the RTC time is valid or not. 2.Detect bad battery. 3.Read CMOS data into BIOS stack area. 4.PnP initializations including. (PnP BIOS only) -Assign CSN to PnP ISA card. -Create resource map from ESCD. 5.Assign IO & Memory for PCI devices. (PCI BIOS only)

POST(hex)	DESCRIPTION
0C	Initialization of the BIOS Data Area. (40:ON - 40:FF)
0D	1.Program some of the Chipset's value according to Setup. (Early Setup Value Program) 2.Measure CPU speed for display & decide the system clock speed. 3.Video initialization including Monochromc, CGA, EGA/VGA. If no display device found, the speaker will beep.
0E	1.Test video RAM. (If Monochromc display device found) 2.Show messages including. -Award Logo, Copyright string, BIOS Data code & Part No. -OEM specific sign on messages. -Energy Star Logo. (Green BIOS ONLY) -CPU brand, type & speed. -Test system BIOS checksum. (Non-Compress Version only)
0F	DMA channel 0 test.
10	DMA channel 1 test.
11	DMA page registers test.
12-13	Reserved.
14	Test 8254 Timer 0 Counter 2.
15	Test 8259 interrupt mask bits for channel 1.
16	Test 8259 interrupt mask bits for channel 2.
17	Reserved.
19	Test 8259 functionality.
1A-1D	Reserved.
1E	If EISA NVM checksum is good, exccute EISA initialization. (EISA BIOS only)
1F-29	Reserved.
30	Detect Base Memory & Extended Memory Size.
31	1.Test Base Memory from 256K to 640K. 2.Test Extended Memory from 1M to the top of memory.

POST(hex)	DESCRIPTION
32	1.Display the Award Plug & Play BIOS Extension message. (PnP BIOS only) 2.Program all onboard super I/O chips (if any) including COM ports, LPT ports, FDD port ... according to setup value.
33-3B	Reserved.
3C	Set flag to allow users to enter CMOS Setup Utility.
3D	1.Initialize Keyboard. 2.Install PS2 mouse.
3E	Try to turn on Level 2 cache. Note : Some chipset may need to turn on the L2 cache in this stage. But usually, the cache is turn on later in POST 61h.
3F-40	Reserved.
BF	1.Program the rest of the Chipset's value according to Setup. (Later Setup Value Program) 2.If auto-configuration is enabled, programmed the chipset with pre-defined Values.
41	Initialize floppy disk drive controller.
42	Initialize Hard drive controller.
43	If it is a PnP BIOS, initialize serial & parallel ports.
44	Reserved.
45	Initialize math coprocessor.
46-4D	Reserved.
4E	If there is any error detected (such as video, kb...), show all the error messages on the screen & wait for user to press <F1> key.
4F	1.If password is needed, ask for password. 2.Clear the Energy Star Logo. (Green BIOS only)
50	Write all CMOS values currently in the BIOS stack area back into the CMOS.
51	Reserved.

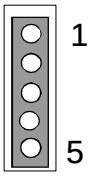
POST(hex)	DESCRIPTION
52	1.Initialize all ISA ROMs. 2.Later PCI initializations. (PCI BIOS only) -assign IRQ to PCI devices. -initialize all PCI ROMs. 3.PnP Initialzations. (PnP BIOS only) -assign IO, Memory, IRQ & DMA to PnP ISA devices. -initialize all PnP ISA ROMs. 4.Program shadows RAM according to Setup settings. 5.Program parity according to Setup setting. 6.Power Management Initialization. -Enable/Disable global PM. -APM interface initialization.
53	1.If it is NOT a PnP BIOS, initialize serial & paralled ports. 2.Initialize time value in BIOS data area by translate the RTC time value into a timer tick value.
60	Setup Virus Protection. (Boot Sector Protection) functionality according to Setup setting.
61	1.Try to turn on Level 2 cache. Note : if L2 cache is already turned on in POST 3D, this part will be skipped. 2.Set the boot up speed according to Setup setting. 3.Last chance for Chipset initialization. 4.Last chance for Power Management initialization. (Green BIOS only) 5.Show the system configuration table.
62	1.Setup daylight saving according to Setup value. 2.Program the NUM Lock, typematic rate & typematic speed according to Setup setting.
63	1.If there is any changes in the hardware configuration, update the ESCD information. (PnP BIOS only) 2.Clear memory that have been used. 3.Boot system via INT 19H.
FF	System Booting. This means that the BIOS already pass the control right to the operating system.

Unexpected Errors:

POST(hex)	DESCRIPTION
B0	If interrupt occurs in protected mode.
B1	Unclaimed NMI occurs.

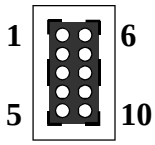
APPENDIX B: I/O CONNECTORS

J10: PS/2 MOUSE CONNECTOR:



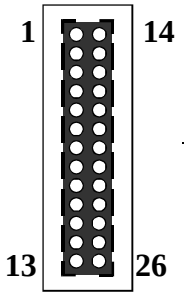
Pin	Signal Name
1	Data (Red Wire)
2	Clock(Blue Wire)
3	GND(Green Wire)
4	NC
5	VCC(Yellow Wire)

J13,J14: Serial Ports Connector



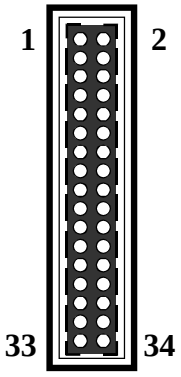
Signal Name	Pin	Pin	Signal Name
DCD	1	6	DSR
SIN	2	7	RTS
SOUT	3	8	CTS
DTR	4	9	RI
GND	5	10	N.C.

J15: Parallel Port Connector



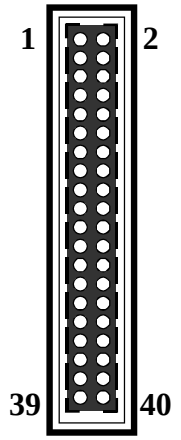
Signal Name	Pin	Pin	Signal Name
STROBE-	1	14	AUTO FEED-
Data Bit 0	2	15	ERROR-
Data Bit 1	3	16	INIT-
Data Bit 2	4	17	SLCT IN-
Data Bit 3	5	18	Ground
Data Bit 4	6	19	Ground
Data Bit 5	7	20	Ground
Data Bit 6	8	21	Ground
Data Bit 7	9	22	Ground
ACJ-	10	23	Ground
BUSY	11	24	Ground
PE	12	25	Ground
SLCT	13	26	N.C.

J11: Floppy Disk Connector



Signal Name	Pin	Pin	Signal Name
Ground	1	2	FDHDIN
Ground	3	4	Reserved
Ground	5	6	FDEDIN
Ground	7	8	Index-
Ground	9	10	Motor Enable
Ground	11	12	Drive Select B-
Ground	13	14	Drive Select A-
Ground	15	16	Motor Enable
Ground	17	18	DIR-
Ground	19	20	STEP-
Ground	21	22	Write Data
Ground	23	24	Write Gate
Ground	25	26	Track 00-
Ground	27	28	Write Protect-
Ground	29	30	Read Data-
Ground	31	32	SIDE 1 SELECT-
Ground	33	34	Diskette

IDE1,IDE2: Primary, Secondray Connector



Signal Name	Pin	Pin	Signal Name
Reset IDE	1	2	Ground
Host Data 7	3	4	Host Data 8
Host Data 6	5	6	Host Data 9
Host Data 5	7	8	Host Data 10
Host Data 4	9	10	Host Data 11
Host Data 3	11	12	Host Data 12
Host Data 2	13	14	Host Data 13
Host Data 1	15	16	Host Data 14
Host Data 0	17	18	Host Data 15
Ground	19	20	Key
DRQ3	21	22	Ground
I/O Write-	23	24	Ground
I/O Read-	25	26	Ground
IOCHRDY	27	28	BALE
DACK3-	29	30	Ground
IRQ14	31	32	IOCS16-
Addr 1	33	34	Ground
Addr 0	35	32	Addr 2
Chip Select 0-	37	38	Chip Select 1-
Activity	39	40	Ground