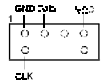
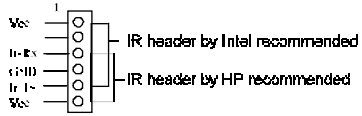
Jumper Setting Quick Reference

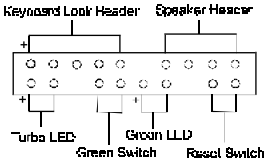
J4: PS/2 mouse connector

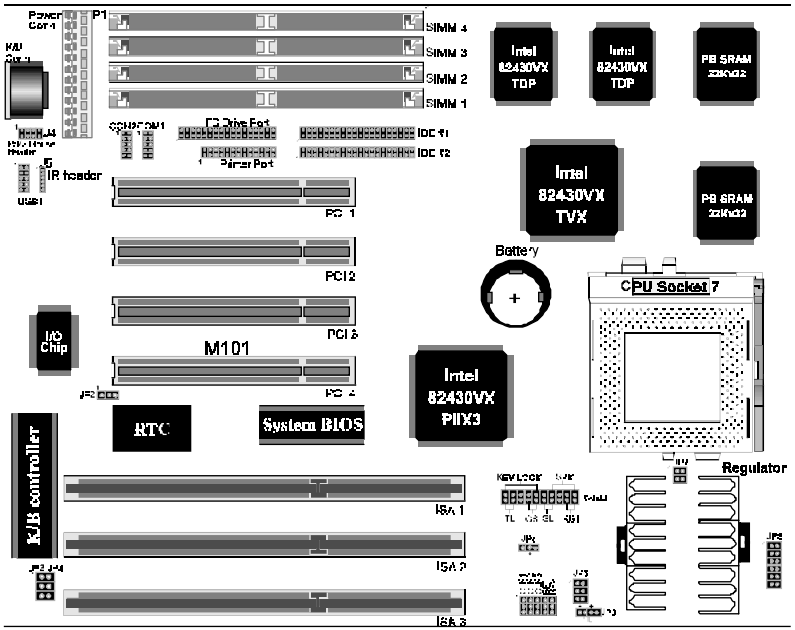


J5: IR connector



PANEL1:





JP2: CMOS clear data jumper
1~2 short: Normal (default)
2~3 short: Clear CMOS data

JP3: PS/2 Mouse Enable/Disable
1~2 short: Normal (default)
2~3 short: PS/2 mouse disable

JP4: Password bypass control jumper
1~2 short: Normal (default)
2~3 short: Password bypass

JP5: CPU cooling fan header

JP9: Hard disk LED header

Int. CPU Speed = Speed rate x System clock	BF1	BF2
75/90/100 = 1.5 x system clock	1~2	1~2
110/120/133 = 2 x system clock	2~3	1~2
150/166 = 2.5 x system clock	2~3	2~3
180/200 = 3 x system clock	1~2	2~3

For VRT (Voltage Reduction Technology) processor (such as Intel P55C), the split power plan (CPU's core voltage ≠ CPU's I/O voltage) design is required.

Core Vcc			I/O Vcc	
V	JP7	JP8	V	JP6
2.5	1	3	3.3	1
2.6		4	3.4	1
2.8		5		
2.9		6	3.5	1

CPU-type		S-spce	CPU Power Voltage I/O Vcc	CPU Power Voltage Core Vcc	JP6	JP7	JP8	System freq. MHz	System freq. CLK1, CLK2, CLK3	Freq. ratio Speed rate	Freq. ratio BF1, BF2
Intel	P54C-75		3.3		JP6 1	JP7 1 2	JP8 1	50	CLK1,CLK2,CLK3 1	x1.5	BF1 BF2 1
	P54C-90	QO653 QO655 SZ978 SX957 SX959	3.3		JP6 1			60	CLK1,CLK2,CLK3 1	x1.5	BF1 BF2 1
		QO654 SX958	3.4		JP6 1						
			3.5		JP6 1						
	P54C-120	QO708	3.3		JP6 1					x2	BF1 BF2 1
	P54C-150		3.5		JP6 1					x2.5	BF1 BF2 1
	P54C-100	QO656	3.3		JP6 1			66	CLK1,CLK2,CLK3 1	x1.5	BF1 BF2 1
		QO657	3.4		JP6 1						
	P54C-133		3.5		JP6 1					x2	BF1 BF2 1
	P54C-166									x2.5	BF1 BF2 1
	P54C-200									x3	BF1 BF2 1
	P55C-166		3.3	2.8	JP6 1	JP7 1 2	JP8 1			x2.5	BF1 BF2 1
	P55C-200									x3	BF1 BF2 1
Cyrix	6x86-P120 @100MHz	028	3.5		JP6 1	JP7 1 2	JP8 1	50	CLK1,CLK2,CLK3 1	x2	BF1 BF2 1
	6x86-P133 @110MHz							55	CLK1,CLK2,CLK3 1		
	6x86-P150 @120MHz							60	CLK1,CLK2,CLK3 1		
	6x86-P166 @133MHz							66	CLK1,CLK2,CLK3 1		
AMD	K5-PR75	ABQ	3.5		JP6 1	JP7 1 2	JP8 1	50	CLK1,CLK2,CLK3 1	1.5	BF1 BF2 1
	K5-PR90							60	CLK1,CLK2,CLK3 1		
	K5-PR100							66	CLK1,CLK2,CLK3 1		