Chapter 1

System Board Overview

1.1 The mainboard specifications

1. CPU:	Intel Pentium 75/90/100/120/133/150/180 MHz
2. On board PCI IDE:	Built-in SiS chipsets Two IDE channels, Supports up to 4 Hard Drives
3. On board FDC:	Supports two floppy disk drives up to 2.88MB
4. On board Fast I/O:	Advanced High Performance Controllers Enhanced Parallel Port (EPP) Compatible Extended Capabilities Port (ECP) Compliant Two high speed NS16C550 UARTs with 16 Bytes FIFOs
5. Cache memories:	Primary: Built-in 16KB in Pentium Secondary: Standard: 0/256/512 KB Default: Standard 256KB (W/T, W/B)
6. L2 cache module:	Supports Standard/Burst/Pipeline SRAM
7. Memory:	128MB max on board Using four 72pin SIMM modules Support from 2MB to 128MB
8. I/O slots:	Four 32-bit PCI slots, three 16-bit slots for AT compatible add-on cards.
9. BIOS:	Award BIOS (EPROM or Flash ROM)

1.3 Placement

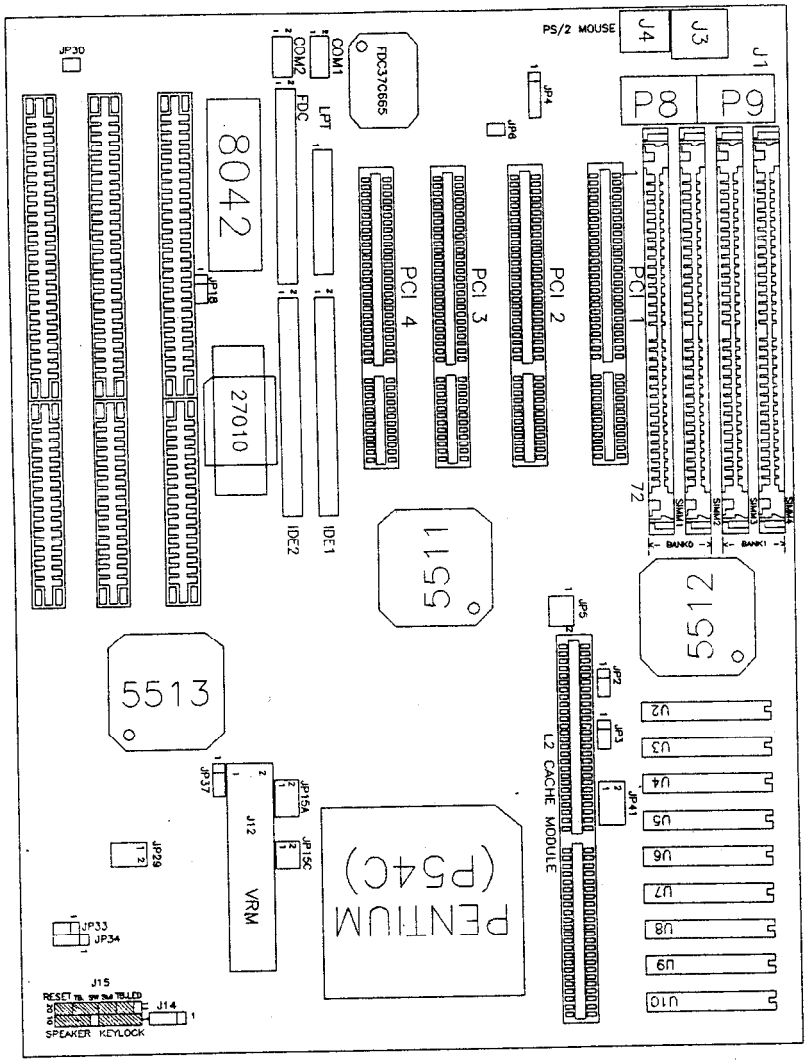

Figure 1-1

Table 1. Members of Pentium processors Family supported on the AB-PH5 motherboard.

	Pentium Processor (610/75, 735/90, 815/100) (Note 1)	P54CS	P55C	P54CT	P55CT
Core Freq. (MHz)	75, 90, 100	120, 133	133, 150	125, 150, 166, 180	TBD
Bus Freq.	50, 60, 66	60, 66	60, 66	50, 60, 66	60, 66
Core Voltage	3.3V	3.3V	2.5V	3.3V	2.5V (Note 2)
I/O Voltage	3.3V	3.3V	3.3V	3.3V	3.3V
Max. Power Dissipation	10.1W @ 100MHz	~11W@ 133MHz	~8W@ 150MHz	15W	20W
Package	296 Pin SPGA	296 Pin SPGA	296 Pin SPGA	320 Pin SPGA (Socket 5/7)	321 Pin SPGA (Socket 7)

Note: 1. This includes the Pentium Processor VR s-spec (3.3V +5% -0%) and VRM/MD s-spec (3.45V to 3.6V).
2. Intel will provide a 2.5V Voltage Regulator Module with the P55CT to meet the core Vcc requirement.

1.4.2 EDO DRAM

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. EDO DRAM holds the memory data valid until the next CAS# falling edge, unlike standard fast page mode DRAM which tri-states the memory data when CAS# negates to precharge for the next cycle. With EDO, the CAS# precharge overlaps the data valid time, allowing CAS# to negate earlier while still satisfying the memory data valid window time.

This is one variation of the regular page mode DRAM with minor changes in the CAS# and data output timing. Figure 1-2 illustrates the data out on page mode DRAM and EDO DRAM.

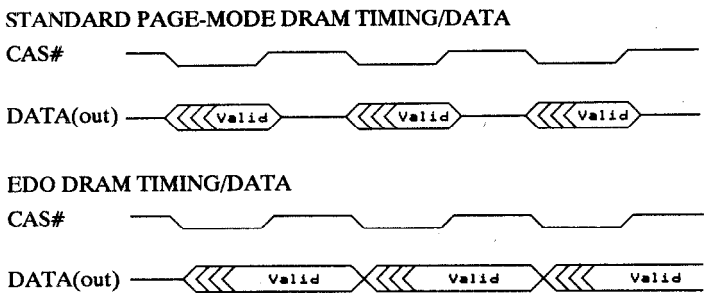

Figure 1-2

By using EDO DRAM, the CPU to memory bandwidth will increase from 100MB/s to >200MB/s. The EDO DRAM has about 5% premium of the page mode DRAM at this stage. Both of them are available on 72-pin SIMM module. There is no physical difference on the dimension and users can plug either type into the SIMM sockets.

1.4.3 Burst & pipeline burst SRAM (L2 cache module)

Various types of SRAM can be used to implement the level-2 cache for Pentium processor motherboards. Asynchronous SRAM, standard burst SRAM, and pipelined burst SRAM are three examples. The following table shows the performance of the level-2 cache using asynchronous and pipelined burst SRAM. The bandwidth of CPU to Pipeline Burst SRAM > 300MB/s.

Cycle Type	Asynch. SRAM	Pipelined Burst SRAM
Burst Read	3-2-2-2	3-1-1-1
Burst Write (Write Back)	4-3-3-3	3-1-1-1
Single Read	3	3
Single Write	4	3
Back-to-back Burst Read	3-2-2-2-2	3-1-1-1-1

The numbers in the table on the left mean the "T" (CPU clock) for each operation. i.e. 3-1-1-1 means the first data will be available at the third "T" when issue the operation, then the following data only need one additional "T" cycle, and so on. For example, to execute 4 consequently read operations, it only requires 6 "T" by using pipelined burst SRAM vs. 9 "T" using async. SRAM.

1.4.4 Keyboard connector

The standard Baby-AT form factor specifies an AT style keyboard connector. The baseboard is designed to accept either a standard AT style keyboard connector or PS/2 style mouse and keyboard connectors. Boards will include AT style keyboard connector and PS/2 style mouse connector.

1.4.5 Bus Master IDE

The traditional PIO (Programmable I/O) IDE requires the CPU to handle all the activities of the IDE access including waiting for the mechanical parts. When the CPU becomes faster, the workload of CPU becomes relatively inefficient. In order to reduce the workload of the CPU and to use the CPU more efficiently, a Bus Master logic has been designed in the Triton chipset which will take care of the data transfer between IDE and main memory. The CPU can handle other events while waiting for data transfer between memory and IDE devices.

The enhanced IDE controller on AB-PH5 M/B has two more dedicated DMA channels for Bus Master IDE and 32 bytes of PCI-IDE buffer. The enhanced IDE controller basically provides the PIO mode 3 and mode 4 IDE. The maximum data transfer rate for mode 4 IDE can reach up to 15MB/sec. and the data transfer rate under DMA mode 2 on AB-PH5 M/B can reach up to 22MB/sec. (Max.)

No matter how good the IDE interface is, either PIO or bus master IDE needs a fast hard disk drive to deliver the best performance.

1.4.6 Plug and Play BIOS

The ISA bus architecture requires the allocation of memory and I/O addresses, DMA channels and interrupt levels among multiple ISA cards. However, configuration of ISA cards is typically done with "jumper" that change the decode maps for memory and I/O space and steer the DMA and interrupt signals to different pins on the bus. Further, system configuration files may need to be updated to reflect these changes. Users typically resolve sharing conflicts by referring to documentation provided by each manufacturer. For the average user, this configuration process can be unreliable frustrating.

Plug and Play (PnP) eliminates the ISA add-on card hardware conflict problem. The PnP BIOS uses a memory block to define and remember each card's configuration, which allows the user to change card's IRQs, DMA in BIOS automatically or manually. The focus is on ease-to-use for the users.

The AB-PH5 M/B PnP BIOS provides an inter-operation with legacy ISA cards and Plug and Play ISA cards.

1.4.7 VRM (Voltage Regulator Module)

When the CPU socket is populated with P55C, a 2.5V OEM or third party vendor VRM is installed in the VRM socket to supply 2.5V to the CPU core Vcc pins. When upgraded with P55CT, the original P55C VRM is replaced by an end-user installed VRM (that is shipped with the processor) to supply the proper voltage and current to the P55CT core. The 3.3V supply require for CPU I/O is not provided by the VRM in the case of P55C or P55CT. The VRM only supplies 2.5V to the core Vcc pins. The P55C VRM and P55CT VRM however will have provision to allow 3.3V from the power supply to pass through to the CPU I/O volatge island (or motherboard's regulator to pass through to the CPU I/O voltage island).

Connector Name	Pin Assignments	Description
Turbo LED Connector J15 (12, 13 Pin)	Pin 12: Cathode terminal of LED. Pin 13: Anode terminal of LED.	If the connection is correct, the turbo LED will light up when the system is in turbo speed mode. Otherwise the turbo LED will be off.
Turbo Switch Connector: J15 (16, 17, 18 Pin)	Pin16: Ground. Pin 17: Turbo Signal. Pin 18: No connection.	16-17: Low speed mode. 17-18: Turbo mode. Connect Pin 16, 17, 18 to the chassis' turbo button cable.
Hardware Reset Connector: J15 (19, 20 Pin)	Pin 19: Reset input Pin 20: Ground	Connect to the chassis' reset button cable. Press and hold the reset button for at least one second to reset the system.
Keylock and Power LED connector: J15 (1-5 Pin)	Pin 1: +5VDC. Pin 2: No connection. Pin 3: Ground. Pin 4: Keyboard inhibit Signal. Pin 5: Ground.	Connect to the chassis' keylock and Power LED' cable.
Speaker connector: J15 (7-10 Pin)	Pin 7: Sound signal. Pin 8: Ground. Pin 9: Ground. Pin 10: +5VDC.	Connect to the speaker connector in the front panel of the chassis.
Keyboard connector: J3 (5 Pins)	Pin 1: Keyboard clock. Pin 2: Keyboard data. Pin 3: No connection. Pin 4: Ground. Pin 5 : +5VDC.	Connect to the Keyboard connector.
PS/2 Mouse connector: J4 (6 Pins)	Pin 1: Mouse data. Pin 2: No connection. Pin 3: Ground. Pin 4: +5VDC. Pin 5 : Mouse clock. Pin 6: No connection.	Connect to the PS/2 mouse connector.
External Battery Connector: JP34 (4 Pins)	Pin 1: 4.5V battery input Pin 2: N.C. Pin 3: Ground Pin 4: Ground	If on-board battery no longer functions remove it from the mainboard and connect a 4.5V external battery to the 4 pin JP34.
Auxilary 12V fan power: JP37 (3 Pins)	Pin 1: Ground Pin 2: +12V Pin 3: Ground	Connect to 12V Fan power.

2.3 Jumpers

Jumper No.	No. of Pins		Description	Default Setting
JP18	3	1-2 2-3	Flash ROM write voltage 12V Flash ROM write voltage 5V	2-3
JP33	3	2-3 1-2	CMOS RAM Discharge Normal	1-2
J15(14,15Pin)	2		Suspend switch	
J14	4		HDD LED Connector	
J12 (VRM)	30	12-14, 11-13 OFF	Use on board regulator Use VRM module	12-14, 11-13
JP2 (For L2 cache module only)	3	1-2 2-3	L2 Asynchronous SRAM L2 Burst/Pipeline Burst SRAM	2-3
JP3 (On board cache)	3	1-2 2-3	256KB (Async) 512KB (Async)	1-2
JP15A	6		1-2 3-4 5-6 Bus speed OFF ON ON 50 ON OFF ON 60 ON ON ON 66	1-2, 5-6
JP15C	4		1-2 3-4 Fraction/Ratio OFF OFF 2/3 ON OFF 1/2 OFF ON 1/3 ON ON 2/5	OFF
JP5	4	1, 3 2, 4	* SM Out Ground	
JP6	2	ON OFF	Disable Multi-I/O (SMC) Enable Multi-I/O (SMC)	OFF
JP29	6	1-2 3-4 5-6	3.3V (CPU voltage) 3.45V (CPU voltage) 3.6V (CPU voltage)	3-4
JP30	2	ON OFF	Color Monitor Mono Monitor	ON
JP41	10		Reserved for future	OFF

Notes: JP15A, JP15C see page 3-4 for detail description.
* SM Out are the System Management Output control pins. This pin is used to control peripheral's power, clock .... etc, for power management. SM Out is an active-low signal.

Bank1		Bank 0		Total
SIMM4	SIMM3	SIMM2	SIMM1	
Empty	Empty	Empty	1Mx32 (4MB)	4MB
Empty	Empty	Empty	2Mx32 (8MB)	8MB
Empty	Empty	Empty	4M x 32 (16MB)	16MB
Empty	Empty	Empty	8Mx32 (32MB)	32MB
Empty	Empty	256Kx32 (1MB)	256K x 32 (1MB)	2MB
Empty	Empty	1M x 32 (4MB)	1Mx32 (4MB)	8MB
Empty	Empty	2Mx32 (8MB)	2M x 32 (8MB)	16MB
Empty	Empty	4Mx32 (16MB)	4M x 32 (16MB)	32MB
Empty	Empty	8Mx32 (32MB)	8M x 32 (32MB)	64MB
256Kx32 (1MB)	256Kx32 (1MB)	Empty	Empty	2MB
256Kx32 (1MB)	256Kx32 (1MB)	256Kx32 (1MB)	256Kx32 (1MB)	4MB
256Kx32 (1MB)	256Kx32 (1MB)	1Mx32 (4MB)	1Mx32 (4MB)	10MB
256Kx32 (1MB)	256Kx32 (1MB)	2Mx32 (8MB)	2Mx32 (8MB)	18MB
256Kx32 (1MB)	256Kx32 (1MB)	4Mx32 (16MB)	4Mx32 (16MB)	34MB
256Kx32 (1MB)	256Kx32 (1MB)	8Mx32 (32MB)	8Mx32 (32MB)	66MB
1M x 32 (4MB)	1Mx32 (4MB)	Empty	Empty	8MB
1M x 32 (4MB)	1Mx32 (4MB)	256Kx32 (1MB)	256Kx32 (1MB)	10MB
1M x 32 (4MB)	1Mx32 (4MB)	1Mx32 (4MB)	1M x 32 (4MB)	16MB
1M x 32 (4MB)	1Mx32 (4MB)	2Mx32 (8MB)	2M x 32 (8MB)	24MB
1M x 32 (4MB)	1Mx32 (4MB)	4Mx32 (16MB)	4M x 32 (16MB)	40MB
1M x 32 (4MB)	1Mx32 (4MB)	8Mx32 (32MB)	8M x 32 (32MB)	72MB
2M x 32 (8MB)	2Mx32 (8MB)	Empty	Empty	16MB
2M x 32 (8MB)	2Mx32 (8MB)	256Kx32 (1MB)	256Kx32 (1MB)	18MB
2M x 32 (8MB)	2Mx32 (8MB)	1Mx32 (4MB)	1M x 32 (4MB)	24MB
2M x 32 (8MB)	2Mx32 (8MB)	2Mx32 (8MB)	2M x 32 (8MB)	32MB
2M x 32 (8MB)	2Mx32 (8MB)	4Mx32 (16MB)	4M x 32 (16MB)	48MB
2M x 32 (8MB)	2Mx32 (8MB)	8Mx32 (32MB)	8M x 32 (32MB)	80MB
4M x 32 (16MB)	4Mx32 (16MB)	Empty	Empty	32MB
4M x 32 (16MB)	4Mx32 (16MB)	256Kx32 (1MB)	256Kx32 (1MB)	34MB
4M x 32 (16MB)	4Mx32 (16MB)	1Mx32 (4MB)	1M x 32 (4MB)	40MB
4M x 32 (16MB)	4Mx32 (16MB)	2Mx32 (8MB)	2M x 32 (8MB)	48MB
4M x 32 (16MB)	4Mx32 (16MB)	4Mx32 (16MB)	4M x 32 (16MB)	64MB
4M x 32 (16MB)	4Mx32 (16MB)	8Mx32 (32MB)	8M x 32 (32MB)	96MB
8M x 32 (32MB)	8Mx32 (32MB)	Empty	Empty	64MB
8M x 32 (32MB)	8Mx32 (32MB)	256Kx32 (1MB)	256Kx32 (1MB)	66MB
8M x 32 (32MB)	8Mx32 (32MB)	1Mx32 (4MB)	1M x 32 (4MB)	72MB
8M x 32 (32MB)	8Mx32 (32MB)	2Mx32 (8MB)	2M x 32 (8MB)	80MB
8M x 32 (32MB)	8Mx32 (32MB)	4Mx32 (16MB)	4M x 32 (16MB)	96MB
8M x 32 (32MB)	8Mx32 (32MB)	8Mx32 (32MB)	8M x 32 (32MB)	128MB

Table 1-1

3.3 CPU frequency selection

CPU speed	Bus speed	JP15A			JP15C	
		1-2	3-4	5-6	1-2	3-4
75 MHz	50 MHz	OFF	ON	ON	OFF	OFF
90 MHz	60 MHz	ON	OFF	ON	OFF	OFF
100 MHz	66 MHz	ON	ON	ON	OFF	OFF
120 MHz	60 MHz	ON	OFF	ON	ON	OFF
125 MHz	50 MHz	OFF	ON	ON	ON	ON
133 MHz	66 MHz	ON	ON	ON	ON	OFF
150 MHz	60 MHz	ON	OFF	ON	ON	ON
166 MHz	66 MHz	ON	ON	ON	ON	ON
180 MHz	60 MHz	ON	OFF	ON	OFF	ON