RU430HX Motherboard Specification Update

Release Date: January 1998

Order Number: 281811-012

The RU430HX motherboard may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

Copies of documents which have an ordering number and are referenced in this document, or other Intel literature, may be obtained from:

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or call in North America 1-800-548-4725, Europe 44-0-1793-431-155, France 44-0-1793-421-777,

Germany 44-0-1793-421-333, other Countries 708-296-9333

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REVISION HISTORY

Date of Revision	Version	Description
May 1996	-001	This document is the first Specification Update for the Intel RU430HX motherboard.
June 1996	-002	Changed product name from Advanced/RU to RU430HX. Added Errata 2-5. Added Documentation Changes 1-10.
July 1996	-003	Added Documentation Changes 11-14.
October 1996	-004	Added Documentation Changes 15-16.
November 1996	-005	Added Erratum 6.
December 1996	-006	Added Errata 7-8.
February 1997	-007	Added PBA/BIOS Table. Modified Documentation Changes 1 and 8.
March 1997	-008	Added AA Revision to Motherboard Identification table. Added Errata 9-10. Updated status of Errata 2-5 and 7.
April 1997	-009	Revised format of PBA/BIOS revision table. Added Errata 11-12.
June 1997	-010	Added Specification Clarifications 1-2 and Documentation Change 17. Updated status of Errata 6 and 10.
July 11997	-011	Added Specification Clarification 3 and Documentation Change 18.
January 1998	-012	Added Erratum 13. Updated status of Erratum 1.

PREFACE

This document is an update to the specifications contained in the *RU430HX Motherboard Technical Product Specification* (Order Number 281811). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® Processor Specification Update* (Order Number 242480) for specification updates concerning the Pentium processor. Items contained in the *Pentium Processor Specification Update* that either do not apply to the RU430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82430HX PCIset Specification Update* (Order Number 297652) for specification updates concerning the 82430HX PCIset. Items contained in the *82430HX PCIset Specification Update* that either do not apply to the RU430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Refer to the *82371SB PIIX3 Specification Update* (Order Number 297658) for specification updates concerning the 82371SB PIIX3. Items contained in the *82371SB PIIX3 Specification Update* that either do not apply to the RU430HX motherboard or have been worked around are noted in this document. Otherwise, it should be assumed that any PCIset errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the RU430HX motherboard's behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all motherboards.

Specification Update for RU430HX Motherboards

GENERAL INFORMATION

Basic RU430HX Motherboard Identification Information

AA Revision	PBA Revision	430HX PCIset Stepping	BIOS Version	Notes
652513-301	651614-301	A1	1.00.01.CW0	1, 2, 3, 6, 8
652513-401	651614-301	A1	1.00.01.CW0	1, 2, 3, 6, 8
652513-302	651614-302	A1	1.00.01.CW0	1, 2, 3, 6, 8
661752-501	661731-501	A1	1.00.04.CW0	1, 3, 4, 6, 9
661752-502	661731-502	A3	1.00.05.CW0	1, 3, 5, 7, 9
661752-503	661731-503	A3	1.00.05.CW0	1, 3, 5, 7, 9
661752-504	661731-504	A3	1.00.05.CW0	1, 3, 5, 7, 9
666579-500	666578-500	A3	1.00.04.DL0	1, 3, 5, 7, 9
666579-501	666578-501	A3	1.00.06.DL0	1, 3, 5, 7, 9
666579-502	666578-502	A3	1.00.06.DL0	1, 5, 7, 9-10
666579-503	666578-503	A3	1.00.08.DL0	1, 5, 7, 9-10

NOTES:

1. The PBA number is found on a small label on the component side of the board
2. The 430HX PCIset kit used on this PBA revision consists of two components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	A1	SU052

3. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71-79, all DP errata, all AP errata, all TCP errata. All other errata in Part I may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*
4. The 430HX PCIset kit used on this PBA revision consists of two components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A1	SU087
82371SB	B0	SU093

5. The 430HX PCIset kit used on this PBA revision consists of two components as follows:

Device	Stepping	S-Spec Numbers
82439HX	A3	SU115
82371SB	B0	SU093

6. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 2-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
7. The following errata contained in the *82430HX PCIset Specification Update* (Order Number 297652) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 1-3. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82430HX PCIset Specification Update*.
8. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 1-2, 4-13. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
9. The following errata contained in the *82371SB PIIX3 Specification Update* (Order Number 297658) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 1-2, 4-13. All other errata associated with the PCIset apply to this PBA revision. For specific details of any erratum please refer to the *82371SB PIIX3 Specification Update*.
10. The following errata contained in Part I of the *Pentium® Processor Specification Update* (Order Number 242480) either do not apply to the RU430HX motherboard or have been worked around in this PBA and/or BIOS revision: 5, 7, 9-11, 13-14, 16-17, 29, 31, 34, 36-37, 39, 40, 46, 48-50, 58, 60-64, 66-67, 69, 71, all DP errata, all AP errata, all TCP errata. All other errata in Part II may apply to this revision level of the motherboard, depending on the stepping of the processor or the specific software that is being executed. Also, some of these errata apply only to motherboards being used in an application development environment. For specific details of any erratum please refer to the *Pentium Processor Specification Update.*

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the RU430HX motherboard. Intel intends to fix some of the errata in a future revision of the motherboard, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the motherboard or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	ERRATA
1	Fixed	ECC non-detection of single-/double-bit errors on partial memory writes
2	Fixed	BIOS SETUP does not recognize February 29, 2000 as a valid date
3	Fixed	System BIOS does not recognize certain dates as valid
4	Fixed	PCI Delayed Transactions are not supported
5	Fixed	System BIOS may detect memory in unpopulated SIMM* rows
6	Fixed	BIOS does not support no-emulation mode for CD-ROM boot
7	Fix	CMOS checksum may be lost if power is cycled during boot
8	NoFix	PCI device scan may terminate abnormally
9	Fixed	Audio IRQ may not function correctly after boot
10	NoFix	Slave on secondary IDE channel is not disabled
11	Fix	System BIOS does not recognize bootable USB devices
12	NoFix	Cannot meet FCC Class B requirements using unshielded USB cable
13	NoFix	System BIOS may corrupt audio add-in card EEPROM
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Advanced Power Management (APM) will not function as expected with Universal Serial Bus (USB) enabled
2	Doc	PCI 2.1 Specification optional features
3	Doc	Administrator and user passwords

NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Correction to BIOS identifier
2	Doc	Corrections to board feature drawing
3	Doc	Add Parity/ECC setup option to System Memory description
4	Doc	Add “Each device mode is supported independently, even when operating devices of different modes on the same cable.” as the last sentence of paragraph 1, Section 1.6.3
5	Doc	Add note to table of riser connector signal descriptions
6	Doc	Power Supply Connectors section should read “SLEEP/PWR”, not “PS SLEEP” in Section 1.10.14
7	Doc	Add manufacturing options for on-board audio
8	Doc	Add Table 13 to Section 3.3, BIOS upgrades
9	Doc	Change overview of setup menu screens
10	Doc	Add audio configuration options to description of Setup screens
11	Doc	Remove 180 MHz jumper settings from CPU configuration table 4 in section 1.11.1. References to “J9C1” in the table header should be changed to “J1F1”.
12	Doc	Additions to power consumption table
13	Doc	Additions to regulatory compliance section
14	Doc	Change description in section 2.4, Table 9 for Device Number 08 to read as “S3* Graphics Controller”.
15	Doc	Addition of connector descriptions to Section 1.10
16	Doc	Addition of jumper description to Section 1.11
17	Doc	Revision of Section 1.10.16.3, Wavetable Upgrade
18	Doc	Revision of Section 1.11.3, Clear CMOS Jumper

The errata described in this specification update apply to combinations of PBA revision and BIOS revision as shown in the table below. Descriptions of the individual errata referred to by number in the table below are found in the ERRATA section of this document.

PBA Revision	BIOS Revision	Errata That Apply
651614-301	1.00.01.CW0	1-8, 10
	1.00.02.CW0	1, 4 ,6-8, 10
	1.00.04.CW0	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10
651614-302	1.00.01.CW0	1-8, 10
	1.00.02.CW0	1, 4 ,6-8, 10
	1.00.04.CW0	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10
661731-501	1.00.01.CW0‡	1-8, 10
	1.00.02.CW0‡	1, 4 ,6-8, 10
	1.00.04.CW0	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10
661731-502	1.00.01.CW0‡	1-8, 10
	1.00.02.CW0‡	1, 4 ,6-8, 10
	1.00.04.CW0‡	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10
661731-503	1.00.01.CW0‡	1-8, 10
	1.00.02.CW0‡	1, 4 ,6-8, 10
	1.00.04.CW0‡	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10
661731-504	1.00.01.CW0‡	1-8, 10
	1.00.02.CW0‡	1, 4 ,6-8, 10
	1.00.04.CW0‡	1, 4 ,6-8, 10
	1.00.05.CW0	1, 4 ,6-8, 10

PBA Revision	BIOS Revision	Errata That Apply
666578-500	1.00.04.DL0	1, 6, 8-13
	1.00.06.DL0	1, 6, 8, 10-13
	1.00.07.DL0	8, 10-13
	1.00.08.DL0	8, 10-13
666578-501	1.00.04.DL0‡	1, 6, 8-13
	1.00.06.DL0	1, 6, 8, 10-13
	1.00.07.DL0	8, 10-13
	1.00.08.DL0	8, 10-13
666578-502	1.00.04.DL0‡	1, 6, 8-13
	1.00.06.DL0	1, 6, 8, 10-13
	1.00.07.DL0	8, 10-13
	1.00.08.DL0	8, 10-13
666578-503	1.00.04.DL0‡	1, 6, 8-13
	1.00.06.DL0‡	1, 6, 8, 10-13
	1.00.07.DL0‡	8, 10-13
	1.00.08.DL0	8, 10-13

‡ Note: This combination of BIOS revision and PBA revision has not undergone regression testing. Use of a PBA with down-revision BIOS is an untested combination and is undertaken at the user's risk.

ERRATA

1. ECC Non-detection of Single/Double-Bit Errors on Partial Memory Writes

PROBLEM: When the 82439HX TXC performs a partial write to main memory (data less than a 64-bit quadword) in ECC mode, single bit errors are corrected but not logged. Double-bit errors are not detected or logged.

IMPLICATION: Normally, the controller is able to buffer writes and group them into quadwords. In all these cases where 64 bits are written to memory at a time, both single and double-bit errors will be signaled to the operating system. Single bit errors will be corrected using the information contained in the checkbits that are stored with the data in memory. Double-bit errors cannot be corrected by the memory controller, but the operating system can warn the user that the error has occurred. If the controller must perform a partial write, a read-merge-write cycle will occur so that the proper checkbits can be regenerated across the entire 64 bits to be written into DRAM. If erroneous data is read during this cycle, the following will occur:

For single bit errors, the error will be corrected based on the memory checkbits. The corrected data will be written back to memory, but the error will not be flagged to the system, so the user will not receive information from the error log that could be useful in isolating a failing memory module.

For double-bit errors, no error will be detected or signaled to the operating system. The erroneous data will be rewritten to memory and a set of regenerated checkbits will be rewritten at the same time, marking the erroneous data as correct.

WORKAROUND: None. However, for ECC systems that require only single bit error protection, the A1 stepping of the 430HX PCIset does provide this level of reliability.

STATUS: This erratum was fixed in PBA revision 666578-500 or higher when used with BIOS revision 1.00.07.DL0 or higher. This erratum will not be fixed in other PBAs.

2. BIOS SETUP Does Not Recognize February 29, 2000 As a Valid Date

PROBLEM: The BIOS Setup program will not allow the system date to be set to Feb 29, 2000.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: If the system BIOS has not been upgraded, the system date will have to be reset to the correct date on March 1, 2000.

STATUS: This erratum was fixed in BIOS revision 1.00.02.CW0 and in BIOS revision 1.00.04.DL0.

3. System BIOS Does not Recognize Certain Dates As Valid

PROBLEM: If the motherboard is powered on or reset with the system date set to October 20-31 or December 20-31, the system BIOS will report “CMOS Time and Date Not Set” and the system date will be reset to Jan 01, 1990 during Power On Self Test (POST). If the user resets the system to the correct date and reboots, the system BIOS reports the same error message and again resets the date to Jan 01, 1990.

IMPLICATION: Any program that uses the system time and date stamps to determine when to perform some activity will not perform that scheduled activity. Date and time stamps for files created on these dates will be incorrect.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision 1.00.02.CW0 and in BIOS revision 1.00.04.DL0.

4. PCI Delayed Transactions Are Not Supported

PROBLEM: An erratum to the A1 stepping of the 82371SB PCI ISA IDE Xcelerator (PIIX3) requires that the option for Delayed Transactions be turned off by the BIOS.

IMPLICATION: System level performance and compatibility are not affected by turning off delayed transactions. The system will be PCI 2.1 compatible and will support all PCI 2.1 compliant cards.

WORKAROUND: None.

STATUS: This erratum was fixed in PBA revision 666578-500 and BIOS revision 1.00.04.DL0. This erratum will not be fixed in other PBAs.

5. System BIOS May Detect Memory In Unpopulated SIMM Rows*

PROBLEM: During Power-On Self Test (POST), the system BIOS may improperly determine that memory is present in an unpopulated SIMM* bank. Subsequently, the BIOS memory sizing algorithm may fail to reflect the correct total memory configuration.

IMPLICATION: If memory is falsely detected in the first SIMM bank (Bank 0), a POST error (code E8h) will be generated and the system will not boot. No sizing problems have been observed in cases where memory is falsely detected in a higher numbered SIMM bank and the lowest numbered bank is populated.

WORKAROUND: Install SIMMs in consecutive banks beginning with Bank 0.

STATUS: This erratum was fixed in BIOS revision 1.00.02.CW0 and in BIOS revision 1.00.04.DL0.

6. BIOS Does Not Support No-Emulation Mode for CD-ROM Boot

PROBLEM: The system BIOS does not support booting from an “El Torito” bootable CD-ROM using the no-emulation mode format.

IMPLICATION: Booting from a CD-ROM using no emulation mode is not supported. For example, Microsoft Windows* NT* version 4.0 uses no-emulation mode for its boot CD-ROM.

WORKAROUND: Boot the computer from a floppy or hard disk, then install or run the program from the CD-ROM.

STATUS: This erratum was fixed in BIOS revision 1.00.07.DL0. This erratum will not be fixed in other BIOS versions.

7. CMOS Checksum May Be Lost If Power Is Cycled During Boot

PROBLEM: If the computer power is turned off during a short portion of the boot process, the CMOS checksum byte will not be updated. The next time the computer is turned on, the message "CMOS Checksum Invalid" will be displayed.

IMPLICATION: When the message is displayed, the correct checksum has already been recalculated and stored. No user action is required to recover from the error. If the additional message:

Date and Time Not Set
Press <F1> for Setup, <Esc> to Boot

is displayed, the user will have to reset the current date and time using the BIOS Setup program.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS 1.00.04.DL0. This erratum will not be fixed in BIOS CW0.

8. PCI Device Scan May Terminate Abnormally

PROBLEM: If the system does not contain a device with PCI ID Bus 00, Device 07, Function 3, any program that polls for PCI devices will receive a partial response at that address. If the program is not able to recover from that partial response it may cause the computer to lock up.

IMPLICATION: The user may have to reboot the computer after running a PCI diagnostic program. This is only known to affect the proprietary PCI diagnostic program PCI.EXE. Intel does not know of any application program subject to this erratum.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

9. Audio IRQ May Not Function Correctly After Boot

PROBLEM: The reset logic in the audio CODEC may leave the IRQ asserted, rather than tri-stated, when the computer is turned on.

IMPLICATION: If the onboard audio is enabled, the CODEC will not be able to signal an interrupt request until the part is reset to bring the IRQ signal to its high impedance state. If the onboard audio is disabled, another device attempting to use the IRQ that the audio codec responds to may not be able to force a low to high transition of the signal in order to generate an interrupt request. This erratum has only been seen in a test environment.

WORKAROUND: None.

STATUS: This erratum applies only to revisions of PBA 666578.

This erratum was fixed in BIOS revision 1.00.06.DL0.

This erratum is fixed in the following versions of the audio drivers:

Driver revision 3.02 or later for OS/2*
Driver revision 3.01 or later for Windows* 95
Driver revision 3.02 or later for Windows 3.11
Driver revision 3.02 or later for Windows NT*

This erratum may be fixed either by upgrading the system BIOS or by upgrading the audio drivers.

10 Slave on Secondary IDE Channel Is Not Disabled

PROBLEM: If the IDE Device Configuration option in BIOS Setup is set to disable the secondary IDE slave device, it will not be disabled in the following configuration:

- ATAPI device attached as master to the secondary IDE connector.
- ATAPI device attached as slave to the secondary IDE connector.

IMPLICATION: In the above configuration, any ATAPI device attached as a secondary slave will remain enabled even if the BIOS setting for the secondary slave is set to disabled.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

11. System BIOS Does Not Recognize Bootable USB Devices

PROBLEM: The system BIOS does not recognize a USB keyboard or mouse during a system boot. A USB keyboard or mouse is not recognized until an operating system that supports USB is loaded.

IMPLICATION: 1. The user is not able to use a USB keyboard to enter the BIOS Setup or to respond to error messages that are displayed before an operating system with USB support is loaded.
2. The user is not able to use a USB keyboard or mouse with any operating system that does not have USB support.

WORKAROUND: Use a standard PS/2* style keyboard and mouse in any configuration where input is required before an operating system with USB support is loaded.

STATUS: This erratum will be fixed in a future BIOS revision.

12. Cannot Meet FCC Class B Requirements Using Unshielded USB Cable

PROBLEM: The motherboard will generate excessive electromagnetic radiation on unshielded USB cables, even if no device or a low speed (sub-channel) USB device is attached to the cable.

IMPLICATION: Systems based on this motherboard will not meet FCC Part 15 Class B requirements when unshielded USB cable is used. Although this condition is a violation of the USB v1.0 specification, it is not believed to have any effect on normal USB device operation.

WORKAROUND: Use USB devices with shielded cable that meet the requirements for high speed (fully-rated) USB devices.

STATUS: This erratum will not be fixed.

13. System BIOS May Corrupt Audio Add-In Card EEPROM

PROBLEM: Audio add-in cards using the Yamaha OPL3-SA2 or OPL3-SA3 audio codec have the same hardware identification number that is used by the Yamaha audio device integrated on the motherboard. This causes the system BIOS to inadvertently write information into the audio add-in card's serial EEPROM during system startup, thereby corrupting the audio add-in card's EEPROM contents.

IMPLICATION: The audio add-in card will not operate and no audio will be available.

WORKAROUND: Disable the onboard audio in BIOS Setup before installing an audio add-in card.

STATUS: This erratum will not be fixed.

SPECIFICATION CLARIFICATIONS

1. Advanced Power Management (APM) Will Not Function as Expected with Universal Serial Bus (USB) Enabled

The following will be added to Section 3.7, Advanced Power Management:

Advanced Power Management will not function as expected when a USB keyboard or mouse is used. USB activity is not monitored by the APM event counter, therefore, activity from a USB keyboard or mouse will not keep the system awake or bring a system out of APM sleep mode. If a USB keyboard or mouse is being used, APM should be disabled.

2. PCI 2.1 Specification Optional Features

The following will be added to Section 1.10.11, PCI/ISA Riser Connectors:

The following optional features in the PCI 2.1 Specification are not implemented on the RU430HX motherboard:

- Cache Support Pins **SBO#** and **SDONE** (Section 2.2.7)
- **PRSNTx#** (Section 2.2.8)
- **CLKRUN#** (Section 2.2.8)
- 64 Bit Bus Extension Pins (Section 2.2.9)
- 66 MHz support (Section 2.2.8)
- JTAG/Boundary scan (Section 2.2.10)

3. Administrator and User Passwords

The following will be added to Section 3.12.11.1, Administrative and User Access Modes:

If an administrator password has been set, but no user password has been set, a user can create a password by entering BIOS Setup at boot by pressing the <F1> key and pressing enter at the administrator password prompt. Once in BIOS Setup, a user will be able to create a new user password.

Once defined, a user password can be cleared by either defining a new user password in Setup, or by moving the Password Clear jumper (J1K2-A) on the motherboard. See Section 1.11.2, Password Clear, for more information on how to use this jumper.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *RU430HX Motherboard Technical Product Specification* (Order Number 281810). All Documentation Changes will be incorporated into a future version of the appropriate RU430HX motherboard documentation.

1. Correction to BIOS Identifier

The inside front cover which reads “This product specification applies only to standard Advanced/RU LPX motherboards with BIOS identifier 1.00.01.RU” will be changed to read “This product specification applies only to standard Advanced/RU LPX motherboards with BIOS identifiers shown in Table 13, BIOS Extensions.”

2. Corrections to Board Feature Drawing

The legend of Table 1, Board features, will be changed as follows:

“D - S3* V+ or ViRGE* PCI graphics controller” will be changed to read “D - S3 Trio* 64, V+ or ViRGE PCI graphics controller”

“CC - Flash Recovery jumper” will be changed to read “CC - Flash Recovery jumper (option)“

3. Add Parity/ECC Setup Option to System Memory Description

Section 1.5.1, System Memory, will be changed to add the following as the last sentence of paragraph 1:

“When parity SIMM*s are installed, a BIOS Setup option provides choices for Error Detection only (parity) or Error Correction (ECC).”

4. Refer to Summary Table of Changes

5. Add Note to Table of Riser Connector Signal Descriptions

Section 1.10.11, the table showing signal definitions for the PCI/ISA Riser Connector, will be changed by adding the following note at the end of the table:

“Note: J5G1 Riser Configuration Jumper must be set for either two or three PCI riser card slots to ensure correct clock signal routing. For two PCI slots, set jumpers to positions 1-2 and 4-5. For three PCI slots, set jumpers to positions 2-3 and 5-6.

6. Refer to Summary Table of Changes

7. Add Manufacturing Options for On-board Audio

Section 1.10.16.1, Audio I/O Connector, will be changed by adding the following as paragraph 2:

"There are two manufacturing options for on-board audio. When the rear panel jacks are installed, the MIDI/Audio Upgrade connector (J9G2) pins 1-16 only are available for MIDI and game port support. When the rear panel jacks are not installed, pins 1-34 of J9G2 are available including line in and out. The microphone preamp is not installed on the baseboard in this configuration."

8. Add Table 13 to Section 3.3, BIOS Upgrades

Table 13. BIOS Extensions

BIOS Extension	Baseboard Configuration
CW0	V+ graphics, 60 ns Video DRAM, 1 Mbit flash memory
DC0	ViRGE* graphics, 50 ns Video DRAM, 1 Mbit flash memory
DL0	V+ graphics with 60 ns video DRAM or Virge graphics with 50 ns video DRAM, 2 Mbit flash memory

9. Change Overview of Setup Menu Screens

Table 14. Overview of the Setup Menu Screens, will be changed to read as follows:

Setup Menu Screen	Description
Main	For setting up and modifying some of the basic options of a PC, such as time, date, diskette drives, hard drives.
Advanced	For modifying the more advanced features of a PC, such as peripheral configuration, audio and advanced chipset configuration.
Security	For specifying passwords that can be used to limit access to the system.
Exit	For saving or discarding changes.
Setup Subscreen	**Description**
Floppy Options	For configuring your diskette drives.
IDE Device Configuration	For configuring your IDE devices.
Boot Options	For modifying options that affect the system boot up, such as the boot sequence.
Peripheral Configuration	For modifying options that affect the serial ports, the parallel port, and the disk drive interfaces.

Table 14. Overview of the Setup Menu Screens (Cont'd)

Setup Subscreen	Description
Audio Configuration	For modifying options that affect on-board audio resources.
Advanced Chipset Configuration	For modifying options that affect memory and system busses.
Power Management Configuration	For accessing and modifying Advanced Power Management (APM) options.
Plug and Play Configuration	For modifying options that affect the system's Plug and Play capabilities.

10. Add Audio Configuration Options to Description of Setup Screens

Section 3.12.6.5 will be added as follows:

AUDIO CONFIGURATION

When selected, this brings up the Audio Configuration Subscreen

Section 3.12.8, Audio Configuration Subscreen, will be added as follows:

3.12.8 AUDIO CONFIGURATION SUBSCREEN

This section describes the screens for the Audio Configuration Subscreen.

3.12.8.1 Configuration Mode

Enables you to choose between setting the audio configuration yourself, or having the system do it. The options are Disabled, Auto and Manual. The default is Auto.

When Auto is selected, the system peripherals are automatically configured during power up and the options below for cannot be modified. The settings displayed for those options reflect the current state of the hardware. Listed options can be user selected in Manual mode only.

3.12.8.2 SB Base Port Address

Selects the Sound Blaster* Base Port Address. Options are Disabled, 220h, 240h.

3.12.8.3 WSS Base Port Address

Selects the Windows Sound System Base Port Address. Options are Disabled, 530h, E80h, F40h, 604h.

3.12.8.4 MPU401 Base Port Address

Selects the MPU401 Base Port Address. Options are Disabled, 330h, 332h, 334h, 300h.

3.12.8.5 WSS Interrupt

Selects the Windows Sound System Interrupt. Options are Disabled, IRQ 7, IRQ 9, IRQ 10, IRQ 11.

3.12.8.6 SB Play/MPU401 Interrupt

Selects the Sound Blaster Play/MPU401 Interrupt. Options are Disabled, IRQ5, IRQ 7, IRQ 9.

3.12.8.7 WSS Play DMA

Selects the Windows Sound System Playback Direct Memory Access Channel. Options are Disabled, Channel 0, Channel 1, Channel 3.

3.12.8.8 SB Play, WSS Capture DMA

Selects the Sound Blaster* Playback/Windows Sound System Record Direct Memory Access Channel. Options are Disabled, Channel 1.

3.12.8.9 Game Port

Selects the status of the Game Port. Options are Disabled, Enabled, Auto.

11. Refer to Summary Table of Changes

12. Power Consumption

Table 6 in section 1.14 should be replaced with the following:

		DC (amps)			
	AC (watts)	**+5 V**	**-5 V**	**+12 V**	**-12 V**
No APM enabled					
DOS prompt	37.6	4.26	.10	.10	.05
APM enabled					
DOS prompt (sleep)	21.6	1.75	.03	.08	.05
No APM enabled					
Windows* 95	36.1	3.46	.10	.10	.10
APM Enabled					
Windows 95	27.4	2.26	.07	.08	.01

13. Regulatory Compliance

Section 1.15 should contain the following information:

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system:

SAFETY

UL 1950 - CSA 950-95, 3rd edition, dated 3-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)

CSA C22.2 No. 950-93, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

EN 60 950, 2nd Edition, 1992 (with Amendments. 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark & Finland)

EMI

CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

EN 55 022, 1995

Limits and Methods of Measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

EN 50 082-1 (1992)

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3 and -4. (Europe)

VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

FCC Class B

Verified to be within the energy emission limits for Class B digital devices defined in the FCC Rules, Subpart B. (U.S.)

ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

PRODUCT CERTIFICATION MARKINGS

European CE Marking

CE Marking on the board.

UL Recognition

UL Recognized Marking consists of UL File No. E139761 on component side of board, PB No. on solder side of board. Board material flammability traceabiltiy markings.

Canadian Compliance

Marking consists of small c followed by a stylized backward UR on component side of board.

14. Refer to Summary Table of Changes

15 Addition of Connector Descriptions to Section 1.10

The following table with pinout descriptions of the Serial 2 stake connector will be added following 1.10.12 and following sections will be renumbered as necessary:

SERIAL PORT CONNECTOR (J5H1)

Serial B (Stake)	Signal Name
P1	DCD
P3	Serial In #
P5	Serial Out #
P7	DTR#
P9	GND
P2	DSR#
P4	RTS#
P6	CTS#
P8	RI
P10	Key

16 Addition of Jumper Description to Section 1.11

The following row will be added to Table 3, Configuration Jumper Settings:

Number of PCI slots on the expansion riser card	J5G1	1-2 & 4-5 2 slots (Default) 2-3 & 5-6 3 slots

The following jumper description will be added as Section 1.11.6:

NUMBER OF PCI RISER SLOTS (J5G1)

This jumper block must be changed to reflect the number of PCI slots on the expansion riser card. Pins 1-2 and 4-5 are jumpered for a 2 slot card. (This is the default configuration.) Pins 2-3 and 5-6 are jumpered for a 3 slot card.

17. Revision of Section 1.10.16.3, Wavetable Upgrade

This second paragraph in this section will be replaced in its entirety as follows:

Compatible wavetable cards are available from several vendors.

18. Revision of Section 1.11.3, Clear CMOS Jumper

This section will be replaced in its entirety as follows:

Allows CMOS settings to be reset to default values by moving the jumper from pins 4-5 to pins 5-6 and turning the system on. When the system reports that “NVRAM cleared by jumper”, the system can be turned off, and the jumper should be returned to the 4-5 position to restore normal operation. Default is for this jumper to be on pins 4-5.

Caution: This procedure should only be done if, after a BIOS update, the system does not boot to a point where BIOS Setup can be entered or if, after CMOS default settings have been restored from within the Setup program, the system does not boot to the operating system.