# SR440BX Motherboard
## Technical Product Specification

**intel** ®

# Revision History

| Revision | Revision History | Date |
|----------|------------------|------|
| -001 | First release of the SR440BX Motherboard Technical Product Specification | February 1999 |
| | | |

This product specification applies only to standard SR440BX motherboards with BIOS identifier 4S4RB0XA.86A.

Changes to this specification will be published in the SR440BX Motherboard Specification Update before being incorporated into a revision of this document.

# Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the SR440BX motherboard. It describes the standard motherboard product and available manufacturing options.

## Intended Audience

The TPS is intended to provide detailed, technical information about the motherboard and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

## What This Document Contains

| Chapter | Description |
|---------|-------------|
| 1 | A description of the hardware used on this board |
| 2 | A map of the resources of the board |
| 3 | The features supported by the BIOS Setup program |
| 4 | The contents of the BIOS Setup program's menus and submenus |
| 5 | A description of the BIOS error messages, beep codes, and POST codes |
| 6 | A list of where to find information about specifications supported by the motherboard |

## Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

### Notes, Cautions, and Warnings

⇒ **NOTE**

*Notes call attention to important information.*

⚠ **CAUTION**

*Cautions are included to help you avoid damaging hardware or losing data.*

⚠ **WARNING**

*Warnings indicate conditions which, if not observed, can cause personal injury.*

# Other Common Notation

| | |
|---|---|
| # | Used after a signal name to identify an active-low signal (such as USBP0#). |
| (NxnX) | When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the motherboard, and X is the instance of the particular part at that general location.  For example, J5J1 is a connector, located at 5J.  It is the first connector in the 5J area. |
| KB | Kilobyte (1024 bytes) |
| Kbit | Kilobit (1024 bits) |
| MB | Megabyte (1,048,576 bytes) |
| Mbit | Megabit (1,048,576 bits) |
| GB | Gigabyte (1,073,741,824 bytes) |
| xxh | An address or data value ending with a lowercase h indicates a hexadecimal value. |
| x.x V | Volts.  Voltages are DC unless otherwise specified. |
| † | This symbol is used to indicate third-party brands and names that are the property of their respective owners. |

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# 6   Specifications and Customer Support

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# 1    Motherboard Description

## What This Chapter Contains

# 1.1  Overview

The SR440BX motherboard is available with the following features:

| Feature | |
|---|---|
| **Form Factor** | microATX: 9.6 x 9.6 inches |
| **Expansion Slots** | Three dedicated PCI slots<br>One shared ISA/PCI slot |
| **Microprocessor** | Support for the following processors:<br>• Intel® Pentium® III processor with 100-MHz host bus speed<br>• Intel® Pentium II processor with 66-MHz or 100-MHz host bus speed<br>• Intel® Celeron™ processor with 66-MHz host bus speed |
| **Main Memory** | Two 168-pin dual inline memory module (DIMM) sockets<br>Supports up to 512 MB of 66 MHz or 100 MHz synchronous DRAM (SDRAM)<br>Supports Error Checking and Correcting (ECC) and non-ECC memory |
| **Chipset** | Intel® 82440BX, consisting of:<br>• Intel® 82443BX PCI/AGP controller (PAC)<br>• Intel® 82371EB PCI ISA IDE Xcelerator (PIIX4E) |
| **I/O Control** | SMSC FDC37M807 Super I/O controller |
| **Peripheral Interfaces** | • Two serial ports<br>• Two Universal Serial Bus (USB) ports<br>• One parallel port<br>• Two IDE interfaces with Ultra DMA support<br>• Single diskette drive |
| **Video** | • NVIDIA† RIVA TNT† Enhanced 128-Bit 3D Processor<br>• 16 MB SDRAM video memory<br>• VIP video side port (optional) |
| **Audio** | AC '97 Crystal CS4297 audio codec<br>Sound Blaster† AudioPCI 64V digital audio controller |
| **BIOS** | • Intel/AMI BIOS<br>• Intel® E28F004B5 4 Mbit boot block flash memory<br>• Support for SMBIOS, Advanced Power Management (APM), Advanced Configuration and Power Management Interface (ACPI), and Plug and Play (see Section 6.2 for specification compliance levels) |
| **Other Features** | • Speaker<br>• Hardware monitor (optional)<br>• Wake on Ring<br>• Wake on LAN† technology (optional)<br>• SCSI LED connector (optional) |

# 1.2 Motherboard Layout

Figure 1 shows the location of the major components on the motherboard.
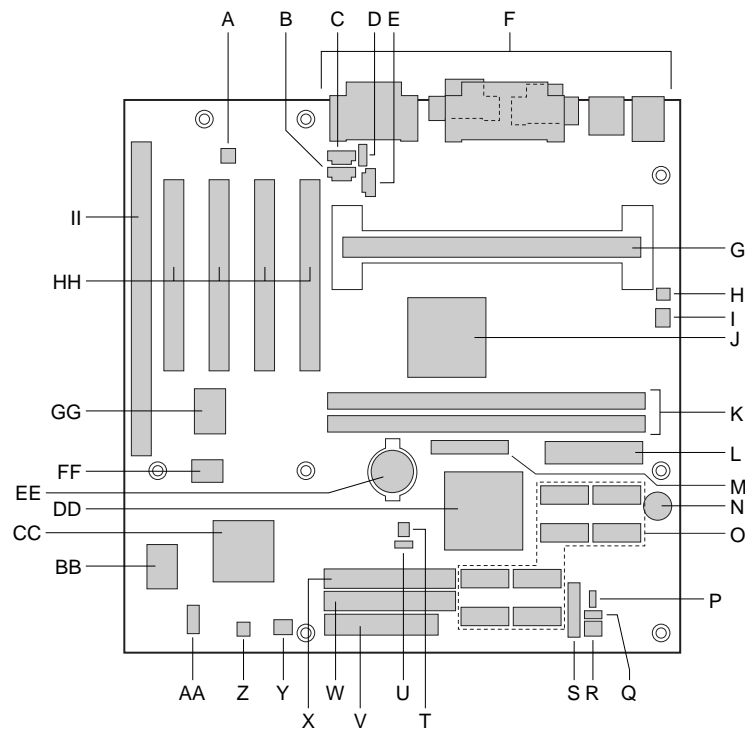


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| | | | |
|---|---|---|---|
| A | CS4297 audio codec | S | Front panel connector |
| B | Auxiliary line in connector | T | SCSI LED connector (optional) |
| C | Telephony connector | U | Configuration jumper block |
| D | Legacy-style CD-ROM connector | V | Diskette drive connector |
| E | ATAPI-style CD-ROM connector | W | Primary IDE connector |
| F | Back panel connectors | X | Secondary IDE connector |
| G | Processor connector | Y | Fan 2 (system) connector |
| H | Chassis intrusion connector (optional) | Z | Wake on Ring connector |
| I | Fan 3 (processor) connector | AA | Serial port B connector (optional) |
| J | Intel 82443BX PAC | BB | SMSC I/O controller |
| K | DIMM sockets | CC | Intel 82371EB PIIX4E |
| L | Power supply connector | DD | Graphics controller |
| M | VIP video connector (optional) | EE | Battery |
| N | Speaker | FF | Flash memory |
| O | SDRAM video memory | GG | Sound Blaster Audio PCI 64V audio controller |
| P | Front panel LED connector | HH | PCI connectors |
| Q | Wake on LAN technology connector (optional) | II | ISA connector |
| R | Fan 1 (power supply) connector (optional) | | |

**Figure 1. Motherboard Components**

Figure 2 is a block diagram of the SR440BX motherboard.
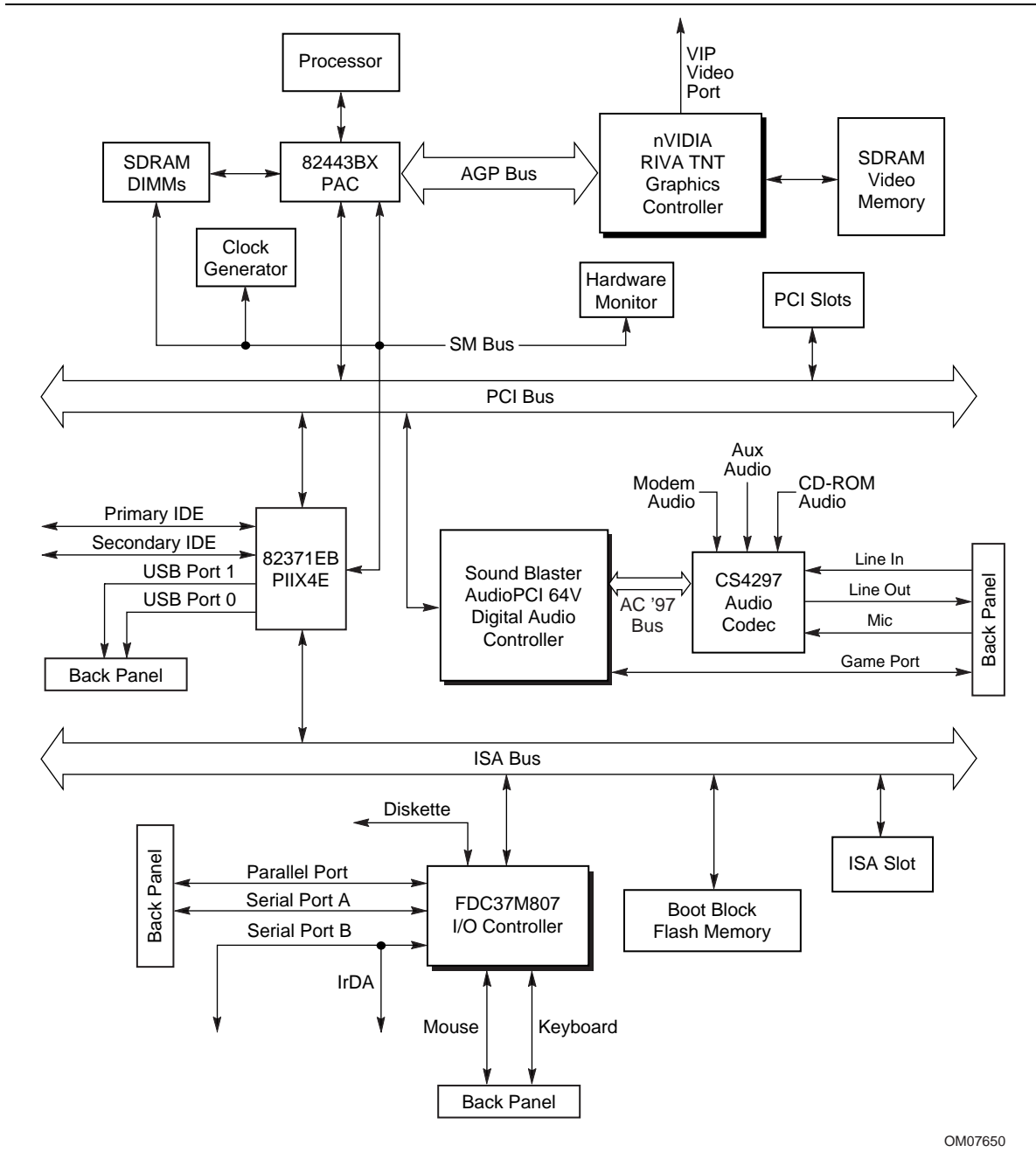


**Figure 2.  Motherboard Block Diagram**

## 1.3 Processor

The motherboard supports a single Pentium III, Pentium II, or Celeron processor.  The host bus speed (66 MHz or 100 MHz) is automatically selected. The processor connects to the motherboard through the 242-contact slot connector.  The processor must be secured by a retention mechanism attached to the motherboard.

⚠️ **CAUTION**

*The motherboard supports Pentium III processors with a 100-MHz host bus, Pentium II processors with a 100- or 66-MHz host bus, and Celeron processors with a 66-MHz host bus.  Processors with a 100-MHz host bus should be used only with 100-MHz SDRAM; the motherboard may not operate reliably if a processor with a 100-MHz host bus is paired with 66-MHz SDRAM.  However, processors with a 66-MHz host bus can be used with either 66-MHz or 100-MHz SDRAM.*

The motherboard supports the processors listed in Table 1.

**Table 1.    Processors Supported by the Motherboard**

| Processor Type | Processor Speed | Host Bus Frequency | L2 Cache Size | Package Type |
|---|---|---|---|---|
| Pentium II processor | 233 | 66 MHz | 512 KB | Single Edge Contact cartridge |
| | 266 | 66 MHz | 512 KB | |
| | 300 | 66 MHz | 512 KB | |
| | 333 | 66 MHz | 512 KB | |
| | 350 | 100 MHz | 512 KB | |
| | 400 | 100 MHz | 512 KB | |
| | 450 | 100 MHz | 512 KB | |
| Pentium III processor | 450 | 100 MHz | 512 KB | Single Edge Contact cartridge |
| | 500 | 100 MHz | 512 KB | |
| Celeron processor | 266 | 66 MHz | None | Single Edge Processor package |
| | 300 | 66 MHz | None | |
| | 300A | 66 MHz | 128 KB | |
| | 333 | 66 MHz | 128 KB | |
| | 366 | 66 MHz | 128 KB | |
| | 400 | 66 MHz | 128 KB | |

For processors with L2 cache, all supported onboard memory can be cached.

## 1.4 System Memory

The motherboard has two DIMM sockets. The minimum memory size is 16 MB and the maximum memory size is 512 MB. The BIOS automatically detects memory type, size, and speed. Memory can be installed in one or both sockets. Memory size can vary between sockets.

➡ **NOTE**

*Processors with 100 MHz host bus should be paired only with 100 MHz SDRAM. Processors with 66 MHz host bus can be paired with either 66 MHz or 100 MHz SDRAM.*

The motherboard supports the following memory features:

- 168-pin DIMMs with gold-plated contacts
- 66 and 100 MHz (matching host bus speed) unbuffered SDRAM only
- Non-ECC (64-bit) and ECC (72-bit) memory
- 100 MHz memory shall be Serial Presence Detect (SPD) memory; 66 MHz may be either SPD or non-SPD
- 3.3 V memory only
- Single- or double-sided DIMMs in the following sizes:

| DIMM Size | Non-ECC Configuration | ECC Configuration |
|-----------|----------------------|-------------------|
| 16 MB | 2 Mbit x 64 | 2 Mbit x 72 |
| 32 MB | 4 Mbit x 64 | 4 Mbit x 72 |
| 64 MB | 8 Mbit x 64 | 8 Mbit x 72 |
| 128 MB | 16 Mbit x 64 | 16 Mbit x 72 |
| 256 MB | 32 Mbit x 64 | 32 Mbit x 72 |

When ECC memory is installed, the BIOS supports both ECC and non-ECC mode. ECC mode is enabled in the Setup program. The BIOS automatically detects if ECC memory is installed and provides the Setup option for selecting ECC mode. If any non-ECC memory is installed, the Setup option for ECC mode does not appear and ECC operation is not available.

The following table describes the effect of using Setup to put each memory type in each supported mode:

| | Memory Error Detection Mode Established in Setup Program | |
|---|---|---|
| | ECC Disabled | ECC Enabled |
| Non-ECC DIMM | No error detection | N/A |
| ECC DIMM | No error detection | Single-bit error correction, multiple-bit error detection |

Whenever ECC mode is selected in Setup, some performance loss occurs.

⇒ **NOTE**

*All memory components and DIMMs used with the SR440BX motherboard should comply with the PC SDRAM Specifications. These include: the* PC SDRAM Specification *(memory component specific), the* PC Unbuffered SDRAM Specifications, *and the* PC Serial Presence Detect Specification. *See Section 6.2 for information about these specifications.*

## 1.5  Chipset

The Intel 82440BX AGPset consists of the Intel 82443BX PAC and the Intel 82371EB PIIX4E bridge chip.  The PAC provides an optimized DRAM controller and an Accelerated Graphics Port (AGP) interface.  The I/O subsystem of the 82440BX is based on the PIIX4E, which is a highly integrated PCI ISA IDE Xcelerator Bridge.

### 1.5.1  Intel® 82443BX PAC

The Intel 82443BX PAC provides bus-control signals, address paths, and data paths for transfers between the processor's host bus, PCI bus, the AGP, and main memory.  The PAC features:

- Processor interface control
  — Support for processor host bus frequencies of 100 MHz and 66 MHz
  — 32-bit addressing
  — Desktop optimized GTL+ compliant host bus interface
- Integrated DRAM controller, with support for
  — +3.3 V only DIMM DRAM configurations
  — Up to two double-sided DIMMs
  — 100-MHz or 66-MHz SDRAM
  — DIMM serial presence detect via SMBus interface
  — 16- and 64-Mbit devices with 2 KB, 4 KB, and 8 KB page sizes
  — x 4, x 8, x 16, and x 32 DRAM widths
  — SDRAM 64-bit data interface with ECC support
  — Symmetrical and asymmetrical DRAM addressing
- AGP interface
  — Complies with the AGP specification (see Section 6.2 for specification information)
  — Support for AGP 2X device
  — Synchronous coupling to the host bus frequency
- PCI bus interface
  — Complies with the PCI specification +5 V 33-MHz interface (see Section 6.2 for specification information)
  — Asynchronous coupling to the host-bus frequency
  — PCI parity generation support

— Data streaming support from PCI-to-DRAM

— Support for five PCI bus masters in addition to the host and PCI-to-ISA I/O bridge

— Support for concurrent host, AGP, and PCI transactions to main memory

- Data buffering

  — DRAM write buffer with read-around-write capability

  — Dedicated host-to-DRAM, PCI0-to-DRAM, and PCI1/AGP-to-DRAM read buffers

  — AGP dedicated inbound/outbound FIFOs, used for temporary data storage

- Power management functions

  — Support for system suspend/resume (DRAM and power-on suspend)

  — Compliant with ACPI power management

- SMBus support for desktop management functions
- Support for system management mode (SMM)

## 1.5.2   Intel® 82371EB (PIIX4E)

The PIIX4E is a multifunctional PCI device implementing the PCI-to-ISA bridge,
PCI IDE functionality, USB host/hub functionality, and enhanced power management.  The
PIIX4E features:

- Multifunctional PCI-to-ISA bridge

  — Support for the PCI bus at 33 MHz

  — PCI specification-compliant (see Section 6.2 for specification information)

  — Full ISA bus support

- USB controller

  — Two USB ports (see Section 6.2 for specification information)

  — Support for legacy keyboard and mouse

  — Support for Universal Host Controller Interface (UHCI) Design Guide (see Section 6.2 for
    specification information)

- Integrated dual-channel enhanced IDE interface

  — Support for up to four IDE devices

  — PIO Mode 4 transfers at up to 16 MB/sec

  — Support for Ultra DMA/33 synchronous DMA mode transfers at up to 33 MB/sec

  — Bus master mode with an 8 x 32-bit buffer for bus master PCI IDE burst transfers

- Enhanced DMA controller

  — Two 8237-based DMA controllers

  — Support for PCI DMA with three PC/PCI channels and distributed DMA protocols

  — Fast type-F DMA for reduced PCI bus usage

- Interrupt controller based on 82C59

  — Support for 15 interrupts

  — Programmable for edge/level sensitivity

- Power management logic
  — Sleep/resume logic
  — Support for Wake on Ring and Wake on LAN technology
  — Support for APM and ACPI (see Section 6.2 for specification information)
- Real-Time Clock
  — 256-byte battery-backed CMOS SRAM
  — Date alarm
- 16-bit counters/timers based on 82C54

## 1.5.3 USB

The motherboard has two USB ports; one USB peripheral can be connected to each port. For more than two USB devices, an external hub can be connected to either port. The two USB ports are implemented with stacked back panel I/O connectors. The motherboard fully supports UHCI and uses UHCI-compatible software drivers. See Section 6.2 for information about the USB and UHCI specifications.

- Self-identifying peripherals that can be plugged in while the computer is running
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices
- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error-handling and fault-recovery mechanisms built into the protocol

⇒ **NOTE**

*Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.*

## 1.5.4 IDE Support

The motherboard has two independent bus-mastering IDE interfaces. These interfaces support:

- ATAPI devices (such as CD-ROM drives)
- ATA devices using the transfer modes listed in Table 62 on page 80.

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The motherboard supports laser servo (LS-120) diskette technology through its IDE interfaces. LS-120 diskette technology enables users to store 120 MB of data on a single, 3.5-inch removable diskette. LS-120 technology is backward-compatible (both read and write) with 1.44 MB and 720 KB DOS-formatted diskettes and is supported by the Windows† 95, Windows 98, and Windows NT† operating systems. The LS-120 drive can be configured as a boot device, if selected in the BIOS Setup program.

## 1.5.5   Real-Time Clock, CMOS SRAM, and Battery

The real-time clock is compatible with DS1287 and MC146818 components. The clock provides a time-of-day clock and a multicentury calendar with alarm features and century rollover. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the 3.3 V standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the Setup program. The CMOS values can be returned to their defaults by using the Setup program.

⇒ **NOTE**

*The recommended method of accessing the date in systems with Intel® motherboards is indirectly from the Real Time Clock (RTC) via the BIOS. The BIOS on Intel motherboards and baseboards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.*

*For more information on proper date access in systems with Intel motherboards, please see:* http://support.intel.com/support/year2000/

# 1.6   I/O Controller

The FDC37M807 I/O controller from SMSC is an ISA Plug and Play-compatible, multifunctional I/O device that provides the following features (see Section 6.2 for Plug and Play information):

- Two serial ports
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Three-mode diskette drive support (driver required)
- FIFO support on both serial and diskette drive interfaces
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- PS/2[†]-style mouse and keyboard interfaces
- Support for serial IRQ packet protocol
- Intelligent autopower management, including:
  — Shadowed write-only registers for ACPI compliance
  — Programmable wake up event interface

The BIOS Setup program provides configuration options for the I/O controller.

### 1.6.1   Serial Ports

The motherboard has one 9-pin D-Sub serial port connector located on the back panel and an optional connector on the board for a second serial port. The serial ports' NS16C550-compatible UARTs support data transfers at speeds up to 115.2 Kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h)

### 1.6.2   Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-Sub connector located on the back panel. In the Setup program, the parallel port can be configured for the following:

- Output only
- Bidirectional (PS/2 compatible)
- EPP
- ECP

### 1.6.3   Diskette Drive Controller

The I/O controller supports a single diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT[†] and PS/2 modes. In the Setup program, the diskette drive interface can be configured for the following diskette drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

⇒ **NOTE**

*The I/O controller supports 1.2 MB, 3.5-inch diskette drives, but a special driver is required for this type of drive (three-mode).*

### 1.6.4   Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch[†] circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

⇒ **NOTE**

*The mouse and keyboard can be plugged into either of the PS/2 connectors. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.*

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power on/reset. A power on/reset password can be specified in Setup.

The keyboard controller also supports the hot-key sequence <Ctrl><Alt><Del> for a software reset. This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-On Self Test (POST).

# 1.7 AGP Graphics Subsystem

The onboard AGP graphics subsystem supports graphics-intensive applications, such as 3D applications. AGP, while based on the PCI bus, is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amount of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent bus efficiency

For more information on the AGP, please refer to the *Accelerated Graphics Port Interface Specification* listed in Section 6.2.

The graphics subsystem features the NVIDIA RIVA TNT Enhanced 128-Bit 3D Processor, 8 or 16 MB of SDRAM, and an optional video interface port (VIP).

Visit Intel's World Wide Web (see Section 6.1) site for information about graphics drivers.

## 1.7.1 NVIDIA RIVA TNT Graphics Controller

The NVIDIA RIVA TNT graphics controller is paired with 16 MB of SDRAM video memory and features:

- 2x AGP graphics support
- Single pass multitexture rendering achieved by processing two pixels per clock cycle
- Optimization for Direct3D[†] acceleration with complete DirectX[†] 5.0 and 6.0 support
- High-performance, 128-bit 2D/GUI/DirectDraw[†] acceleration
- Video acceleration for DirectShow[†], MPEG-1, MPEG-2, and Indeo® video technology
- Support for Media Port Controller (MPC) polling protocol

Table 2 lists the refresh rates supported by the SR440BX motherboard.

**Table 2.    NVIDIA RIVA TNT Refresh Rates**

| Resolution | Refresh Rates (Hz) at 8 and 16 bpp | Max. Refresh Rate (Hz) at 32 bpp * |
|---|---|---|
| 320 x 200 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 320 x 240 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 480 x 360 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 512 x 384 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 640 x 400 | 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240** |
| 640 x 480 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 800 x 600 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200, 240 | 240 |
| 960 x 720 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200 | 170 |
| 1024 x 768 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150, 170, 200 | 150 |
| 1152 x 864 | 60, 70, 72, 75, 85, 100, 120, 140, 144, 150 | 120 |
| 1280 x 1024 | 60, 70, 72, 75, 85, 100, 120 | 100 |
| 1600 x 1200 | 60, 70, 72, 75, 85 | 70 |
| 1920 x 1080 | 60, 70, 72, 75 | 60 |
| 1920 x 1200 | 60, 70, 72, 75 | 60 |

\*    All lower refresh rates are also supported.

\*\*    All lower refresh rates except 60 Hz are also supported.

## 1.7.2   Video Interface Port (Optional)

The Video Interface Port (VIP) is an optional interface between video-enabled graphics controllers and one or more video devices, such as video decoders.  VIP features:

- Backward compatibility with the VESA† Feature Connector
- Simplified ITU-CCIR-656 Video Format which supports horizontal (HSYNC) and vertical (VSYNC), odd and even video field
- Plug-and-play support through the graphics controller's AGP interface
- Variable resolutions and scan rates and interlaced and non-interlaced video
- Support for Media Port Controller (MPC) polling protocol

# 1.8  Audio Subsystem

The Audio Codec '97 (AC '97) compatible audio subsystem includes these features:

- Two chip split digital/analog architecture for improved S/N (signal-to-noise) ratio ($\geq$ 85 dB) measured at line out, from any analog input, including line in, CD-ROM, and auxiliary line in
- 3-D stereo enhancement

Power management support for APM 1.2 and ACPI 1.0 The audio subsystem consists of these devices:

- Sound Blaster AudioPCI 64V audio controller
- Crystal Semiconductor CS4297 stereo audio codec
- Audio connectors

### 1.8.1   Sound Blaster AudioPCI 64V Audio Controller

- Interfaces to PCI bus as a Plug and Play device
- DOS legacy compatible
- Access to main memory (through the PCI bus) for wavetable synthesis support – does not require a separate wavetable ROM device
- PC 98 compliant

### 1.8.2   Crystal Semiconductor CS4297 Stereo Audio Codec

- High performance 18-bit stereo full-duplex audio codec with up to 48 kHz sampling rate
- Connects to the Sound Blaster AudioPCI 64V using a five-wire digital interface

### 1.8.3   Audio Connectors

The audio connectors include the following:

- CD-ROM (ATAPI-style and legacy-style 2 mm connectors)

- ATAPI-style connectors

   — CD-ROM audio

   — Auxiliary line in

   — Telephony

- Back panel connectors

   — Line out

   — Line in

   — Mic in

   — MIDI/Game Port

⟹ **NOTE**

*The Line out connector, located on the back panel, is designed to power headphones or amplified speakers only.  Poor audio quality may occur if passive (non-amplified) speakers are connected to this output.*

#### 1.8.3.1   CD-ROM Audio Connectors

The motherboard contains two CD-ROM audio connectors to connect an internal CD-ROM drive to the audio mixer:

- A 1 x 4 legacy-style 2 mm connector
- A 1 x 4-pin ATAPI connector

⟹ **NOTE**

*Since both CD-ROM connectors connect to the same motherboard circuitry, they should not be used simultaneously.*

### 1.8.3.2  Auxiliary Line In

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

### 1.8.3.3  Telephony

A 1 x 4-pin ATAPI-style connector connects the monoaural audio signals of an internal telephony device to the audio subsystem.  A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modems, and answering machines.

## 1.8.4  Audio Drivers and Utilities

Audio software and utilities are available from Intel's World Wide Web site (see Section 6.1)

# 1.9  Hardware Monitor (Optional)

The optional hardware monitor subsystem provides low-cost instrumentation capabilities.  The features of the hardware monitor subsystem include:

- Support for an optional chassis intrusion connector
- An integrated ambient temperature sensor
- Fan speed sensors (see Section 1.15.2 for the location of these connectors on the motherboard)
- Power supply voltage monitoring to detect levels above or below acceptable values

When suggested ratings for temperature, fan speed, or voltage are exceeded, an interrupt is activated.  The hardware monitor component connects to the SMBus.

# 1.10  SCSI Hard Drive LED Connector (Optional)

The optional SCSI hard drive LED connector is a 1 x 2-pin connector that allows an add-in SCSI controller to use the same LED as the IDE controller.  This connector can be connected to the LED output of the add-in controller card.  The LED will indicate when data is being read or written using the add-in controller.  See Section 1.15.2 for the location and pinouts of the SCSI hard drive LED connector.

## 1.11  Wake on LAN Technology (Optional)

Wake on LAN technology enables remote wakeup of the computer through a network.  Wake on LAN technology requires a PCI add-in network interface card (NIC) with remote wakeup capabilities.  The remote wakeup connector on the NIC must be connected to the motherboard Wake on LAN technology connector.  The NIC monitors network traffic at the MII interface; upon detecting a Magic Packet†, the NIC asserts a wakeup signal that powers up the computer.  To access this feature, use the optional Wake on LAN technology connector on the motherboard.  See Section 1.15.2 for the location and pinouts of the Wake on LAN technology connector.

⚠ **CAUTION**

*For Wake on LAN technology, the 5-V standby line for the power supply must be capable of delivering +5 V ±5 % at 720 mA.  Failure to provide adequate standby current when implementing Wake on LAN technology, can damage the power supply.*

## 1.12  Wake on Ring

Wake on Ring enables the computer to wake from sleep or soft-off mode when a call is received on a telephony device, such as a faxmodem, configured for operation on either serial port.  The first incoming call powers up the computer.  A second call must be made to access the computer.  To access this feature use the Wake on Ring connector  See Section 1.15.2 for the location and pinouts of the Wake on Ring connector.

## 1.13  Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the motherboard can turn off the system power through software control.  See Section 6.2 for information about the microATX specification.

To enable soft-off control in software, advanced power management must be enabled in the Setup program and in the operating system.  When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With Last State enabled in the BIOS (see Table 69), if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off).

## 1.14  Speaker

A 47 Ω inductive speaker is mounted on the motherboard.  The speaker provides audible error code (beep code) information during the power-on self test (POST).

# 1.15 Connectors

This section describes the motherboard's connectors. The connectors can be divided into three groups, as shown in Figure 3.



| | |
|---|---|
| A | Back panel I/O connectors (see Section 1.15.1) |
| B | Midboard connectors (see Section 1.15.2) |
| C | Front panel connectors (see Section 1.15.3) |

OM07651
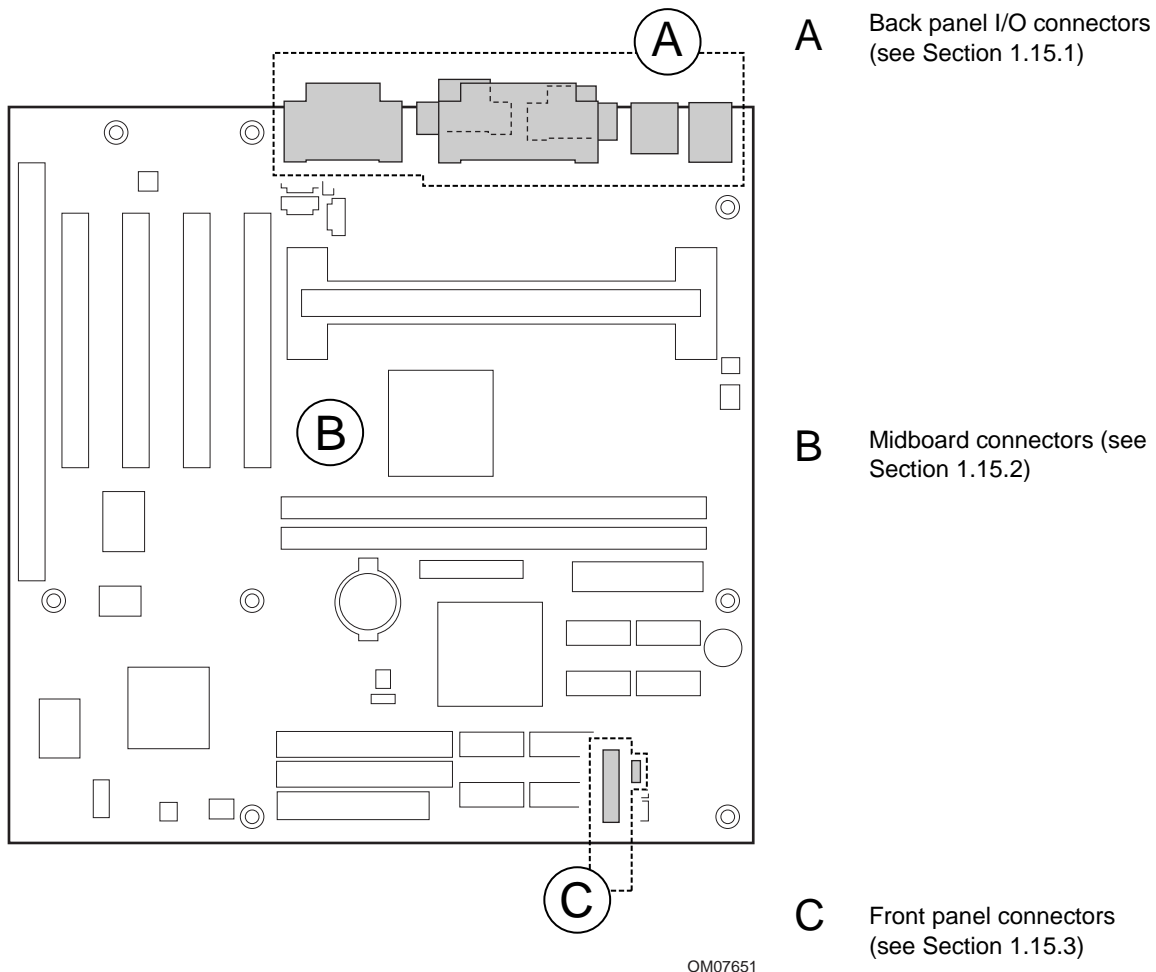
**Figure 3.  Connector Groups**

## ⚠ CAUTION

*Only the back panel connectors of this motherboard have overcurrent protection.  The internal motherboard connectors are not overcurrent protected, and should connect only to devices inside the computer chassis, such as fans and internal peripherals.  Do not use these connectors for powering devices external to the computer chassis.  A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.*

## 1.15.1   Back Panel I/O Connectors

Figure 4 shows the location of the back panel I/O connectors.



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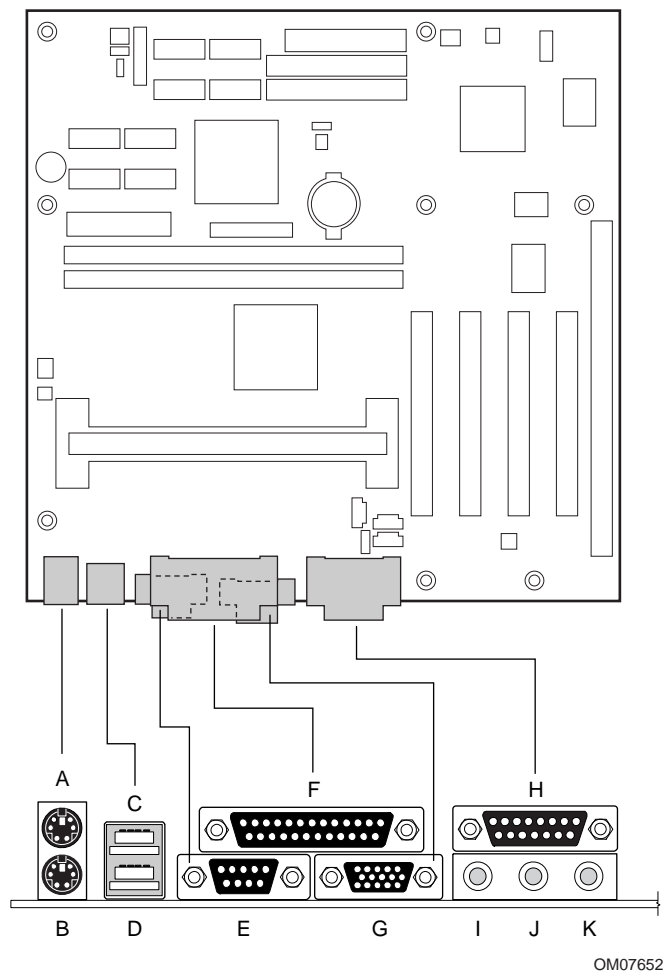
| | | | |
|---|---|---|---|
| A | PS/2 keyboard or mouse | G | VGA |
| B | PS/2 keyboard or mouse | H | MIDI/Game port |
| C | USB port 0 | I | Audio line out |
| D | USB port 1 | J | Audio line in |
| E | Serial port A | K | Mic in |
| F | Parallel port | | |

**Figure 4.  Back Panel I/O Connectors**

**Table 3.     PS/2 Keyboard/Mouse Connectors**

| Pin | Signal |
|-----|--------|
| 1 | Data |
| 2 | Not connected |
| 3 | Ground |
| 4 | Fused +5 V |
| 5 | Clock |
| 6 | Not connected |

**Table 4.     USB Stacked Connector**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | Fused +5 V | 5 | Fused +5 V |
| 2 | 3.3 V differential USB signal USB_D– | 6 | 3.3 V differential USB signal USB_D– |
| 3 | 3.3 V differential USB signal USB_D+ | 7 | 3.3 V differential USB signal USB_D+ |
| 4 | Ground | 8 | Ground |

**Table 5.     Serial Port A Connector**

| Pin | Signal |
|-----|--------|
| 1 | DCD (Data Carrier Detect) |
| 2 | SIN# (Serial Data In) |
| 3 | SOUT# (Serial Data Out) |
| 4 | DTR (Data Terminal Ready) |
| 5 | Ground |
| 6 | DSR (Data Set Ready) |
| 7 | RTS (Request to Send) |
| 8 | CTS (Clear to Send) |
| 9 | RI (Ring Indicator) |

**Table 6.    Parallel Port Connector**

| Pin | Std Signal | ECP Signal | EPP Signal | I/O |
|---|---|---|---|---|
| 1 | STROBE# | STROBE# | WRITE# | I/O |
| 2 | PD0 | PD0 | PD0 | I/O |
| 3 | PD1 | PD1 | PD1 | I/O |
| 4 | PD2 | PD2 | PD2 | I/O |
| 5 | PD3 | PD3 | PD3 | I/O |
| 6 | PD4 | PD4 | PD4 | I/O |
| 7 | PD5 | PD5 | PD5 | I/O |
| 8 | PD6 | PD6 | PD6 | I/O |
| 9 | PD7 | PD7 | PD7 | I/O |
| 10 | ACK# | ACK# | INTR | I |
| 11 | BUSY | BUSY#, PERIPHACK | WAIT# | I |
| 12 | PERROR | PE, ACKREVERSE# | PE | I |
| 13 | SELECT | SELECT | SELECT | I |
| 14 | AUDOFD# | AUDOFD#, HOSTACK | DATASTB# | O |
| 15 | FAULT# | FAULT#, PERIPHREQST# | FAULT# | I |
| 16 | INIT# | INIT#, REVERSERQST# | RESET# | O |
| 17 | SLCTIN# | SLCTIN# | ADDRSTB# | O |
| 18 - 25 | GND | GND | GND | - |

**Table 7.    VGA Connector**

| Pin | Signal |
|---|---|
| 1 | RED |
| 2 | GREEN |
| 3 | BLUE |
| 4 | Not connected |
| 5 | GND |
| 6 | GND |
| 7 | GND |
| 8 | GND |
| 9 | FUSED_+5V |
| 10 | GND |
| 11 | Not connected |
| 12 | MONID1 |
| 13 | HSYNC |
| 14 | VSYNC |
| 15 | MONID2 |

**Table 8.      Audio Line-In Connector**

| Pin | Signal |
| --- | --- |
| Tip | Audio left in |
| Ring | Audio right in |
| Sleeve | Ground |

**Table 9.      Audio Line-Out Connector**

| Pin | Signal |
| --- | --- |
| Tip | Audio left out |
| Ring | Audio right out |
| Sleeve | Ground |

**Table 10.    Audio Mic In Connector**

| Pin | Signal |
| --- | --- |
| Tip | Mono in |
| Ring | Mic bias voltage |
| Sleeve | Ground |

**Table 11.    MIDI/Game Port Connector**

| Pin | Signal Name | Pin | Signal Name |
| --- | --- | --- | --- |
| 1 | +5 V (fused) | 9 | +5 V (fused) |
| 2 | GP4 (JSBUT0) | 10 | GP6 (JSBUT2) |
| 3 | GP0 (JSX1) | 11 | GP2 (JSX2) |
| 4 | Ground | 12 | MIDI-OUT |
| 5 | Ground | 13 | GP3 (JSY2) |
| 6 | GP1 (JSY1) | 14 | GP7 (JSBUT3) |
| 7 | GP5 (JSBUT1) | 15 | MIDI-IN |
| 8 | +5 V (fused) | | |

## 1.15.2   Midboard Connectors

The midboard connectors are divided into the following functional groups:

- Audio/video (see Section 1.15.2.1)
  — Auxiliary line in
  — Telephony
  — CD-ROM
  — VIP (optional)
- Peripheral interfaces (see Section 1.15.2.2)
  — USB front panel
  — SCSI LED (optional)
  — Diskette Drive
  — IDE
  — Serial port B header (optional)
- Hardware Management and Power (see Section 1.15.2.3)
  — Chassis intrusion (optional)
  — Fans
  — Power
  — Wake on Ring
  — Wake on LAN technology (optional)
- Add-in board (see Section 1.15.2.4)
  — ISA bus
  — PCI bus

### 1.15.2.1 Audio/Video

Figure 5 shows the location of the midboard audio/video connectors.
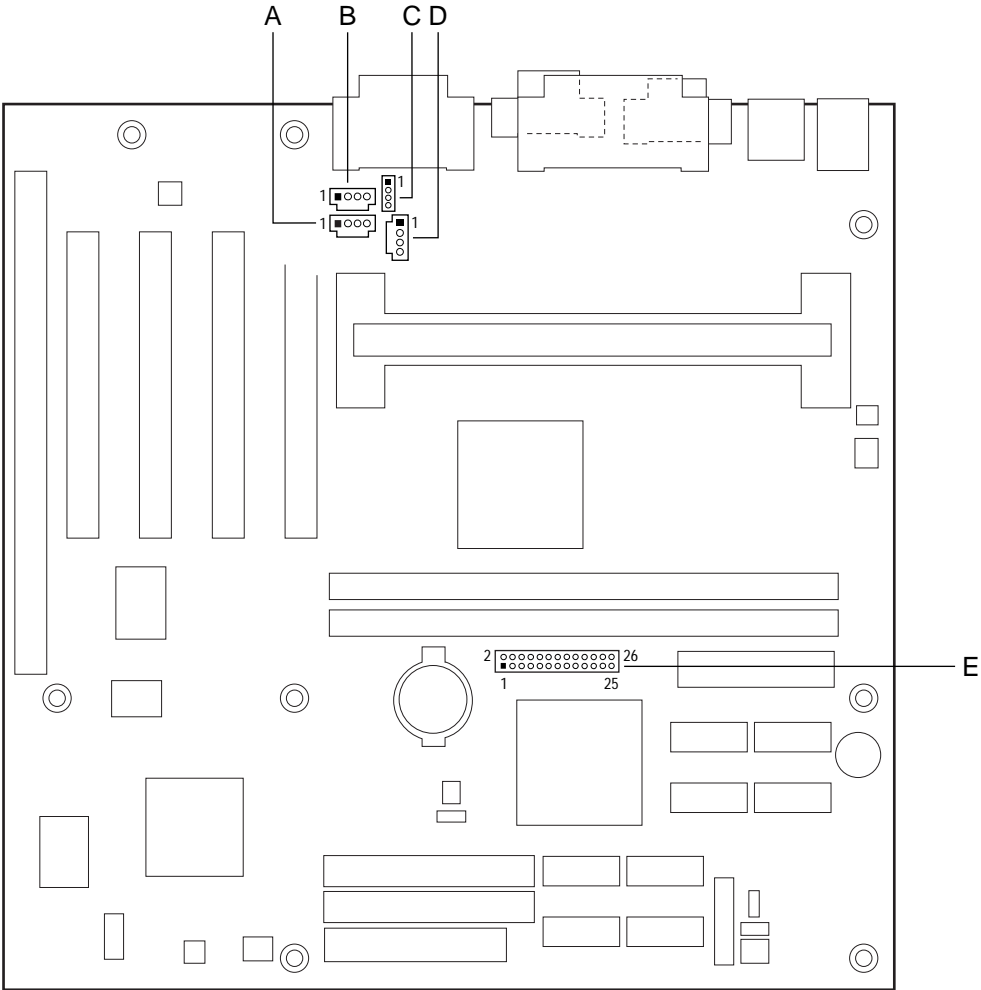


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| A | Auxiliary line in (natural) | D | ATAPI-style CD-ROM (black) |
|---|---|---|---|
| B | Telephony (green) | E | VIP (optional) |
| C | Legacy-style CD-ROM (white) | | |

**Figure 5.  Midboard Audio/Video Connectors**

**Table 12. Auxiliary Line In Connector (natural) (J2D2)**

| Pin | Signal |
|-----|--------|
| 1 | Left auxiliary line in |
| 2 | Ground |
| 3 | Ground |
| 4 | Right auxiliary line in |

**Table 13. Telephony Connector (green) (J2D1)**

| Pin | Signal |
|-----|--------|
| 1 | Analog audio mono input |
| 2 | Ground |
| 3 | Ground |
| 4 | Analog audio mono output |

**Table 14. CD-ROM Connector (ATAPI-style) (black) (J2E1)**

| Pin | Signal |
|-----|--------|
| 1 | Left audio input from CD-ROM |
| 2 | CD audio differential ground |
| 3 | CD audio differential ground |
| 4 | Right audio input from CD-ROM |

**Table 15. CD-ROM Connector (Legacy-style 2 mm) (white) (J1E2)**

| Pin | Signal |
|-----|--------|
| 1 | CD audio differential ground |
| 2 | Left audio input from CD-ROM |
| 3 | CD audio differential ground |
| 4 | Right audio input from CD-ROM |

**Table 16.    VIP Connector (J7G1)**

| VESA Feature Connector | | VIP Mode | VESA Feature Connector | | VIP Mode |
|---|---|---|---|---|---|
| **Pin** | **VESA Signal** | **VIP Signal** | **Pin** | **VESA Signal** | **VIP Signal** |
| 1 | Ground | Ground | 2 | P0 | VID[0] |
| 3 | Ground | Ground | 4 | P1 | VID[1] |
| 5 | Ground | Ground | 6 | P2 | VID[2] |
| 7 | EVIDEO | HAD[1] | 8 | P3 | VID[3] |
| 9 | ESYNC | HAD[0] | 10 | P4 | VID[4] |
| 11 | EDCLK# | HCTL | 12 | P5 | VID[5] |
| 13 | Not connected | SCL | 14 | P6 | VID[6] |
| 15 | Ground | Ground | 16 | P7 | VID[7] |
| 17 | Ground | Ground | 18 | DCLK | PIXCLK |
| 19 | Ground | Ground | 20 | BLANK# | VIPCLK |
| 21 | Ground | Ground | 22 | HSYNC | Not connected |
| 23 | Not connected | VIRQ# | 24 | VSYNC | Not connected |
| 25 | Not connected | SDA | 26 | Ground | Ground |

## 1.15.2.2    Peripheral Interfaces

Figure 6 shows the location of the peripheral interface connectors.



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| | | | | |
|---|---|---|---|---|
| A | Serial port B header (optional) | | D | Diskette drive |
| B | Secondary IDE | | E | SCSI LED (optional) |
| C | Primary IDE | | | |
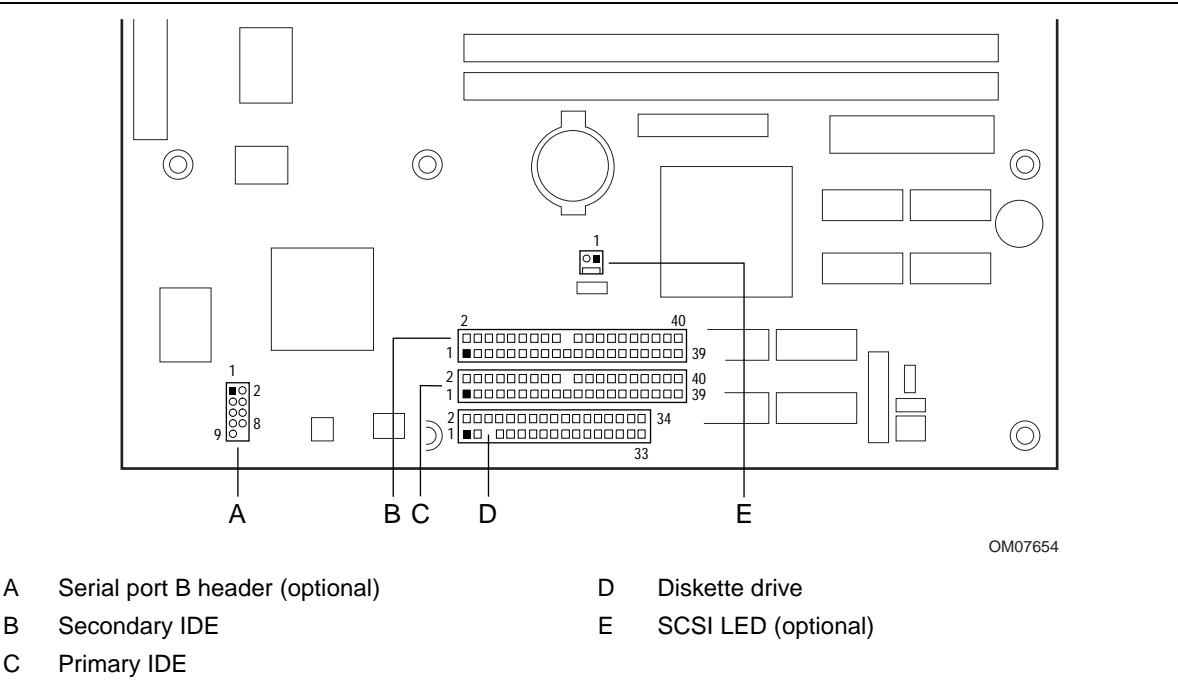
**Figure 6.  Peripheral Interface Connectors**

**Table 17.    SCSI LED Connector (J8E1)**

| Pin | Signal |
|-----|--------|
| 1 | SCSI activity |
| 2 | Not connected |

**Table 18.    Diskette Drive Connector (J10E1)**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | Ground | 2 | DENSEL |
| 3 | Ground | 4 | Reserved |
| 5 | Key | 6 | FDEDIN |
| 7 | Ground | 8 | FDINDX# (Index) |
| 9 | Ground | 10 | FDM00# (Motor Enable A) |
| 11 | Ground | 12 | No connect |
| 13 | Ground | 14 | FDDS0# (Drive Select A) |
| 15 | Ground | 16 | No connect |
| 17 | No connect | 18 | FDDIR# (Stepper Motor Direction) |
| 19 | Ground | 20 | FDSTEP# (Step Pulse) |
| 21 | Ground | 22 | FDWD# (Write Data) |
| 23 | Ground | 24 | FDWE# (Write Enable) |
| 25 | Ground | 26 | FDTRK0# (Track 0) |
| 27 | No connect | 28 | FDWPD# (Write Protect) |
| 29 | Ground | 30 | FDRDATA# (Read Data) |
| 31 | Ground | 32 | FDHEAD# (Side 1 Select) |
| 33 | Ground | 34 | DSKCHG# (Diskette Change) |

**Table 19.   PCI IDE Connectors (J9E2, J9E1)**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | Reset IDE | 2 | Ground |
| 3 | Data 7 | 4 | Data 8 |
| 5 | Data 6 | 6 | Data 9 |
| 7 | Data 5 | 8 | Data 10 |
| 9 | Data 4 | 10 | Data 11 |
| 11 | Data 3 | 12 | Data 12 |
| 13 | Data 2 | 14 | Data 13 |
| 15 | Data 1 | 16 | Data 14 |
| 17 | Data 0 | 18 | Data 15 |
| 19 | Ground | 20 | Key |
| 21 | DDRQ0 [DDRQ1] | 22 | Ground |
| 23 | I/O Write# | 24 | Ground |
| 25 | I/O Read# | 26 | Ground |
| 27 | IOCHRDY | 28 | P_ALE (Cable Select pullup) |
| 29 | DDACK0# [DDACK1#] | 30 | Ground |
| 31 | IRQ 14 [IRQ 15] | 32 | Reserved |
| 33 | DAG1 (Address 1) | 34 | Reserved |
| 35 | DAG0 (Address 0) | 36 | DAG2Address 2 |
| 37 | Chip Select 1P# [Chip Select 1S#] | 38 | Chip Select 3P# [Chip Select 3S#] |
| 39 | Activity# | 40 | Ground |

NOTE:  Signal names in brackets ([ ]) are for the secondary IDE connector (J9E1).

**Table 20.   Serial Port B Connector (J10B1)**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | DCD (Data Carrier Detect) | 2 | DSR (Data Set Ready) |
| 3 | SIN# (Serial Data In) | 4 | RTS (Request to Send) |
| 5 | SOUT# (Serial Data Out) | 6 | CTS (Clear to Send) |
| 7 | DTR (Data Terminal Ready) | 8 | RI (Ring Indicator) |
| 9 | Ground | | |

### 1.15.2.3    Hardware Management and Power

Figure 7 shows the location of the hardware management and power connectors.
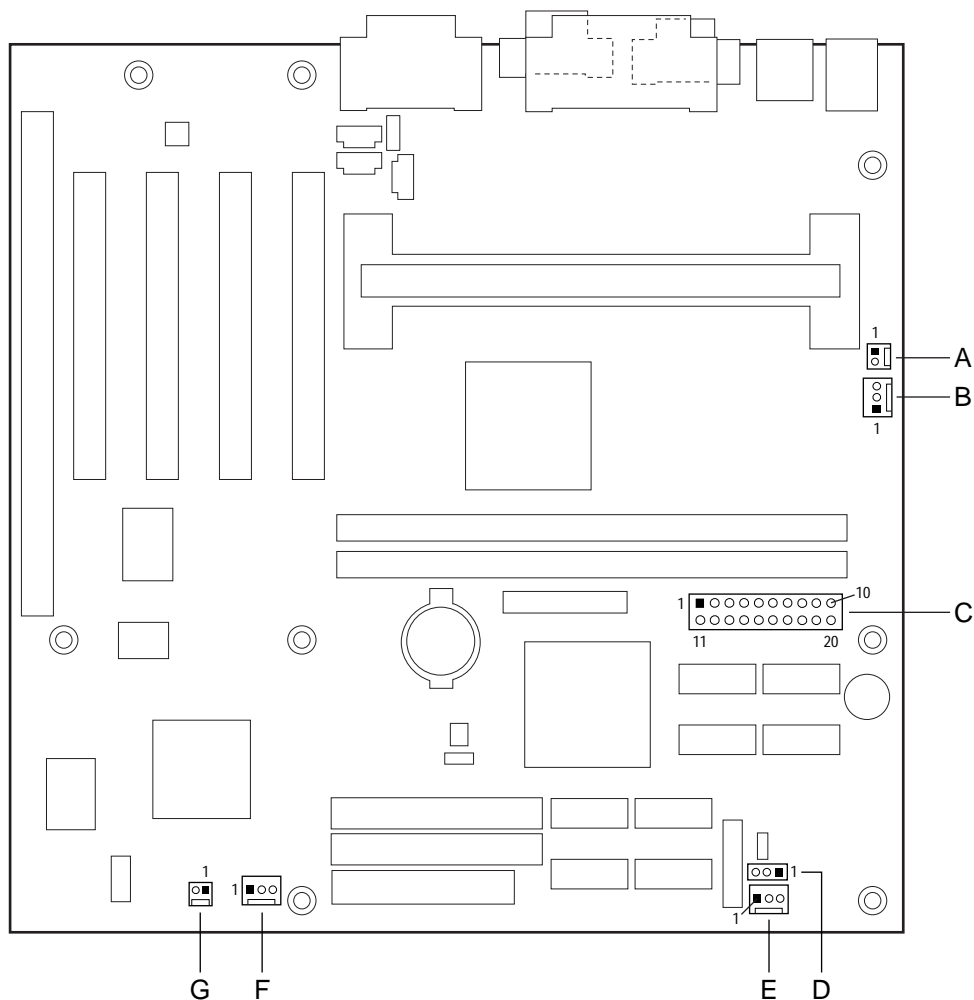


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| A | Chassis intrusion (optional) | E | Fan 1 (power supply fan) (optional) |
|---|---|---|---|
| B | Fan 3 (processor fan) | F | Fan 2 (system fan) |
| C | Power | G | Wake on Ring |
| D | Wake on LAN technology (optional) | | |

**Figure 7.  Hardware Management and Power Connectors**

**Table 21.    Chassis Intrusion Connector (J4K1)**

| Pin | Signal |
|---|---|
| 1 | Ground |
| 2 | CHS_SECURITY |

**Table 22.    Fan 3 (Processor Fan) Connector (J4K2)**

| Pin | Signal |
|-----|--------|
| 1 | Ground |
| 2 | +12 V |
| 3 | Ground |

**Table 23.    Power Connector (J7J1)**

| Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|
| 1 | +3.3 V | 11 | +3.3 V |
| 2 | +3.3 V | 12 | -12 V |
| 3 | Ground | 13 | Ground |
| 4 | +5 V | 14 | PS-ON# (power supply remote on/off) |
| 5 | Ground | 15 | Ground |
| 6 | +5 V | 16 | Ground |
| 7 | Ground | 17 | Ground |
| 8 | PWRGD (Power Good) | 18 | -5 V |
| 9 | +5 VSB (Standby for real-time clock) | 19 | +5 V |
| 10 | +12 V | 20 | +5 V |

⇒ **NOTE**

*The standard SFX 90 W power supply is not sufficient for the SR440BX motherboard.  For more information, see Section 1.13.*

**Table 24.    Wake on Ring Connector (J10C2)**

| Pin | Signal |
|-----|--------|
| 1 | Ground |
| 2 | RINGA# |

**Table 25.    Fan 1 (Power Supply Fan) Connector (optional) (J10J1)**

| Pin | Signal |
|-----|--------|
| 1 | Ground |
| 2 | +12 V (FAN_C) |
| 3 | Tach |

**Table 26.   Wake on LAN Technology Connector (J9J3)**

| Pin | Signal |
|-----|--------|
| 1 | +5 VSB |
| 2 | Ground |
| 3 | WOL |

**Table 27.   Fan 2 (System Fan) Connector (J10C1)**

| Pin | Signal |
|-----|--------|
| 1 | Ground |
| 2 | +12 V (FAN_C) |
| 3 | Tach |

### 1.15.2.4   Add-In Board

Figure 8 shows the location of the add-in board connectors.
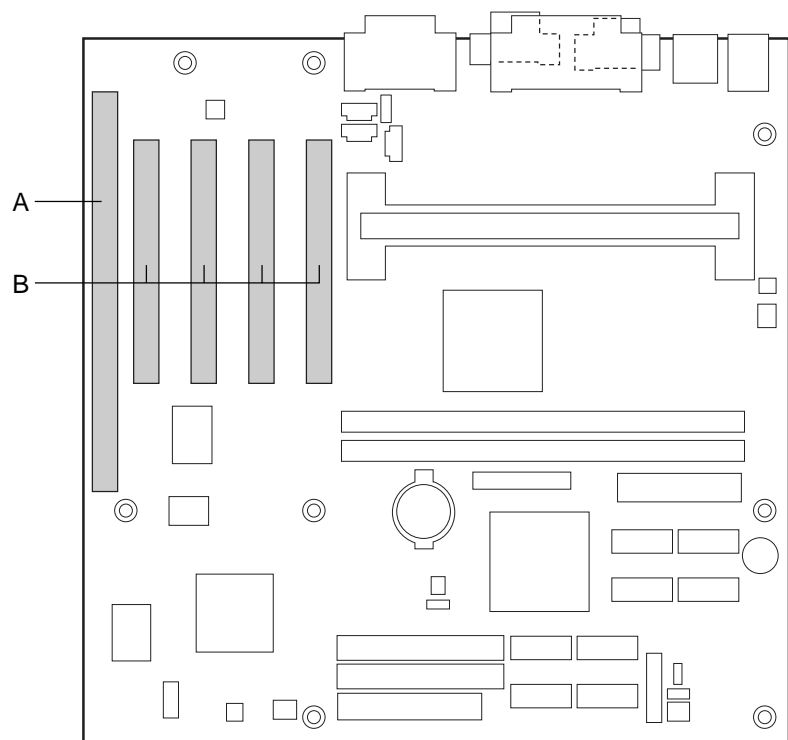


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| A | ISA Bus Connector |
|---|-------------------|
| B | PCI Bus Connectors |

**Figure 8.  Add-In Board Connectors**

**Table 28.  ISA Bus Connector**

| Pin | Signal * | Pin | Signal * |
|-----|----------|-----|----------|
| B1 | Ground | A1 | IOCHK# (IOCHCK#) |
| B2 | RESET (RESDRV) | A2 | SD7 |
| B3 | +5 V | A3 | SD6 |
| B4 | IRQ9 | A4 | SD5 |
| B5 | -5 V | A5 | SD4 |
| B6 | DRQ2 | A6 | SD3 |
| B7 | -12 V | A7 | SD2 |
| B8 | SRDY# (NOWS#) | A8 | SD1 |
| B9 | +12 V | A9 | SD0 |
| B10 | Ground | A10 | IOCHRDY (CHRDY) |
| B11 | SMEMW# (SMWTC#) | A11 | AEN |
| B12 | SMEMR# (SMRDC#) | A12 | SA19 |
| B13 | IOW# (IOWC#) | A13 | SA18 |
| B14 | IOR# (IORC#) | A14 | SA17 |
| B15 | DACK3# | A15 | SA16 |
| B16 | DRQ3 | A16 | SA15 |
| B17 | DACK1# | A17 | SA14 |
| B18 | DRQ1 | A18 | SA13 |
| B19 | REFRESH# | A19 | SA12 |
| B20 | BCLK | A20 | SA11 |
| B21 | IRQ7 | A21 | SA10 |
| B22 | IRQ6 | A22 | SA9 |
| B23 | IRQ5 | A23 | SA8 |
| B24 | IRQ4 | A24 | SA7 |
| B25 | IRQ3 | A25 | SA6 |
| B26 | DACK2# | A26 | SA5 |
| B27 | TC | A27 | SA4 |
| B28 | BALE | A28 | SA3 |
| B29 | +5 V | A29 | SA2 |
| B30 | OSC | A30 | SA1 |
| B31 | Ground | A31 | SA0 |
| Key | | Key | |
| D1 | MEMCS16# (M16#) | C1 | SBHE# |
| D2 | IOCS16# (IO16#) | C2 | LA23 |
| D3 | IRQ10 | C3 | LA22 |
| D4 | IRQ11 | C4 | LA21 |
| D5 | IRQ12 | C5 | LA20 |
| D6 | IRQ15 | C6 | LA19 |

continued

**Table 28.    ISA Bus Connector** (continued)

| Pin | Signal  * | Pin | Signal  * |
|-----|-----------|-----|-----------|
| D7  | IRQ14     | C7  | LA18      |
| D8  | DACK0#    | C8  | LA17      |
| D9  | DRQ0      | C9  | MEMR# (MRDC#) |
| D10 | DACK5#    | C10 | MEMW# (MWTC#) |
| D11 | DRQ5      | C11 | SD8       |
| D12 | DACK6#    | C12 | SD9       |
| D13 | DRQ6      | C13 | SD10      |
| D14 | DACK7#    | C14 | SD11      |
| D15 | DRQ7      | C15 | SD12      |
| D16 | +5 V      | C16 | SD13      |
| D17 | Master16# (MASTER#) | C17 | SD14 |
| D18 | Ground    | C18 | SD15      |

\*    Items in parentheses are alternate versions of signal names.

**Table 29.    PCI Bus Connectors**

| Pin | Signal | Pin | Signal | Pin | Signal | Pin | Signal |
|-----|--------|-----|--------|-----|--------|-----|--------|
| A1 | Ground (TRST#)* | B1 | -12 V | A32 | AD16 | B32 | AD17 |
| A2 | +12 V | B2 | Ground (TCK)* | A33 | +3.3 V | B33 | C/BE2# |
| A3 | +5 V (TMS)* | B3 | Ground | A34 | FRAME# | B34 | Ground |
| A4 | +5 V (TDI)* | B4 | No connect (TDO)* | A35 | Ground | B35 | IRDY# |
| A5 | +5 V | B5 | +5 V | A36 | TRDY# | B36 | +3.3 V |
| A6 | INTA# | B6 | +5 V | A37 | Ground | B37 | DEVSEL# |
| A7 | INTC# | B7 | INTB# | A38 | STOP# | B38 | Ground |
| A8 | +5 V | B8 | INTD# | A39 | +3.3 V | B39 | LOCK# |
| A9 | Reserved | B9 | No connect (PRSNT1#)* | A40 | Reserved | B40 | PERR# |
| A10 | +5 V (I/O) | B10 | Reserved | A41 | Reserved | B41 | +3.3 V |
| A11 | Reserved | B11 | No connect (PRSNT2#)* | A42 | Ground | B42 | SERR# |
| A12 | Ground | B12 | Ground | A43 | PAR | B43 | +3.3 V |
| A13 | Ground | B13 | Ground | A44 | AD15 | B44 | C/BE1# |
| A14 | +3.3 V aux | B14 | Reserved | A45 | +3.3 V | B45 | AD14 |
| A15 | RST# | B15 | Ground | A46 | AD13 | B46 | Ground |
| A16 | +5 V (I/O) | B16 | CLK | A47 | AD11 | B47 | AD12 |
| A17 | GNT# | B17 | Ground | A48 | Ground | B48 | AD10 |
| A18 | Ground | B18 | REQ# | A49 | AD09 | B49 | Ground |
| A19 | PME# | B19 | +5 V (I/O) | A50 | Key | B50 | Key |
| A20 | AD30 | B20 | AD31 | A51 | Key | B51 | Key |
| A21 | +3.3 V | B21 | AD29 | A52 | C/BE0# | B52 | AD08 |
| A22 | AD28 | B22 | Ground | A53 | +3.3 V | B53 | AD07 |
| A23 | AD26 | B23 | AD27 | A54 | AD06 | B54 | +3.3 V |
| A24 | Ground | B24 | AD25 | A55 | AD04 | B55 | AD05 |
| A25 | AD24 | B25 | +3.3 V | A56 | Ground | B56 | AD03 |
| A26 | IDSEL | B26 | C/BE3# | A57 | AD02 | B57 | Ground |
| A27 | +3.3 V | B27 | AD23 | A58 | AD00 | B58 | AD01 |
| A28 | AD22 | B28 | Ground | A59 | +5 V (I/O) | B59 | +5 V (I/O) |
| A29 | AD20 | B29 | AD21 | A60 | REQ64C# | B60 | ACK64C# |
| A30 | Ground | B30 | AD19 | A61 | +5 V | B61 | +5 V |
| A31 | AD18 | B31 | +3.3 V | A62 | +5 V | B62 | +5 V |

*    These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

## 1.15.3   Front Panel Connectors

Figure 9 shows the location of the front panel connectors, and Table 30 lists the connector signals.
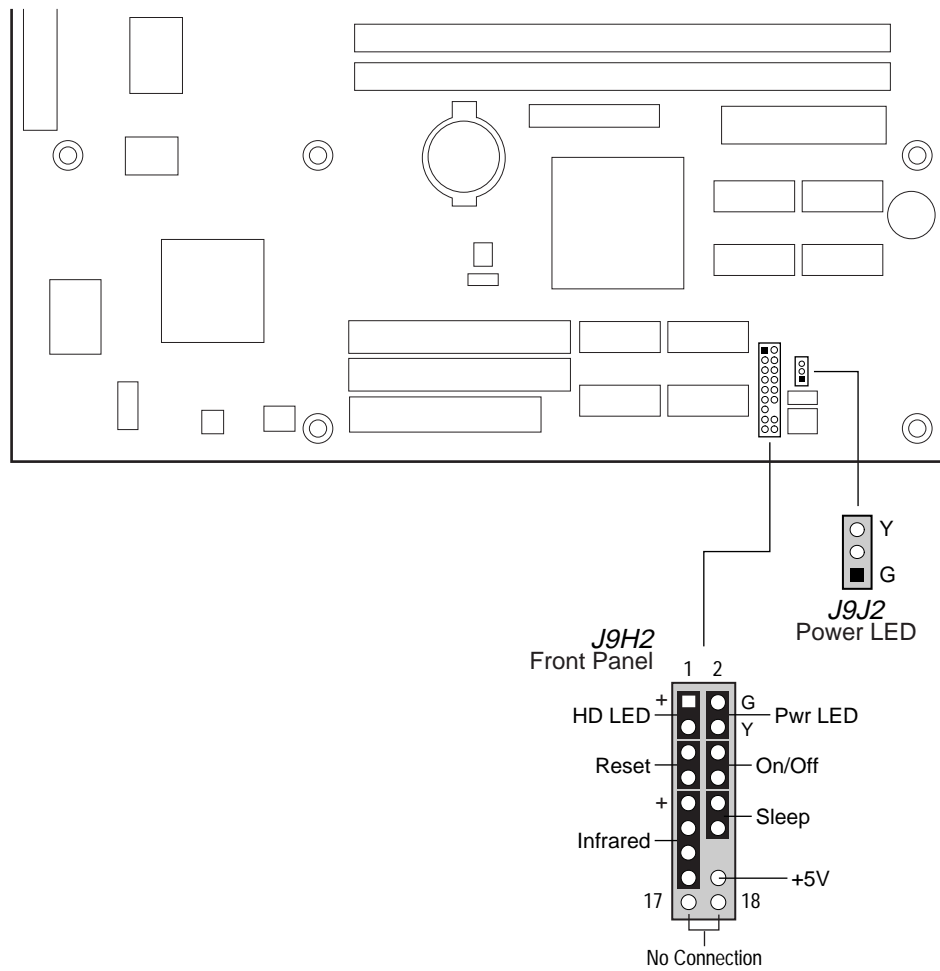


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**Figure 9.  Front Panel I/O Connectors**

**Table 30.    Front Panel I/O Connectors (J9H2)**

| Pin | Signal | In/Out | Description | Pin | Signal | In/Out | Description |
|-----|--------|--------|-------------|-----|--------|--------|-------------|
| 1 | HD_PWR | Out | Hard disk LED pullup (330 Ω) to +5 V | 2 | HDR_BLNK_ GRN | Out | Front panel green LED |
| 3 | HAD# | Out | Hard disk active LED | 4 | HDR_BLNK_ YEL | Out | Front panel yellow LED |
| 5 | GND | | Ground | 6 | FPBUT_IN | In | Front panel On/Off button |
| 7 | FP_RESET# | In | Front panel Reset button | 8 | GND | | Ground |
| 9 | +5 V | Out | IR Power | 10 | FPSLP# | In | Front panel Sleep button |
| 11 | IRRX | In | IrDA† serial input | 12 | GND | | Ground |
| 13 | GND | | Ground | 14 | (pin removed) | | Not connected |
| 15 | IRTX | Out | IrDA serial output | 16 | +5 V | Out | Power |
| 17 | N/C | | Not connected | 18 | N/C | | Not connected |

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive.  For the LED to function properly, an IDE drive must be connected to the onboard hard drive controller.

Pins 2 and 4 can be connected to either a single or dual colored LED that will light when the computer is powered on.  Table 31 and Table 32 show the possible states for these LEDs.

**Table 31.    Power LED (Single-colored)**

| LED State | Description |
|-----------|-------------|
| Off | Off |
| Steady Green | Running |
| Blinking Green | Running or message waiting (Note) |

Note:  To utilize the message waiting function, an OnNow/Instantly
Available aware message capturing software application must be invoked.

**Table 32.    Power LED (Dual-colored)**

| LED State | Description |
|-----------|-------------|
| Off | Off |
| Steady Green | Running |
| Blinking Green | Running or message waiting (Note) |
| Steady Yellow | Sleeping |
| Blinking Yellow | Sleeping or message waiting (Note) |

Note:  To utilize the message waiting function, an OnNow/instantly
Available aware message capturing software application must be invoked.

Pins 6 and 8 can be connected to a momentary SPST type switch that is normally open. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the motherboard.) At least two seconds must pass before the power supply will recognize another on/off signal.

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the motherboard resets and runs the POST.

Pins 10 and 12 can be connected to a momentary SPST type switch that is normally open. When the switch is pressed and the power is on, the motherboard will toggle in or out of the sleep state.

Pins 11, and 13 - 16 can be connected to an IrDA module. After the IrDA interface is configured, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

**Table 33.    Power LED Front Panel Connector (J9J2)**

| Pin | Signal | In/Out | Description |
| --- | --- | --- | --- |
| 1 | HDR_BLNK_GRN | Out | Front panel green LED |
| 2 | | | Not connected |
| 3 | HDR_BLNK_YEL | Out | Front panel yellow LED |

Pins 1 and 3 can be connected to either a single or dual colored LED that will light when the computer is powered on. Table 31 and Table 32 show the possible states for these LEDs.

# 1.16 BIOS Setup Configuration Jumper Block

This 3-pin jumper block enables all motherboard configuration to be done in the BIOS Setup program. Table 34 describes the jumper settings for normal, configure, and recovery modes.

## ⚠ CAUTION

*Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing the jumper.*



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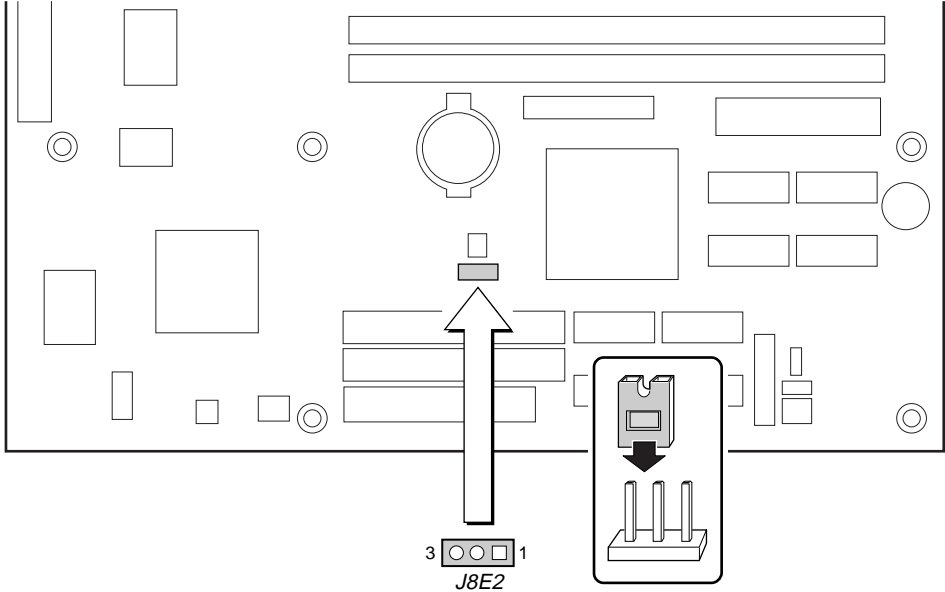
**Figure 10. Location of the BIOS Setup Configuration Jumper Block**

**Table 34. BIOS Setup Configuration Jumper Settings**

| Function | Jumper | Configuration |
|---|---|---|
| Normal | 1-2 | The BIOS uses current configuration information and passwords for booting. |
| Configure | 2-3 | After the POST runs, Setup runs automatically. The maintenance menu is displayed. |
| Recovery | none | The BIOS attempts to recover the BIOS configuration. A recovery diskette is required. |

# 1.17  Mechanical Considerations

## 1.17.1  Form Factor

The motherboard is designed to fit into a microATX form-factor chassis.  Figure 11 illustrates the mechanical form factor for the motherboard.  Dimensions are given in inches.  The outer dimensions are 9.6 x 9.6 inches.  Location of the I/O connectors and mounting holes are in strict compliance with the microATX specification (see Section 6.2).
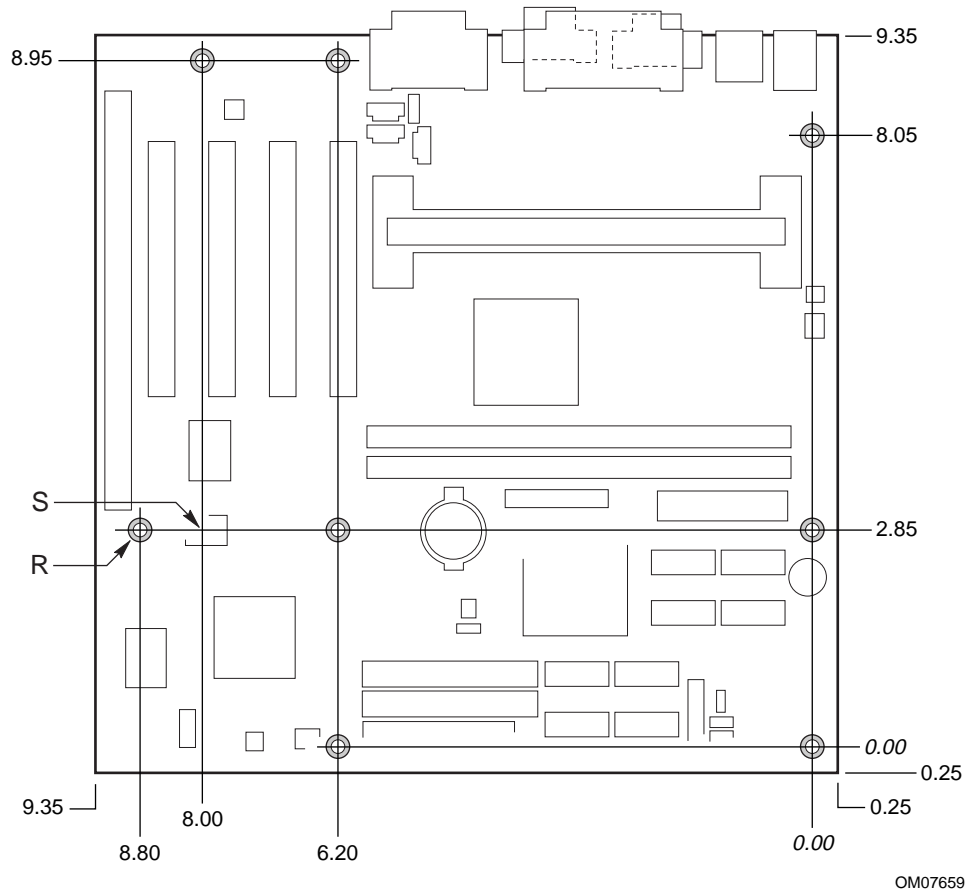


**Figure 11. Motherboard Dimensions**

## ⚠ CAUTION

*As permitted by the microATX specification, the optional hole at location S in Figure 11 was omitted from the SR440BX.  The chassis standoff in this position should not be implemented or should be removable to avoid damage to traces on the motherboard.*

## 1.17.2   I/O Shield

The back panel I/O shield for the motherboard must meet specific dimension and material requirements.  Systems based on this motherboard need the back panel I/O shield to pass certification testing.  Figure 12 shows the critical dimensions of the chassis-independent I/O shield. Dimensions are given in inches.  The figure indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the microATX specification.

⟹  **NOTE**

*A chassis-independent I/O shield designed to be compliant with the microATX chassis specification is available from Intel (part number IO668333-001).*
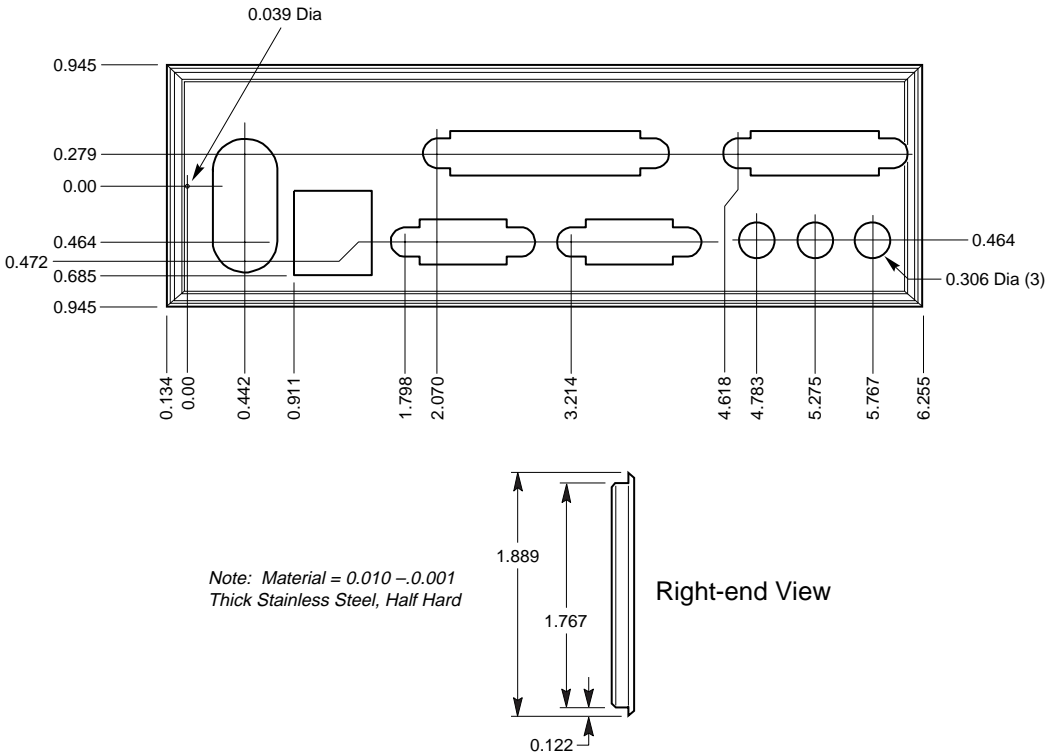


**Figure 12.  Back Panel I/O Shield Dimensions (microATX Chassis-Independent)**

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# 1.18  Electrical Considerations

## 1.18.1   Add-in Board Considerations

The motherboard is designed to provide 2 A (average) of +5 V current for each add-in board.  The total +5 V current draw for add-in boards in a fully-loaded motherboard (all four expansion slots filled) must not exceed 8 A.

## 1.18.2   Power Consumption

Table 35 and Table 36 list voltage and current specifications for a computer that contains the motherboard, a 500 MHz Pentium III processor, 256 MB SDRAM, 512 KB cache, 3.5-inch diskette drive, and a 2.5 GB IDE hard disk drive.  This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate.  AC watts are measured with a typical 200 W supply, nominal input voltage and frequency, with a true RMS wattmeter at the line input.

⟹  **NOTE**

*Actual system power consumption depends upon system configuration.  The power supply should comply with the recommendations found in the ATX form factor specification (see Section 6.2 for specification information).*

**Table 35.   DC Voltage**

| Voltage | Acceptable Tolerance | Wattage | Current |
|---|---|---|---|
| +3.3 V | ± 4% | 10.23 W | 3.1 A |
| +5 V | ± 5% | 6.5 W | 1.3 A |
| -5 V | ± 5% | 0 W | 0 A |
| +12 V | ± 5% | 3.6 W | 300 mA |
| -12 V | ± 5% | 0.12 W | 100 mA |
| 5 V SB (Stand By) | ± 5% | 0.5 W | 100 mA |

**Table 36.   Power Usage**

| Mode | AC (watts) | DC (amps) at: | | | |
|---|---|---|---|---|---|
| | | +3.3 V | +5 V | +12 V | -12 V |
| DOS prompt, APM disabled | 53 W | 3.0 A | 2.7 A | 0.7 mA | 0.2 mA |
| Windows 98 desktop, APM disabled | 33 W | 2.9 A | 2.3 A | 0.6 mA | 0.2 mA |
| Windows 98 desktop, APM enabled, in System Management Mode (SMM) | 27 W | 2.4 A | 0.5 mA | 0.3 mA | 0.2 mA |

Table 37 lists the maximum DC voltage and current requirements for fan 2 (the system fan) when the board is in the Sleep mode or Normal operating mode.  Power consumption is independent of the operating system used and other variables.

**Table 37.    Fan 2 (System Fan) DC Power Requirements**

| Mode | Voltage | Maximum Current (Amps) |
| --- | --- | --- |
| Sleep | 6.7 VDC | 1 A |
| Normal | 9.1 VDC | 1 A |

## 1.18.3   Power Supply Considerations

System integrators should refer to the power usage values listed in Table 36 when selecting a power supply for use with this motherboard.  The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification (see Section 6.2).

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

# 1.19  Thermal Considerations

Figure 13 shows the locations of the thermally-sensitive components.  Table 38 provides maximum component case temperatures for motherboard components that could be sensitive to thermal changes.  Case temperatures could be affected by the operating temperature, current load, or operating frequency.  Maximum case temperatures are important when considering proper airflow to cool the motherboard.
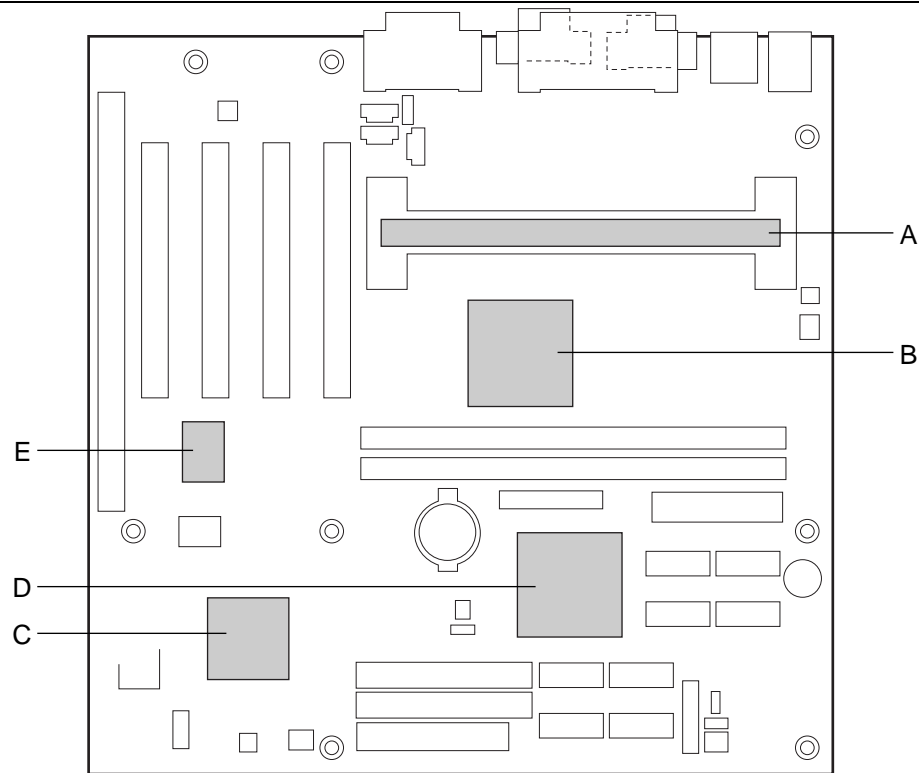


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A    Processor connector
B    Intel 82443BX PAC
C    Intel 82371EB PIIX4E
D    NVIDIA RIVA TNT Graphics controller
E    Sound Blaster Audio PCI 64V audio controller

**Figure 13.  Thermally-sensitive Components**

## ⚠ CAUTION

*An ambient temperature that exceeds the board's maximum operating temperature by 5 $^{o}$C to 10 $^{o}$C could cause components to exceed their maximum case temperature and malfunction.  For information about the maximum operating temperature, see the environmental specifications in Section 1.21.*

**Table 38.    Thermal Considerations for Components**

| Component | Maximum Temperature | | Location |
|---|---|---|---|
| | **SECC** | **SECC2** | |
| Pentium II processor | 233 MHz | 75 °C (thermal plate) | J4G1 (242-contact slot connector) |
| | 266 MHz | 75 °C (thermal plate) | |
| | 300 MHz | 72 °C (thermal plate) | |
| | 333 MHz | 65 °C (thermal plate) | |
| | 350 MHz | 75 °C (thermal plate) | 80 °C (thermal case-core) 105 °C (thermal case-BSRAM) | |
| | 400 MHz | 75 °C (thermal plate) | 80 °C (thermal case-core) 105 °C (thermal case-BSRAM) | |
| | 450 MHz | 70 °C (thermal plate) | 80 °C (thermal case-core) 105 °C (thermal case-BSRAM) | |
| Pentium III processor | 450 MHz | | 80 °C (thermal case-core) 105 °C (thermal case-BSRAM) | |
| | 500 MHz | | 80 °C (thermal case-core) 105 °C (thermal case-BSRAM) | |
| | **SEPP** | | |
| Celeron processor | 266 MHz | 85 °C (thermal case) | |
| | 300 MHz | 85 °C (thermal case) | |
| | 300A MHz | 85 °C (thermal case) | |
| | 333 MHz | 85 °C (thermal case) | |
| | 366 MHz | 85 °C (thermal case) | |
| | 400 MHz | 85 °C (thermal case) | |
| Intel 82443BX (PAC) | 105 °C | | U5F1 |
| Intel 82371EB (PIIX4E) | 85 °C | | U8C1 |
| NVIDIA RIVA TNT graphics controller | 110 °C | | U8G1 |
| Sound Blaster Audio PCI 64V audio controller | 70 °C | | U6B1 |

# 1.20  Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates.  The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991.  The MTBF prediction is for estimating repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC.

Motherboard MTBF:  274,271 hours

# 1.21  Environmental

Table 39 lists the environmental specifications for the motherboard.

**Table 39.    Motherboard Environmental Specifications**

| Parameter | Specification | | |
|---|---|---|---|
| Temperature | | | |
| Non-Operating | -40 °C to +70 °C | | |
| Operating | 0 °C to +55 °C | | |
| Shock | | | |
| Unpackaged | 30 G trapezoidal waveform | | |
| | Velocity change of 170 inches/second | | |
| Packaged | Half sine 2 millisecond | | |
| | Product Weight | Free Fall (inches) | Velocity Change (inches/sec) |
| | <20 lbs. | 36 | 167 |
| | 21-40 lbs. | 30 | 152 |
| | 41-80 lbs. | 24 | 136 |
| | 81-100 lbs. | 18 | 118 |
| Vibration | | | |
| Unpackaged | 5 Hz to 20 Hz :  0.01 g² Hz sloping up to 0.02 g² Hz | | |
| | 20 Hz to 500 Hz :  0.02 g² Hz (flat) | | |
| Packaged | 10 Hz to 40 Hz :  0.015 g² Hz (flat) | | |
| | 40 Hz to 500 Hz :  0.015 g² Hz sloping down to 0.00015 g² Hz | | |

# 1.22  Regulatory Compliance

This motherboard complies with the following safety and EMC regulations when correctly installed in a compatible host system.

**Table 40.  Safety Regulations**

| Regulation | Title |
|---|---|
| UL 1950/CSA950, 3$^{rd}$  edition, Dated 07-28-95 | Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment.  (USA and Canada) |
| EN 60950, 2$^{nd}$ Edition, 1992 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment.  (European Community) |
| IEC 950, 2$^{nd}$ edition, 1991 (with Amendments 1, 2, 3, and 4) | The Standard for Safety of Information Technology Equipment including Electrical Business Equipment.  (International) |
| EMKO-TSE (74-SEC) 207/94 | Summary of Nordic deviations to EN 60950.  (Norway, Sweden, Denmark, and Finland) |

**Table 41.  EMC Regulations**

| Regulation | Title |
|---|---|
| FCC Class B | Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators.  (USA) |
| CISPR 22, 2$^{nd}$ Edition, 1993 (Class B) | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International) |
| VCCI Class B (ITE) | Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines.  (Japan) |
| EN55022 (1994) (Class B) | Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment.  (Europe) |
| EN50082-1 (1992) | Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3, and -4.  (Europe) |
| ICES-003 (1997) | Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374).  (Canada) |

This printed circuit assembly has the following product certification markings

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side)
- Manufacturer's recognition mark:  Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0)  (Solder side)
- UL File Number for motherboards:  E139761 (Component side)
- PB Part Number:  Intel bare circuit board part number 730793-001 (Solder side)
- Battery "+ Side Up" marking:  located on the component side of the board in close proximity to the battery holder
- FCC Logo/Declaration:  (Solder side)
- CE Mark:  (Component side)  The CE mark should also be on the shipping container

# 2 Motherboard Resources

## What This Chapter Contains

## 2.1 Memory Map

**Table 42.    System Memory Map**

| Address Range (decimal) | Address Range (hex) | Size | Description |
|---|---|---|---|
| 1024 K - 524288 K | 100000 - 20000000 | 511 MB | Extended Memory |
| 960 K - 1024 K | F0000 - FFFFF | 64 KB | Runtime BIOS |
| 896 K - 960 K | E0000 - EFFFF | 64 KB | Reserved |
| 800 K - 896 K | C8000 - DFFFF | 96 KB | Available high DOS memory (open to ISA and PCI bus) |
| 640 K - 800 K | A0000 - C7FFF | 160 KB | Video memory and BIOS |
| 639 K - 640 K | 9FC00 - 9FFFF | 1 KB | Extended BIOS data (movable by memory manager software) |
| 512 K - 639 K | 80000 - 9FBFF | 127 KB | Extended conventional memory |
| 0 K - 512 K | 00000 - 7FFFF | 512 KB | Conventional memory |

## 2.2   DMA Channels

**Table 43.   DMA Channels**

| DMA Channel Number | Data Width | System Resource |
|---|---|---|
| 0 | 8 or 16 bits | Audio |
| 1 | 8 or 16 bits | Audio/parallel port |
| 2 | 8 or 16 bits | Diskette drive |
| 3 | 8 or 16 bits | Parallel port (for ECP or EPP)/audio |
| 4 | | Reserved - cascade channel |
| 5 | 16 bits | Open |
| 6 | 16 bits | Open |
| 7 | 16 bits | Open |

## 2.3   I/O Map

**Table 44.   I/O Map**

| Address (hex) | Size | Description |
|---|---|---|
| 0000 - 000F | 16 bytes | PIIX4E - DMA 1 |
| 0020 - 0021 | 2 bytes | PIIX4E - interrupt controller 1 |
| 0040 - 0043 | 4 bytes | PIIX4E - counter/timer 1 |
| 0048 - 004B | 4 bytes | PIIX4E - counter/timer 2 |
| 0060 | 1 byte | Keyboard controller byte - reset IRQ |
| 0061 | 1 byte | PIIX4E - NMI, speaker control |
| 0064 | 1 byte | Keyboard controller, CMD/STAT byte |
| 0070, bit 7 | 1 bit | PIIX4E - enable NMI |
| 0070, bits 6:0 | 7 bits | PIIX4E - real time clock, address |
| 0071 | 1 byte | PIIX4E - real time clock, data |
| 0070 -0071 | 2 bytes | CMOS Bank 0 |
| 0072 - 0073 | 2 bytes | CMOS Bank 1 |
| 0080 - 008F | 16 bytes | PIIX4E - DMA page registers |
| 00A0 - 00A1 | 2 bytes | PIIX4E - interrupt controller 2 |
| 00B2 - 00B3 | 2 bytes | APM control |
| 00C0 - 00DE | 31 bytes | PIIX4E - DMA 2 |
| 00F0 | 1 byte | Reset numeric error |
| 0170 - 0177 | 8 bytes | Secondary IDE channel |
| 01F0 - 01F7 | 8 bytes | Primary IDE channel |
| 0200, or 0208, or 0210, or 0218 | (Note 1) | Audio/game port |
| 0220 - 022F | 16 bytes | Audio (Sound Blaster Pro[†] compatible) |

continued

**Table 44.  I/O Map** (continued)

| Address (hex) | Size | Description |
| --- | --- | --- |
| 0240 - 024F | 16 bytes | Audio (Sound Blaster Pro compatible) |
| 0278 - 027F | 8 bytes | LPT2 |
| 0228 - 022F | 8 bytes | LPT3 |
| 02E8 - 02EF | 8 bytes | COM4/video (8514A) |
| 02F8 - 02FF | 8 bytes | COM2 |
| 0320 - 0327, or 0330 - 0337, or 0340 - 0347, or 0350 - 0357 (Note 2) | 8 bytes | MPU-401 (MIDI) |
| 0376 | 1 byte | Secondary IDE channel command port |
| 0377 | 1 byte | Floppy channel 2 command |
| 0377, bit 7 | 1 bit | Floppy disk change, channel 2 |
| 0377, bits 6:0 | 7 bits | Secondary IDE channel status port |
| 0378 - 037F | 8 bytes | LPT 1 |
| 0388- 038B | 6 bytes | AdLib[†] (FM synthesizer) |
| 03B4 - 03B5 | 2 bytes | Video (VGA) |
| 03BA | 1 byte | Video (VGA) |
| 03C0 - 03CA | 2 bytes | Video (VGA) |
| 03CC | 1 byte | Video (VGA) |
| 03CE - 03CF | 2 bytes | Video (VGA) |
| 03D4 - 03D5 | 2 bytes | Video (VGA) |
| 03DA | 1 byte | Video (VGA) |
| 03E8 - 03EF | 8 bytes | COM3 |
| 03F0 - 03F5 | 6 bytes | Diskette channel 1 |
| 03F6 | 1 byte | Primary IDE channel command port |
| 03F7 (Write) | 1 byte | Diskette channel 1 command |
| 03F7, bit 7 | 1 bit | Diskette disk change channel 1 |
| 03F7, bits 6:0 | 7 bits | Primary IDE channel status port |
| 03F8 - 03FF | 8 bytes | COM1 |
| 04D0 - 04D1 | 2 bytes | Edge/level triggered PIC |
| 0530 - 0537, or 0E80 - 0E87, or 0F40 - 0F47 (Note 2) | 8 bytes | Windows Sound System |
| LPTn + 400h | 8 bytes | ECP port, LPTn base address + 400h |
| 0CF8 - 0CFB (Note 3) | 4 bytes | PCI configuration address register |

continued

**Table 44.    I/O Map** (continued)

| Address (hex) | Size | Description |
|---|---|---|
| 0CF9 (Note 4) | 1 byte | Turbo and reset control register |
| 0CFC - 0CFF | 4 bytes | PCI configuration data register |
| EF00 - EF3F | 64 bytes | Windows Sound System |
| FFA0 - FFA7 | 8 bytes | Primary bus master IDE registers |
| FFA8 - FFAF | 8 bytes | Secondary bus master IDE registers |

Note 1    The address range for this device can vary for 1 to 8 bytes.

Note 2    These are the possible starting address for this device.

Note 3    DWORD access only.

Note 4    Byte access only

# 2.4   PCI Configuration Space Map

**Table 45.    PCI Configuration Space Map**

| Bus Number (hex) | Device Number (hex) | Function Number (hex) | Description |
|---|---|---|---|
| 00 | 00 | 00 | Intel 82443BX (PAC) |
| 00 | 01 | 00 | Intel 82443BX PCI/AGP bridge |
| 00 | 07 | 00 | Intel 82371EB (PIIX4E) PCI/ISA bridge |
| 00 | 07 | 01 | Intel 82371EB (PIIX4E ) IDE bus master |
| 00 | 07 | 02 | Intel 82371EB (PIIX4E) USB |
| 00 | 07 | 03 | Intel 82371EB (PIIX4E) power management |
| 00 | 0C | 00 | PCI audio controller (Sound Blaster AudioPCI 64V) |
| 00 | 0D | 00 | PCI expansion slot 1 (J4D1) |
| 00 | 0E | 00 | PCI expansion slot 2 (J4C1) |
| 00 | 0F | 00 | PCI expansion slot 3 (J4B1) |
| 00 | 10 | 00 | PCI expansion slot 4 (J4A1) |
| 01 | 00 | 00 | NVIDIA RIVA TNT graphics controller |

# 2.5 Interrupts

**Table 46.    Interrupts**

| IRQ | System Resource |
| --- | --- |
| NMI | I/O channel check |
| 0 | Reserved, interval timer |
| 1 | Reserved, keyboard buffer full |
| 2 | Reserved, cascade interrupt from slave PIC |
| 3 | COM2* |
| 4 | COM1* |
| 5 | LPT2 (Plug and Play option) and audio/User available |
| 6 | Diskette drive |
| 7 | LPT1* |
| 8 | Real time clock |
| 9 | Reserved for PIIX4E system management bus |
| 10 | User available |
| 11 | Windows Sound System*/User available |
| 12 | Onboard mouse port (if present, else user available) |
| 13 | Reserved, math coprocessor |
| 14 | Primary IDE (if present, else user available) |
| 15 | Secondary IDE (if present, else user available) |

\*     Default, but can be changed to another IRQ

# 2.6  PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI expansion slots and onboard PCI devices.  The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus.  In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices.  In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices.  Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA:  By default, all add-in cards that require only one interrupt are in this category.  For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB:  Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB.  (This is not an absolute requirement.)
- INTC and INTD:  Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4E PCI-to-ISA bridge has four programmable interrupt request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt. Table 47 lists the PIRQ signals and shows how the signals are connected to the PCI expansion slots and to onboard PCI interrupt sources.

**Table 47.   PCI Interrupt Routing Map**

| PIIX4 PIRQ Signal | 1st PCI Expansion Slot (J4D1) | 2nd PCI Expansion Slot (J4C1) | 3rd PCI Expansion Slot (J4B1) | 4th PCI Expansion Slot (J4A1) | Onboard Video | PCI Audio | USB |
|---|---|---|---|---|---|---|---|
| PIRQA | INTA | INTD | INTC | INTB | INTA | | |
| PIRQB | INTB | INTA | INTD | INTC | | INTA | |
| PIRQC | INTC | INTB | INTA | INTD | | | |
| PIRQD | INTD | INTC | INTB | INTA | | | INTA |

For example, assume an add-in card has one interrupt (group INTA) into the fourth PCI slot. In this slot, an interrupt source from group INTA connects to the PIRQD signal, which is already connected to the USB PCI source. The add-in card shares an interrupt with this onboard interrupt source.

⟹ **NOTE**

*The PIIX4E can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 7, 9, 10, 11, 14, 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.*

# 3 Overview of BIOS Features

## What This Chapter Contains

## 3.1 Introduction

The motherboard uses an Intel/AMI BIOS, which is stored in flash memory and can be upgraded using a disk-based program. In addition to the BIOS, the flash memory contains the Setup program, POST, APM, the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Section 6.2 for the supported versions of these specifications.

This motherboard supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as 4S4RB0XA.86A.

## 3.2   BIOS Flash Memory Organization

The Intel E28F004B5 4-Mbit flash component is organized as 512 KB x 8 bits and is divided into areas as described in Table 48.  The table shows the addresses in the ROM image in normal mode (the addresses change in BIOS recovery mode).

**Table 48.    Flash Memory Organization**

| Address (Hex) | Size | Description |
| --- | --- | --- |
| FFFFC000 - FFFFFFFF | 16 KB | Boot block |
| FFFFA000 - FFFFBFFF | 8 KB | Vital Product Data (VPD) Extended System Configuration Data (ESCD) (DMI configuration data/Plug and Play data) |
| FFFF9000 - FFFF9FFF | 4 KB | Used by the BIOS (e.g., for event logging) |
| FFFF8000 - FFFF8FFF | 4 KB | OEM logo or Scan Flash Area |
| FFF80000 - FFFF7FFF | 480 KB | Main BIOS block |

## 3.3   Resource Configuration

### 3.3.1   Plug and Play:  PCI Autoconfiguration

The BIOS can automatically configure PCI devices and Plug and Play devices.  PCI devices may be onboard or add-in cards.  Plug and Play devices are ISA devices built to meet the Plug and Play specification.  Autoconfiguration lets a user insert or remove PCI or Plug and Play cards without having to configure the system.  When a user turns on the system after adding a PCI or Plug and Play card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources.  The assignment of PCI interrupts to ISA IRQs is nondeterministic. PCI devices can share an interrupt, but an ISA device cannot share an interrupt allocated to PCI or to another ISA device.  Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by this BIOS, see Section 6.2.

### 3.3.2   ISA Plug and Play

If Plug and Play operating system (see Section 4.4.1) is selected in Setup, the BIOS autoconfigures only ISA Plug and Play cards that are required for booting (IPL devices).  If Plug and Play operating system is not selected in Setup, the BIOS autoconfigures all Plug and Play ISA cards. Since ISA legacy devices are not autoconfigurable, the resources for them must be reserved in BIOS Setup.

### 3.3.3  PCI IDE Support

If you select Auto in Setup, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support.  The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 6.2 for the supported version of ATAPI).  Add-in ISA IDE controllers are not supported.  The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance.  To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive.  You can override the auto-configuration options by specifying manual configuration in Setup.

⟹ **NOTE**

*Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device.*

## 3.4  SMBIOS

SMBIOS is a method for managing computers in a managed network.  See Section 6.2 for information about the latest SMBIOS specification.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components.  Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components.  The MIF database defines the data and provides the method for accessing this information.  The BIOS enables applications such as Intel® LANDesk® Client Manager to use SMBIOS.  The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

## 3.5  Power Management

The BIOS supports both APM and ACPI.  If the board is used with an ACPI-aware operating system, the BIOS provides ACPI support.  Otherwise, it defaults to APM support.

### 3.5.1  APM

See Section 6.2 for the version of the APM specification that is supported.  The energy saving standby mode can be initiated in the following ways:

- Time-out period specified in Setup
- Suspend/resume switch connected to the front panel sleep connector
- From the operating system, such as the Suspend menu item in Windows 95

In standby mode, the motherboard can reduce power consumption by spinning down hard drives, and reducing power to or turning off VESA DPMS-compliant monitors.  Power-management mode can be enabled or disabled in Setup (see Section 4.6).

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default; but the operating system must support an APM driver for the power-management features to work. For example, Windows 95 supports the power-management features upon detecting that APM is enabled in the BIOS.

Table 49 describes which APM devices or specific events can wake the computer from specific states.

**Table 49. APM Wake Up Devices and Events**

| These devices/events can wake up the computer… | …from this APM state |
|---|---|
| Power switch | Standby, Soft Off |
| RTC alarm | Standby, Soft Off |
| LAN | Standby, Soft Off |
| Modem | Standby, Soft Off |
| IR command | Not Available |
| USB | Not Available |
| PS/2* keyboard | Standby |
| PS/2 mouse | Standby |
| Sleep button | Soft Off (from front panel header) |

## 3.5.2  ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. ACPI requires an ACPI-aware operating system. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM functionality normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the Power On Suspend sleeping state, and less than 5-watt system operation in the Suspend to Disk sleeping state
- A Soft-off feature that enables the operating system to power off the computer
- Support for multiple wake up events (see Table 52)
- Support for a front panel power and sleep mode switch. Table 50 describes the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system

**Table 50. Effects of Pressing the Power Switch**

| If the system is in this state… | …and the power switch is pressed for | …the system enters this state |
|---|---|---|
| Off | Less than four seconds | Power on |
| On | Less than four seconds | Soft off/Suspend |
| On | More than four seconds | Fail safe power off |
| Sleep | Less than four seconds | Wake up |

### 3.5.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 51 lists the power states supported by the motherboard along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

**Table 51. Power States and Targeted System Power**

| Global States | Sleeping States | CPU States | Device States | Targeted System Power * |
|---|---|---|---|---|
| G0 - working state | S0 - working | C0 - working | D0 - working state | Full power > 60 W |
| G1 - sleeping state | S1 - CPU stopped | C1 - stop grant | D1, D2, D3-device specification specific. | 5 W < power < 30 W |
| G2/S5 | S5 - Soft off. Context not saved. Cold boot is required. | No power | D3 - no power except for wake up logic. | Power < 5 W  ** |
| G3 - mechanical off. AC power is disconnected from the computer. | No power to the system. | No power | D3 - no power for wake up logic, except when provided by battery or external source. | No power to the system so that service can be performed. |

- Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

** Dependent on the standby power consumption of wake-up devices used in the system.

### 3.5.2.2　Wake Up Devices and Events

Table 52 describes which devices or specific events can wake the computer from specific states.

**Table 52.　ACPI Wake Up Devices and Events**

| These devices/events can wake up the computer… | …from this state |
| --- | --- |
| Power switch | S1, S5 |
| RTC alarm | S1, S5 |
| LAN | S1 |
| Modem | S1 |
| IR command | S1 |
| USB | S1 |
| PS/2 keyboard | S1 |
| PS/2 mouse | S1 |
| Sleep button | S1 |

### 3.5.2.3　Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration.  ACPI is used only to enumerate and configure motherboard devices that do not have other hardware standards for enumeration and configuration.  PCI devices on the motherboard, for example, are not enumerated by ACPI.

## 3.6　BIOS Upgrades

A new version of the BIOS can be upgraded from a diskette using the Intel® Flash Memory Update Utility that is available from Intel.  This utility supports the following BIOS maintenance functions:

- Update the flash BIOS from a file on a diskette
- Change the language section of the BIOS
- Verify that the upgrade BIOS matches the target system to prevent accidentally installing an incompatible BIOS

BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel through the Intel World Wide Web site.  See Section 6.1 for information about this site.

⇒ **NOTE**

*Please review the instructions distributed with the upgrade utility before attempting a BIOS upgrade.*

### 3.6.1   Language Support

The Setup program and help messages can be supported in 32 languages.  Five languages are available in the BIOS:  American English, German, Italian, French, and Spanish.  The default language is American English, which is present unless another language is selected in BIOS Setup.

The BIOS includes extensions to support the Kanji character set and other non-ASCII character sets.  Translations of other languages may become available at a later date.

### 3.6.2   OEM Logo or Scan Area

A 4 KB flash-memory user area is available for displaying a custom OEM logo during POST.  A utility is available from Intel to assist with installing a logo into the flash memory.  Information about this capability is available on the Intel World Wide Web site.  See Section 6.1 for more information about this site.

## 3.7   Recovering BIOS Data

Some types of failure can destroy the BIOS.  For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory.  The BIOS can be recovered from a diskette using the BIOS recovery mode (see Section 1.16).  When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the nonerasable boot block area, there is no video support.  The procedure can only be monitored by listening to the speaker and looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- A single beep indicates the beginning of the BIOS recovery process.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the recovery files copied to it.  The recovery files are available at the Intel World Wide Web site.  See Section 6.1 for more information about this site.

⇒ **NOTE**

*If the computer is configured to boot from an LS-120 diskette (see Section 4.7), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.*

⇒ **NOTE**

*BIOS Recovery cannot be accomplished using non-SPD DIMMs.  SPD data structure is required for the recovery process.*

## 3.8   Boot Options

In the Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network.  The default setting is for the diskette drive to be the primary boot device and the hard drive to be the secondary boot device.

### 3.8.1   CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification.  See Section 6.2 for information about the El Torito specification.  Under the Boot menu in the Setup program, CD-ROM is listed as a boot device.  Boot devices are defined in priority order.  If the CD-ROM is selected as the boot device, it must be the first device.

The network can be selected as a boot device.  This selection allows booting from a network add-in card with a remote boot ROM installed.

### 3.8.2   Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if no video adapter, keyboard, or mouse is attached.  During POST, the board will beep six times to indicate that no video adapter was detected, but this is not a fatal error.

With regard to standard settings and custom default settings in the BIOS, if custom defaults have been set, the battery has failed, and AC power has failed, custom defaults will be loaded back into CMOS RAM at power on.  If no custom defaults have been set, the standard defaults will be loaded back into CMOS RAM at power on.

## 3.9   USB Legacy Support

USB legacy support enables USB keyboards and mice to be used even when no operating system USB drivers are in place.  By default, USB legacy support is disabled.  USB legacy support is only intended to be used in accessing BIOS Setup and installing an operating system that supports USB.

This sequence describes how USB legacy support operates in the default (disabled) mode.

1.  When you power up the computer, USB legacy support is disabled.
2.  POST begins.
3.  USB legacy support is temporarily enabled by the BIOS.  This allows you to use a USB keyboard to enter the Setup program or the maintenance mode.
4.  POST completes and disables USB legacy support (unless it was set to Enabled while in Setup).
5.  The operating system loads.  While the operating system is loading, USB keyboards and mice are not recognized.  After the operating system loads the USB drivers, the USB devices are recognized.

To install an operating system that supports USB, enable USB Legacy support in BIOS Setup and follow the operating system's installation instructions.  Once the operating system is installed and the USB drivers configured, USB legacy support is no longer used.  USB Legacy Support can be left enabled in BIOS Setup if needed.

Notes on using USB legacy support:

*   If USB legacy support is enabled, don't mix USB and PS/2 keyboards and mice.  For example, do not use a PS/2 keyboard with a USB mouse, or a USB keyboard and a PS/2 mouse.
*   Do not use USB devices with an operating system that does not support USB.  USB legacy is not intended to support the use of USB devices in a non-USB aware operating system.
*   USB legacy support is for keyboards and mice only.  Hubs and other USB devices are not supported.

# 3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the Setup program. This is supervisor mode.
- The user password gives restricted access to view and change Setup options in the Setup program. This is user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 53 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

**Table 53. Supervisor and User Password Functions**

| Password Set | Supervisor Mode | User Mode | Setup Options | Password to Enter Setup | Password During Boot |
|---|---|---|---|---|---|
| Neither | Can change all options * | Can change all options * | None | None | None |
| Supervisor only | Can change all options | Can change a limited number of options | Supervisor Password | Supervisor | None |
| User only | N/A | Can change all options | Enter Password Clear User Password | User | User |
| Supervisor and user set | Can change all options | Can change a limited number of options | Supervisor Password Enter Password | Supervisor or user | Supervisor or user |

\*     If no password is set, any user can change all Setup options.

# 4 BIOS Setup Program

## What This Chapter Contains

## 4.1 Introduction

The Setup program is for viewing and changing the BIOS settings for a computer. Setup is accessed by pressing the <F2> key after the Power-On Self Test (POST) memory test begins and before the operating system boot begins.

Table 54 shows the menus available from the menu bar at the top of the Setup screen.

**Table 54.  Setup Menu Bar**

| Setup Menu Screen | Description |
|---|---|
| Maintenance | Specifies the processor speed and clears the Setup passwords. This menu is only available in configure mode. Refer to Section 1.16 for information about configure mode. |
| Main | Allocates resources for hardware components. |
| Advanced | Specifies advanced features available through the chipset. |
| Security | Specifies passwords and security features. |
| Power | Specifies power management features. |
| Boot | Specifies boot options and power supply controls. |
| Exit | Saves or discards changes to the Setup program options. |

Table 55 shows the function keys available for menu screens.

**Table 55.    Setup Function Keys**

| Setup Key | Description |
|---|---|
| <Esc> | Exits the menu. |
| <←> or <→> | Selects a different menu screen. |
| <↑> or <↓> | Moves cursor up or down. |
| <F9> | Load the default configuration values for the current menu. |
| <F10> | Save the current values and exit Setup. |
| <Enter> | Executes command or selects the submenu. |

# 4.2   Maintenance Menu

The Maintenance Menu is for setting the processor speed (where appropriate) and for clearing the Setup passwords.  Setup only displays this menu in configure mode.  See Section 1.16 for information about setting configure mode.

The processor speed of Intel processors that have been available through late 1998 is determined by the logic levels provided at the processor bus function pins.  With these processors, the speed settings are controlled by the motherboard BIOS in configure mode via the Maintenance Menu.

The processor speed option previously available in configure mode is not displayed when newer Intel processors are installed on this motherboard.  Newer Intel processors boot with the ratio preset and tested during manufacturing.  The fixed pre-selected ratios are reflected in the EBL_CR_POWERON register.

**Table 56.    Maintenance Menu**

| Feature | Options | Description |
|---|---|---|
| Processor Speed (66 MHz Host Bus) | • 233<br>• 266<br>• 300<br>• 333<br>• 366<br>• 400 | Specifies the processor speed in megahertz.  This setup screen will only show speeds up to and including the maximum speed of the processor installed on the motherboard.<br><br>With a host bus operating at 66 MHz, the board supports processors at the following speeds:  233, 266, 300, 333, 366, and 400 MHz. |
| Processor Speed (100 MHz Host Bus) | • 350<br>• 400<br>• 450<br>• 500 | With a host bus operating at 100 MHz, the board supports processors at the following speeds:  350, 400, 450, and 500 MHz. |
| Clear All Passwords | No options | Clears the user and supervisor passwords. |

# 4.3  Main Menu

This menu reports processor and memory information and is for configuring the system date and system time.

**Table 57.  Main Menu**

| Feature | Options | Description |
| --- | --- | --- |
| BIOS Version | No options | Displays the version of the BIOS. |
| Processor Type | No options | Displays processor type. |
| Processor Speed | No options | Displays processor speed. |
| Cache RAM | No options | Displays the size of second-level cache. |
| Total Memory | No options | Displays the total amount of RAM on the motherboard. |
| Bank 0<br>Bank 1 | No options | Displays size and type of DIMM installed in each memory bank. |
| Language | • **English (US) (default)**<br>• German<br>• French<br>• Italian<br>• Spanish | Selects the default language used by the BIOS. |
| Cache Bus ECC | • **Disabled (default)**<br>• Enabled<br>• N/A | Enables or disables ECC on the cache bus. |
| Memory Configuration | • **non-ECC (default)**<br>• ECC | Enables or disables ECC. |
| System Time | Hour, minute, and second | Specifies the current time. |
| System Date | Month, day, and year | Specifies the current date. |

# 4.4 Advanced Menu

This menu is for setting advanced features that are available through the chipset.

**Table 58.    Advanced Menu**

| Feature | Options | Description |
|---|---|---|
| Boot Settings Configuration | No options | Configures Plug and Play and the Numlock key, and resets configuration data.  When selected, displays the Boot Settings Configuration submenu. |
| Peripheral Configuration | No options | Configures peripheral ports and devices.  When selected, displays the Peripheral Configuration submenu. |
| IDE Configuration | No options | Specifies type of connected IDE device. |
| Diskette Configuration | No options | When selected, displays the Floppy Options submenu. |
| Event Log Configuration | No options | Configures event logging.  When selected, displays the Event Log Configuration submenu. |
| Video Configuration | No options | Configures video features.  When selected, displays the Video Configuration submenu. |
| Resource Configuration | No options | Configures memory blocks and IRQs for legacy ISA devices. When selected, displays the Resource Configuration submenu. |

## 4.4.1 Boot Setting Configuration Submenu

This menu is for setting Plug and Play and the Numlock key, and for resetting configuration data.

**Table 59.    Boot Setting Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Plug & Play O/S | • **No (default)**<br>• Yes | Specifies if a Plug and Play operating system is being used. *No* lets the BIOS configure all devices. *Yes* lets the operating system configure Plug and Play devices.  Not required with a Plug and Play operating system. |
| Reset Config Data | • **No (default)**<br>• Yes | Clears the BIOS configuration data on the next boot. |
| Numlock | • Off<br>• **On (default)** | Specifies the power on state of the Numlock feature on the numeric keypad of the keyboard. |

## 4.4.2    Peripheral Configuration Submenu

This submenu is used for configuring the computer peripherals.

**Table 60.    Peripheral Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Serial port A | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures serial port A.<br><br>*Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4.<br><br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Base I/O address | • **3F8 (default)**<br>• 2F8<br>• 3E8<br>• 2E8 | Specifies the base I/O address for serial port A, if serial port A is set to *Enabled*. |
| Interrupt | • IRQ 3<br>• **IRQ 4 (default)** | Specifies the interrupt for serial port A, if serial port A is set to *Enabled*. |
| Serial port B | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures serial port B.<br><br>*Auto* assigns the first free COM port, normally COM2, the address 2F8h and the interrupt IRQ3.<br><br>An * (asterisk) displayed next to an address indicates a conflict with another device.<br><br>If either serial port address is set, that address will not appear in the list of options for the other serial port. |
| Mode | • **Normal (default)**<br>• IrDA SIR-A<br>• ASK_IR | Specifies the mode for serial port B for normal (COM 2) or infrared applications.  This option is not available if serial port B has been disabled. |
| Base I/O address | • 3F8<br>• **2F8 (default)**<br>• 3E8<br>• 2E8 | Specifies the base I/O address for serial port B. |
| Interrupt | • **IRQ 3 (default)**<br>• IRQ 4 | Specifies the interrupt for serial port B. |

continued

**Table 60.    Peripheral Configuration Submenu** (continued)

| Feature | Options | Description |
|---|---|---|
| Parallel port | • Disabled<br>• Enabled<br>• **Auto (default)** | Configures the parallel port.<br>*Auto* assigns LPT1 the address 378h and the interrupt IRQ7.<br>An * (asterisk) displayed next to an address indicates a conflict with another device. |
| Mode | • Output Only<br>• **Bi-directional (default)**<br>• EPP<br>• ECP | Selects the mode for the parallel port.  Not available if the parallel port is disabled.<br>*Output Only* operates in AT†-compatible mode.<br>*Bi-directional* operates in PS/2-compatible mode.<br>*EPP* is Extended Parallel Port mode, a high-speed bi-directional mode.<br>*ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode. |
| Base I/O address | • **378 (default)**<br>• 278<br>• 228 | Specifies the base I/O address for the parallel port. |
| Interrupt | • **IRQ 5 (default)**<br>• IRQ 7 | Specifies the interrupt for the parallel port. |
| Audio Device | • Disabled<br>• **Enabled (default)** | Enables or disables the onboard audio subsystem. |
| Legacy USB Support | • Disabled<br>• Enabled<br>• **Auto (default)** | Enables or disables USB legacy support.<br>(See Section 3.9 for more information.) |

## 4.4.3　IDE Controller Submenu

**Table 61.　IDE Device Configuration**

| Feature | Options | Description |
|---|---|---|
| IDE Controller | • Disabled<br>• Primary<br>• Secondary<br>• **Both (default)** | Specifies the integrated IDE controller.<br>*Primary* enables only the Primary IDE Controller.<br>*Secondary* enables only the Secondary IDE Controller.<br>*Both* enables both IDE controllers. |
| Hard Disk Pre-Delay | • **Disabled (default)**<br>• 3 Seconds<br>• 6 Seconds<br>• 9 Seconds<br>• 12 Seconds<br>• 15 Seconds<br>• 21 Seconds<br>• 30 Seconds | Specifies the hard disk drive pre-delay. |
| Primary IDE Master | No options | Reports type of connected IDE device.  When selected, displays the Primary IDE Master submenu. |
| Primary IDE Slave | No options | Reports type of connected IDE device.  When selected, displays the Primary IDE Slave submenu. |
| Secondary IDE Master | No options | Reports type of connected IDE device.  When selected, displays the Secondary IDE Master submenu. |
| Secondary IDE Slave | No options | Reports type of connected IDE device.  When selected, displays the Secondary IDE Slave submenu. |

## 4.4.4   IDE Device Configuration Submenus

This submenu is for configuring IDE devices, including:

- Primary IDE master
- Primary IDE slave
- Secondary IDE master
- Secondary IDE slave

**Table 62.   IDE Device Configuration Submenus**

| Feature | Options | Description |
|---|---|---|
| Type | • None<br>• User<br>• **Auto (default)**<br>• CD-ROM<br>• ATAPI Removable<br>• Other ATAPI<br>• IDE Removable | Specifies the IDE configuration mode for IDE devices.<br>*User* allows the LBA Mode Control, Multi-Sector Transfers, Transfer Mode, and Ultra DMA settings to be changed.<br>*Auto* automatically fills in the values for the LBA Mode Control, Multi-Sector Transfers, Transfer Mode, and Ultra DMA settings. |
| Maximum Capacity | No options | Reports the maximum capacity for the hard disk, if the type is User or Auto. |
| LBA Mode Control | • Disabled<br>• **Enabled (default)** | Enables or disables the LBA mode control. |
| Multi-Sector Transfers | • Disabled<br>• **2 Sectors (default)**<br>• 4 Sectors<br>• 8 Sectors<br>• 16 Sectors | Specifies number of sectors per block for  transfers from the hard disk drive to memory.<br>Check the hard disk drive's specifications for optimum setting. |
| Transfer Mode | • Standard<br>• **Fast PIO 1 (default)**<br>• Fast PIO 2<br>• Fast PIO 3<br>• Fast PIO 4<br>• FPIO 3/DMA 1<br>• FPIO 4/DMA 2 | Specifies the method for moving data to/from the drive. |
| Ultra DMA | • **Disabled (default)**<br>• Mode 0<br>• Mode 1<br>• Mode 2 | Specifies the Ultra DMA mode for the drive. |

## 4.4.5 Diskette Configuration Submenu

This submenu is for configuring the diskette drive.

**Table 63. Diskette Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Diskette Controller | • Disabled<br>• **Enabled (default)** | Disables or enables the integrated diskette controller. |
| Diskette A: | • Not Installed<br>• 360 KB, 5¼″<br>• 1.2 MB, 5¼″<br>• 720 KB, 3½″<br>• **1.44/1.25 MB, 3½″ (default)**<br>• 2.88 MB, 3½″ | Specifies the capacity and physical size of diskette drive A. |
| Diskette Write Protect | • **Disabled (default)**<br>• Enabled | Disables or enables write protect for the diskette drive. |

## 4.4.6 Event Log Configuration Submenu

This submenu is for configuring the event logging features.

**Table 64. Event Log Configuration Submenu**

| Feature | Options | Description |
|---|---|---|
| Event log | No options | Indicates if there is space available in the event log. |
| Event log validity | No options | Indicates if the contents of the event log are valid. |
| View event log | [Enter] | Displays the event log. |
| Clear all event logs | • **No (default)**<br>• Yes | Clears the event log after rebooting. |
| Event Logging | • Disabled<br>• **Enabled (default)** | Enables logging of events. |
| ECC Event Logging | • Disabled<br>• **Enabled (default)** | Enables logging of ECC events. |
| Mark events as read | [Enter] | Marks all events as read. |

## 4.4.7   Video Configuration Submenu

This submenu is for configuring video features.

**Table 65.    Video Configuration Submenu**

| Feature | Options | Description |
|---------|---------|-------------|
| Palette Snooping | • **Disabled (default)**<br>• Enabled | Controls the ability of a primary PCI graphics controller to share a common palette with an ISA add-in video card. |
| AGP Aperture Size | • **64 MB (default)**<br>• 256 MB | Specifies the aperture size for the AGP video controller. |

## 4.4.8   Resource Configuration Submenu

This submenu is for configuring the memory and interrupts.

**Table 66.    Resource Configuration Submenu**

| Feature | Options | | Description |
|---------|---------|---|-------------|
| Memory Reservation | • C8000 - CBFFF<br>• CC000 - CFFFF<br>• D0000 - D3FFF<br>• D4000 - D7FFF<br>• D8000 - DBFFF<br>• DC000 - DFFFF | **Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved | Reserves specific upper memory blocks for use by legacy ISA devices. |
| IRQ Reservation | • IRQ3<br>• IRQ4<br>• IRQ5<br>• IRQ7<br>• IRQ10<br>• IRQ11 | **Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved<br>**Available (default)** \| Reserved | Reserves specific IRQs for use by legacy ISA devices.<br>An * (asterisk) displayed next to an IRQ indicates an IRQ conflict. |

# 4.5   Security Menu

This menu is for setting passwords and security features.

**Table 67.   Security Menu**

| Feature | Options | Description |
|---|---|---|
| User Password Is | No options | Reports if there is a user password set. |
| Supervisor Password Is | No options | Reports if there is a supervisor password set. |
| Set User Password | Password can be up to seven alphanumeric characters. | Specifies the user password. |
| Set Supervisor Password | Password can be up to seven alphanumeric characters. | Specifies the supervisor password. |
| Clear User Password | • **No (default)**<br>• Yes | Clears the user password. |
| User Access Level | • **Limited (default)**<br>• No Access<br>• View Only<br>• Full | Controls user access to Setup.<br><br>*No Access* prevents the user from accessing Setup. |
| Unattended Start | • **Disabled (default)**<br>• Enabled | Enables the unattended start feature. When enabled, the computer boots, but the keyboard is locked.  The user must enter a password to unlock the keyboard or boot from a diskette. |

# 4.6 Power Menu

This menu is for setting power management features.

**Table 68.   Power Menu**

| Feature | Options | Description |
|---|---|---|
| Power Management | • Disabled<br>• **Enabled (default)** | Enables or disables the BIOS power management feature. |
| Inactivity Timer | • Off<br>• 1 Minute<br>• 5 Minutes<br>• 10 Minutes<br>• **20 Minutes (default)**<br>• 30 Minutes<br>• 60 Minutes<br>• 120 Minutes | Specifies the amount of time before the computer enters standby mode. |
| Hard Drive | • Disabled<br>• **Enabled (default)** | Enables power management for hard disks during standby and suspend modes. |
| Video Power Down | • Disabled<br>• Standby<br>• **Suspend (default)**<br>• Sleep | Specifies power management for video during standby and suspend modes. |

# 4.7 Boot Menu

This menu is for setting the boot features and the boot sequence.

**Table 69. Boot Menu**

| Feature | Options | Description |
|---|---|---|
| Quiet Boot | • Disabled<br>• **Enabled (default)** | *Disabled* displays normal POST messages.<br>*Enabled* displays OEM logo instead of POST messages. |
| Quick Boot | • Disabled<br>• **Enabled (default)** | Enables the computer to boot without running certain POST tests. |
| Scan User Flash Area | • **Disabled (default)**<br>• Enabled | Enables the BIOS to scan the flash memory for user binary files that are executed at boot time. |
| After Power Failure | • Stays Off<br>• **Last State (default)**<br>• Power On | Specifies the mode of operation if an AC/Power loss occurs.<br>*Power On* restores power to the computer.<br>*Stay Off* keeps the power off until the power button is pressed.<br>*Last State* restores the previous power state before power loss occurred. |
| On Modem Ring | • **Stay Off (default)**<br>• Power On | Specifies how the computer responds to an incoming call on an installed modem when the power is off. |
| On LAN | • Stay Off<br>• **Power On (default)** | Specifies how the computer responds to a LAN wakeup event when the power is off. |
| On PME | • **Stay Off (default)**<br>• Power On | Specifies how the computer responds to a PME wakeup event when the power is off. |
| First Boot Device<br>Second Boot Device<br>Third Boot Device<br>Fourth Boot Device | • Disabled<br>• 1$^{st}$ IDE-HDD<br>• 2$^{nd}$ IDE-HDD<br>• 3$^{rd}$ IDE-HDD<br>• 4$^{th}$ IDE-HDD<br>• Floppy<br>• ARMD-FDD<br>• ARMD-HDD<br>• ATAPI CDROM<br>• SCSI<br>• NETWORK | Specifies the boot sequence from the available devices.  To specify boot sequence, select the boot device with <↑> or <↓> and press <Enter>.<br>The operating system assigns a drive letter to each boot device in the order listed.  Changing the order of the devices changes the drive lettering.<br>Not all of the devices in this list are available as second, third, and fourth boot devices.<br>For a typical system including a diskette drive, a hard disk drive, and a CD-ROM, the default boot devices are:<br>First Boot Device      Floppy<br>Second Boot Device    First IDE-HDD<br>Third Boot Device      ATAPI CD-ROM<br>Fourth Boot Device     Disabled |

## 4.8   Exit Menu

This menu is for exiting the Setup program, saving changes, and loading and saving defaults.

**Table 70.    Exit Menu**

| Feature | Description |
|---------|-------------|
| Exit Saving Changes | Exits and saves the changes in CMOS SRAM. |
| Exit Discarding Changes | Exits without saving any changes made in Setup. |
| Load Setup Defaults | Loads the factory default values for all the Setup options. |
| Load Custom Defaults | Loads the custom defaults for Setup options. |
| Save Custom Defaults | Saves the current values as custom defaults.  Normally, the BIOS reads the Setup values from flash memory.  If this memory is corrupted, the BIOS reads the custom defaults.  If no custom defaults are set, the BIOS reads the factory defaults. |
| Discard Changes | Discards changes without exiting Setup.  The option values present when the computer was turned on are used. |

# 5   Error Messages and Beep Codes

## What This Chapter Contains

## 5.1   BIOS Error Messages

**Table 71.   BIOS Error Messages**

| Error Message | Explanation |
|---|---|
| GA20 Error | An error occurred with Gate-A20 when switching to protected mode during the memory test. |
| Pri Master HDD Error<br>Pri Slave HDD Error<br>Sec Master HDD Error<br>Sec Slave HDD Error | Could not read sector from corresponding drive. |
| Pri Master Drive - ATAPI Incompatible<br>Pri Slave Drive - ATAPI Incompatible<br>Sec Master Drive - ATAPI Incompatible<br>Sec Slave Drive - ATAPI Incompatible | Corresponding drive in not an ATAPI device.  Run Setup to make sure device is selected correctly. |
| A: Drive Error<br>B: Drive Error | No response from diskette drive. |
| Cache Memory Bad | An error occurred when testing L2 cache.  Cache memory may be bad. |
| CMOS Battery Low | The battery may be losing power.  Replace the battery soon. |
| CMOS Display Type Wrong | The display type is different than what has been stored in CMOS.  Check Setup to make sure type is correct. |
| CMOS Checksum Bad | The CMOS checksum is incorrect.  CMOS memory may have been corrupted.  Run Setup to reset values. |
| CMOS Settings Wrong | CMOS values are not the same as the last boot.  These values have either been corrupted or the battery has failed. |
| CMOS Date/Time Not Set | The time and/or date values stored in CMOS are invalid.  Run Setup to set correct values. |
| DMA Error | Error during read/write test of DMA controller. |
| FDC Failure | Error occurred trying to access diskette drive controller. |
| HDC Failure | Error occurred trying to access hard disk controller. |
| Checking NVRAM..... | NVRAM is being checked to see if it is valid. |
| Update OK! | NVRAM was invalid and has been updated. |

**Table 71.    BIOS Error Messages** (continued)

| Error Message | Explanation |
|---|---|
| Updated Failed | NVRAM was invalid but was unable to be updated. |
| Keyboard Is Locked | The system keyboard lock is engaged.  The system must be unlocked to continue to boot. |
| Keyboard Error | Error in the keyboard connection.  Make sure keyboard is connected properly. |
| KB/Interface Error | Keyboard Interface test failed. |
| Memory Size Decreased | Memory size has decreased since the last boot.  If no memory was removed then memory may be bad. |
| Memory Size Increased | Memory size has increased since the last boot.  If no memory was added there may be a problem with the system. |
| Memory Size Changed | Memory size has changed since the last boot.  If no memory was added or removed then memory may be bad. |
| No Boot Device Available | System did not find a device to boot. |
| Off Board Parity Error | A parity error occurred on an offboard card.  This error is followed by an address. |
| On Board Parity Error | A parity error occurred in onboard memory. This error is followed by an address. |
| Parity Error | A parity error occurred in onboard memory at an unknown address. |
| NVRAM/CMOS/PASSWORD cleared by Jumper | NVRAM, CMOS, and passwords have been cleared.  The system should be powered down and the jumper removed. |
| <CTRL_N> Pressed | CMOS is ignored and NVRAM is cleared.  User must enter Setup. |

## 5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires an add-in card (often called a POST card). The POST card can decode the port and display the contents on a medium such as a seven-segment display. These cards can be purchased from JDR Microdevices or other sources.

The following tables provides the POST codes that can be generated by the BIOS. Some codes are repeated in the table because that code applies to more than one operation.

**Table 72.    Uncompressed INIT Code Checkpoints**

| Code | Description of POST Operation |
|------|-------------------------------|
| D0 | NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting. |
| D1 | Keyboard controller BAT test, CPU ID saved, and going to 4GB flat mode. |
| D3 | Do necessary chipset initialization, start memory refresh, do Memory sizing. |
| D4 | Verify base memory. |
| D5 | Init code to be copied to segment 0 and control to be transferred to segment 0. |
| D6 | Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS. |
| D7 | Find Main BIOS module in ROM image. |
| D8 | Uncompress the main BIOS module. |
| D9 | Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM. |

**Table 73.    Boot Block Recovery Code Check Points**

| Code | Description of POST Operation |
|------|-------------------------------|
| E0 | Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller, interrupt controller. |
| E8 | Initialize extra (Intel Recovery) Module. |
| E9 | Initialize floppy drive. |
| EA | Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code. |
| EB | Booting from floppy failed, look for ATAPI (LS120, Zip) devices. |
| EC | Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code. |
| EF | Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9). |

**Table 74.    Runtime Code Uncompressed in F000 Shadow RAM**

| Code | Description of POST Operation |
|------|-------------------------------|
| 03 | NMI is Disabled.  To check soft reset/power-on. |
| 05 | BIOS stack set.  Going to disable Cache if any. |
| 06 | POST code to be uncompressed. |
| 07 | CPU init and CPU data area init to be done. |
| 08 | CMOS checksum calculation to be done next. |
| 0B | Any initialization before keyboard BAT to be done next. |
| 0C | KB controller I/B free.  To issue the BAT command to keyboard controller. |
| 0E | Any initialization after KB controller BAT to be done next. |
| 0F | Keyboard command byte to be written. |
| 10 | Going to issue Pin-23,24 blocking/unblocking command. |
| 11 | Going to check pressing of <INS>, <END> key during power-on. |
| 12 | To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed.  Going to disable DMA and Interrupt controllers. |
| 13 | Video display is disabled and port-B is initialized.  Chipset init about to begin. |
| 14 | 8254 timer test about to start. |
| 19 | About to start memory refresh test. |
| 1A | Memory Refresh line is toggling.  Going to check 15µs ON/OFF time. |
| 23 | To read 8042 input port and disable Megakey GreenPC feature.  Make BIOS code segment writeable. |
| 24 | To do any setup before Int vector init. |
| 25 | Interrupt vector initialization to begin.  To clear password if  necessary. |
| 27 | Any initialization before setting video mode to be done. |
| 28 | Going for monochrome mode and color mode setting. |
| 2A | Different buses init (system, static, output devices) to start if present.  (See Section 5.3 for details of different buses.) |
| 2B | To give control for any setup required before optional video ROM check. |
| 2C | To look for optional video ROM and give control. |
| 2D | To give control to do any processing after video ROM returns control. |
| 2E | If EGA/VGA not found then do display memory R/W test. |
| 2F | EGA/VGA not found. Display memory R/W test about to begin. |
| 30 | Display memory R/W test passed.  About to look for the retrace checking. |
| 31 | Display memory R/W test or retrace checking failed.  To do alternate Display memory R/W test. |
| 32 | Alternate Display memory R/W test passed.  To look for the alternate display retrace checking. |
| 34 | Video display checking over.  Display mode to be set next. |
| 37 | Display mode set.  Going to display the power on message. |
| 38 | Different buses init (input, IPL, general devices) to start if present.  (See Section 5.3 for details of different buses.) |
| 39 | Display different buses initialization error messages.  (See Section 5.3 for details of different buses.) |
| 3A | New cursor position read and saved.  To display the Hit <DEL> message. |

continued

**Table 74.    Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|------|-------------------------------|
| 40 | To prepare the descriptor tables. |
| 42 | To enter in virtual mode for memory test. |
| 43 | To enable interrupts for diagnostics mode. |
| 44 | To initialize data to check memory wrap around at 0:0. |
| 45 | Data initialized.  Going to check for memory wrap around at 0:0 and finding the total system memory size. |
| 46 | Memory wrap around test done.  Memory size calculation over.  About to go for writing patterns to test memory. |
| 47 | Pattern to be tested written in extended memory. Going to write patterns in base 640k memory. |
| 48 | Patterns written in base memory. Going to find out amount of memory below 1M memory. |
| 49 | Amount of memory below 1M found and verified.  Going to find out amount of memory above 1M memory. |
| 4B | Amount of memory above 1M found and verified.  Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh). |
| 4C | Memory below 1M cleared.  (SOFT RESET) Going to clear memory above 1M. |
| 4D | Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h). |
| 4E | Memory test started.  (NOT SOFT RESET) About to display the first 64k memory size. |
| 4F | Memory size display started.  This will be updated during memory test.  Going for sequential and random memory test. |
| 50 | Memory testing/initialization below 1M complete.  Going to adjust displayed memory size for relocation/ shadow. |
| 51 | Memory size display adjusted due to relocation/ shadow.  Memory test above 1M to follow. |
| 52 | Memory testing/initialization above 1M complete.  Going to save memory size information. |
| 53 | Memory size information is saved.  CPU registers are saved.  Going to enter in real mode. |
| 54 | Shutdown successful, CPU in real mode.  Going to disable gate A20 line and disable parity/NMI. |
| 57 | A20 address line, parity/NMI disable successful.  Going to adjust memory size depending on relocation/shadow. |
| 58 | Memory size adjusted for relocation/shadow.  Going to clear Hit <DEL> message. |
| 59 | Hit <DEL> message cleared.  <WAIT...> message displayed.  About to start DMA and interrupt controller test. |
| 60 | DMA page register test passed.  To do DMA#1 base register test. |
| 62 | DMA#1 base register test passed.  To do DMA#2 base register test. |
| 65 | DMA#2 base register test passed.  To program DMA unit 1 and 2. |
| 66 | DMA unit 1 and 2 programming over.  To initialize 8259 interrupt controller. |
| 7F | Extended NMI sources enabling is in progress. |
| 80 | Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command. |
| 81 | Keyboard reset error/stuck key found.  To issue keyboard controller interface test command. |
| 82 | Keyboard controller interface test over.  To write command byte and init circular buffer. |
| 83 | Command byte written, global data init done. To check for lock-key. |

**Table 74.    Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|------|-------------------------------|
| 84 | Lock-key checking over.  To check for memory size mismatch with CMOS. |
| 85 | Memory size check done.  To display soft error and check for password or bypass setup. |
| 86 | Password checked.  About to do programming before setup. |
| 87 | Programming before setup complete.  To uncompress SETUP code and execute CMOS setup. |
| 88 | Returned from CMOS setup program and screen is cleared.  About to do programming after setup. |
| 89 | Programming after setup complete.  Going to display power on screen message. |
| 8B | First screen message displayed.  <WAIT...> message displayed.  PS/2 Mouse check and extended BIOS data area allocation to be done. |
| 8C | Setup options programming after CMOS setup about to start. |
| 8D | Going for hard disk controller reset. |
| 8F | Hard disk controller reset done.  Floppy setup to be done next. |
| 91 | Floppy setup complete.  Hard disk setup to be done next. |
| 95 | Init of different buses optional ROMs from C800 to start.  (See Section 5.3 for details of different buses.) |
| 96 | Going to do any init before C800 optional ROM control. |
| 97 | Any init before C800 optional ROM control is over.  Optional ROM check and control will be done next. |
| 98 | Optional ROM control is done.  About to give control to do any required processing after optional ROM returns control and enable external cache. |
| 99 | Any initialization required after optional ROM test over.  Going to setup timer data area and printer base address. |
| 9A | Return after setting timer and printer base address.  Going to set the RS-232 base address. |
| 9B | Returned after RS-232 base address.  Going to do any initialization before Coprocessor test. |
| 9C | Required initialization before Coprocessor is over.  Going to initialize the Coprocessor next. |
| 9D | Coprocessor initialized.  Going to do any initialization after Coprocessor test. |
| 9E | Initialization after Coprocessor test is complete.  Going to check extended keyboard, keyboard ID and num-lock. |
| A2 | Going to display any soft errors. |
| A3 | Soft error display complete.  Going to set keyboard typematic rate. |
| A4 | Keyboard typematic rate set.  To program memory wait states. |
| A5 | Going to enable parity/NMI. |
| A7 | NMI and parity enabled.  Going to do any initialization required before giving control to optional ROM at E000. |
| A8 | Initialization before E000 ROM control over.  E000 ROM to get control next. |
| A9 | Returned from E000 ROM control.  Going to do any initialization required after E000 optional ROM control. |
| AA | Initialization after E000 optional ROM control is over.  Going to display the system configuration. |
| AB | Put INT13 module runtime image to shadow. |
| AC | Generate MP for multiprocessor support (if present). |
| AD | Put CGA INT10 module (if present) in Shadow. |

continued

**Table 74. Runtime Code Uncompressed in F000 Shadow RAM** (continued)

| Code | Description of POST Operation |
|------|-------------------------------|
| AE | Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow. |
| B1 | Going to copy any code to specific area. |
| 00 | Copying of code to specific area done.  Going to give control to INT-19 boot loader. |

# 5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at the following checkpoints to do various tasks.

| Checkpoint | Description |
|------------|-------------|
| 2A | Different buses init (system, static, output devices) to start if present. |
| 38 | Different buses init (input, IPL, general devices) to start if present. |
| 39 | Display different buses initialization error messages. |
| 95 | Init of different buses optional ROMs from C800 to start. |

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution.  In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines.  The high byte of the checkpoint is the indication of which routine is being executed in the different buses.  The upper nibble of the high byte indicates the function that is being executed:

| Value | Description |
|-------|-------------|
| 0 | func#0, disable all devices on the bus concerned. |
| 1 | func#1, static devices init on the bus concerned. |
| 2 | func#2, output device init on the bus concerned. |
| 3 | func#3, input device init on the bus concerned. |
| 4 | func#4, IPL device init on the bus concerned. |
| 5 | func#5, general device init on the bus concerned. |
| 6 | func#6, error reporting for the bus concerned. |
| 7 | func#7, add-on ROM init for all buses. |

The lower nibble of the high byte indicates the bus on which the routines are being executed:

| Value | Description |
|-------|-------------|
| 0 | Generic DIM (Device Initialization Manager). |
| 1 | On-board System devices. |
| 2 | ISA devices. |
| 3 | EISA devices. |
| 4 | ISA PnP devices. |
| 5 | PCI devices. |

## 5.4  BIOS Beep Codes

Whenever a recoverable error occurs during power-on self test (POST), the BIOS displays an error message describing the problem.  The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones.  For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail.  Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

**Table 75.   Beep Codes**

| Beep | Description |
|------|-------------|
| 1 | Refresh failure |
| 2 | Parity can not be reset |
| 3 | First 64k memory failure |
| 4 | Timer not operational |
| 5 | Processor failure (Reserved for historic reason, not used any more) |
| 6 | Memory not installed |
| 7 | Exception interrupt error |
| 8 | Display memory R/W error |
| 9 | ROM checksum error (Reserved for historic reason, not used any more) |
| 10 | CMOS Shutdown register test error |
| 11 | Invalid BIOS (e.g. POST module not found, etc.) |

# 6 Specifications and Customer Support

## What This Chapter Contains

## 6.1 Online Support

Find information about Intel motherboards at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://www.intel.com/support/motherboards/desktop

## 6.2 Specifications

The motherboard complies with the following specifications:

**Table 76. Compliance with Specifications**

| Specification | Description | Revision Level |
|---|---|---|
| AC '97 | Audio Codec '97 Component Specification | Revision 2.1, May 22, 1998, Intel Corporation. This specification is available at: http://developer.intel.com/pc-supp/platform/ac97/ |
| ACPI | Advanced Configuration and Power Interface specification | Revision 1.0a, July 1, 1998, Intel Corporation, Microsoft Corporation, and Toshiba Corporation. The specification is available at: http://www.teleport.com/~acpi/ |
| AGP | Accelerated Graphics Port Interface Specification (1X and 2X) | Revision 2.0, May 4, 1998, Intel Corporation. The specification is available through the Accelerated Graphics Implementors Forum at: http://www.agpforum.org/ |
| AMI BIOS | American Megatrends BIOS Specification | AMIBIOS 98. This specification is available at http://www.amibios.com |
| APM | Advanced Power Management BIOS interface specification | Revision 1.2, February, 1996, Intel Corporation and Microsoft Corporation. |
| ATA-3 | Information Technology - AT Attachment-3 Interface | X3T10/2008D Revision 6. The specification is available at the ATA Anonymous FTP Site: fission.dt.wdc.com. |
| ATAPI | ATA Packet Interface for CD-ROMs | SFF-8020i Revision 2.5. (SFF) Fax Access: (408) 741-1600. |

**Table 76.   Compliance with Specifications** (continued)

| Specification | Description | Revision Level |
|---|---|---|
| ATX | ATX form factor specification | Revision 2.03, December 1998, Intel Corporation.  The specification is available at: http://developer.intel.com/design/motherbd/atx.htm |
| El Torito | Bootable CD-ROM format specification | Version 1.0, January 25, 1995 Phoenix Technologies Ltd., and IBM Corporation.  The El Torito specification is available on the Phoenix Web site at:  http://www.phoenix.com/products/specs.html |
| EPP | Enhanced Parallel Port | IEEE 1284 standard, Mode [1 or 2], v1.7. |
| IrDA | Serial Infrared Physical Layer Link specification | Version 1.1, October 17, 1995 Infrared Data Association. |
| microATX | microATX Motherboard Interface Specification | Version 1.0, December, 1997 Intel Corporation.  The specification is available at: http://www.teleport.com/~microatx/spec/ |
| PCI | PCI Local Bus Specification | Revision 2.2, December 18, 1998, PCI Special Interest Group. |
| | PCI Power Management Interface Specification | Revision 1.1, December 18, 1998, PCI Special Interest Group. |
| | | These specifications can be ordered at: |
| | | http://www.pcisig.com/ |
| Plug and Play | Plug and Play BIOS specification | Version 1.0a, May 5, 1994 Compaq Computer Corporation, Phoenix Technologies Ltd., and Intel Corporation. |
| SDRAM DIMMs (64-and 72-bit) | PC SDRAM Unbuffered DIMM Specification PC SDRAM DIMM Specification PC Serial Presence Detect (SPD) Specification | Revision 1.0, February , 1998, Intel Corporation. Revision 1.63, October, 1998, Intel Corporation. Revision 1.2A, December, 1997, Intel Corporation. These specifications are available at: http://developer.intel.com/design/chipsets/memory/ |
| SMBIOS | System Management BIOS Reference Specification | Version 2.3, August 12, 1998, American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, Phoenix Technologies Ltd., and SystemSoft Corporation.  The specification is available at:  http://developer.intel.com/ial/WfM/design/smbios/ |
| UHCI | Universal Host Controller Interface (UHCI) Design Guide | Revision 1.1, March 1996 Intel Corporation.  This specification is available at: http://www.usb.org/developers/ |
| USB | Universal serial bus specification | Revision 1.1, September 23, 1998 Compaq Computer Corporation, Digital Equipment Corporation, IBM PC Company, Intel Corporation, Microsoft Corporation, NEC, and Northern Telecom. This specification is available at: http://www.usb.org/developers/ |