Intel® Desktop Board D850MD Specification Update

Release Date: December 2002

Order Number: A72586-010

The Intel® Desktop Board D850MD may contain design defects or errors known as errata, which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
September 2001	-001	This document is the first Specification Update for the Intel® Desktop Board D850MD.
November 2001	-002	Updated General Information section.
January 2002	-003	Updated General Information section. Added Specification Clarifications 1, 2.
February 2002	-004	Added Erratum 1. Updated General Information.
March 2002	-005	Added Specification Changes 1, 2.
April 2002	-006	Added Specification Change 3.
June 2002	-007	Added Erratum 2.
September 2002	-008	Added Specification Change 4. Removed Printed Board Assembly (PBA) information from the document, as this reference is no longer valid. Updated the Legal Disclaimer Section.
October 2002	-009	Added Specification Change 5. Added Erratum 3.
December 2002	-010	Added Erratum 4.

PREFACE

This document is an update to the specifications contained in the *Intel® Desktop Board D850MD Technical Product Specification* (Order Number A65145). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order number 249199) for specification updates concerning the Intel Pentium 4 processor and that may apply to the desktop board D850MD. Unless otherwise noted in this document, it should be assumed that any processor errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel®* 82850 *Chipset:* 82850 *Memory Controller Hub (MCH) Specification Update* (Order Number 298247) for specification updates concerning the 82850 MCH Controller and that may apply to the desktop board D850MD. Unless otherwise noted in this document, it should be assumed that any MCH errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Specification Update* (Order Number 298242) for specification updates concerning the 82802BA I/O Controller Hub and that may apply to the desktop board D850MD. Unless otherwise noted in this document, it should be assumed that any ICH 2 errata for a given stepping are applicable to the Altered Assembly (AA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D850MD's behavior to deviate from published specifications. Hardware and software designed to be used with any given Altered Assembly (AA) and BIOS revision level must assume that all errata documented for that AA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

Specification Update for the Intel® Desktop Board D850MD

GENERAL INFORMATION

Basic Desktop Board D850MD Identification Information

AA Revision	BIOS Revision	Notes
A52481-302	MV85010A.86A.0005.P02	1-5
A52481-303	MV85010A.86A.0005.P02	1-5
A52481-304	MV85010A.86A.0009.P04	1-5
A52481-401	MV85010A.86A.0011.P05	1-5
A56430-302	MV85010A.86A.0005.P02	1-5
A56430-303	MV85010A.86A.0005.P02	1-5
A56430-304	MV85010A.86A.0005.P02	1-5
A56430-305	MV85010A.86A.0009.P04	1-5
A56430-401	MV85010A.86A.0011.P05	1-5
A71258-303	MV85010A.86A.0005.P02	1-5
A71258-304	MV85010A.86A.0005.P02	1-5
A71258-305	MV85010A.86A.0009.P04	1-5
A71258-401	MV85010A.86A.0011.P05	1-5
A71266-303	MV85010A.86A.0005.P02	1-5
A71266-304	MV85010A.86A.0009.P04	1-5
A71266-401	MV85010A.86A.0011.P05	1-5

NOTES:

1. The AA number is found on a small label on the component side of the board.
2. The 82850 Chipset kit used on this AA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
KC82850 MCH	A3	SL5HA
82801BA ICH	B4	SL59Z
82802AB 4Mbit FWH	A1	SB48

3. Refer to the *Intel® Pentium® 4 Processor Specification Update* (Order Number 249199) for errata related to the Pentium 4 processor and that may apply to the desktop board D850MD.
4. Refer to the *Intel® 82850 Memory Controller Hub (MCH) Specification Update* (Order Number 290659) for errata related to the 82850 MCH that may apply to the desktop board D850MD.
5. Refer to the *Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Specification Update* (Order Number 298242) for errata related to the ICH 2 Controller Hub that may apply to the desktop board D850MD.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes that apply to the desktop board D850MD. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

Doc:	Document change or update that will be implemented.
Fix:	This erratum is intended to be fixed in a future revision of the desktop board, driver, or BIOS.
Fixed:	This erratum has been previously fixed.
NoFix:	There are no plans to fix this erratum.
Shaded:	This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Support for faster Intel® Pentium® 4 processors
2	Doc	Third paragraph in Section 1.14.2.2 will be removed
3	Doc	Support for additional Intel Pentium 4 processors
4	Doc	Support for faster Intel Pentium 4 processor
5	Doc	Support for faster Intel Pentium 4 processors
NO.	**PLANS**	**ERRATA**
1	Fix	System hang during POST may occur when using certain USB cameras
2	Fixed	VCCPVID signal noise may cause intermittent no boot condition, system shut down, or system lock-ups
3	Fixed	Wake from an ACPI sleep state using wake methodologies may fail
4	NoFix	System boot time may be excessive when using ECC memory
NO.	**PLANS**	**SPECIFICATION CLARIFICATIONS**
1	Doc	Change to description of Section 2.6, Interrupts
2	Doc	Change to description of Section 2.7, PCI Interrupt Routing Map

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *Desktop Board D850MD Technical Product Specification* (Order Number A65145). All Specification Changes will be incorporated into a future version of that specification.

1. Support For Faster Intel® Pentium® 4 Processors

Section 1.6, Processor, will change in its entirety as follows:

1.6 Processor

⚠ CAUTION

Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D850MD/D850MD Specification Update *for the most up-to-date list of supported processors for these boards.*

The D850MD and D850MD boards support a single Pentium® 4 processor (in a 478-pin socket) with a system bus of 400 MHz. The D850MD and D850MD boards support the processors listed in Table 5. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	Up to 2.0 GHz	400 MHz	256 KB
	2.0 and 2.1 GHz	400 MHz	512 KB

⚠ CAUTION

Use only an ATX12V-compliant power supply with the D850MD and D850MD boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel® Pentium 4 processor and the Intel® 850 chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the D850MD and D850MD boards. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.3, page 18
Processor usage	Section 1.3, page 18
Power supply connectors	Section 2.8.2.3, page 60

2. Third Paragraph in Section 1.14.2.2 Will be Removed

Section 1.14.2.2, Fan Connectors will change in its entirety as follows:

1.14.2.2 Fan Connectors

The D850MD and D850MD boards have two fan connectors with thermal control signals (fan 1 and fan 2) that are used to switch the fans on and off as determined by the thermal sensors.

The ambient temperature of a D850MD- or D850MD-based system is thermally monitored by separate temperature sensors that control voltage to the fan 1 and fan 2 connectors. If the fans attached to these connectors provide a tachometer signal, the sensor reports the fan speed to the hardware monitor component.

Table 12 summarizes the functions of the four fan connectors.

Table 12. Fan Connector Descriptions

Feature	Processor Fan	Fan 1	Fan 2	Fan 3 (Note 1)
+12 V DC connection	Yes	Yes	Yes	Yes
Tachometer output	Yes	No	Yes	No
Controllable	No	Yes	Yes	Yes (Note 2)
Fan is on in the ACPI S0 or S1 states	Yes	Yes	Yes	Yes
Fan is off in the ACPI S3, S4, and S5 states	Yes	Yes	Yes	Yes

Notes:

1. This fan is present on the D850MD board only.
2. Fan 3 uses the same controls as fan 2. If fan 2 is switched off, fan 3 is also off.

For information about	Refer to
The location of the fan connectors	Figure 14, page 60
The signal names of the fan connectors	Section 2.8.2.3, page 58

3. Support For Additional Intel® Pentium® 4 Processors

Section 1.6, Processor, will change in its entirety as follows:

1.6 Processor

CAUTION

Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D850MD/D850MD Specification Update *for the most up-to-date list of supported processors for these boards.*

The D850MD and D850MD boards support a single Pentium® 4 processor (in a 478-pin socket) with a system bus of 400 MHz. The D850MD and D850MD boards support the processors listed in Table 2. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	Up to 2.0 GHz	400 MHz	256 KB
	1.6, 1.8, 2.0 and 2.2 GHz	400 MHz	512 KB

CAUTION

Use only an ATX12V compliant power supply with the D850MD and D850MD boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel® Pentium 4 processor and the Intel® 850 chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the D850MD and D850MD boards. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Most recent D850MD Specification Update
Processor usage	Section 1.3, page 18
Power supply connectors	Section 2.8.2.3, page 60

4. Support For Faster Intel® Pentium® 4 Processor

Section 1.6, Processor, will change in its entirety as follows:

1.6 Processor

CAUTION

Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D850EMD2/D850EMV2 Specification Update *for the most up-to-date list of supported processors for these boards.*

The desktop boards D850EMD2/D850EMV2 support a single Pentium® 4 processor (in a µPGA478 socket) with a system bus of 400/533 MHz. Table 5 lists the supported processors.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	1.60A, 1.70A, 1.80A, 2.0A, 2.2, and 2.4 GHz	400 MHz	512 KB
	1.4, 1.5, 1.6, 1.7, 1.8, 1.9, and 2.0 GHz	400 MHz	256 KB

The list of supported processors for the desktop boards D850EMD2/D850EMV2 is available from Intel's World Wide Web site. All supported onboard memory can be cached. See the processor's data sheet for cachability limits.

CAUTION

Use only an ATX12V-compliant power supply with these desktop boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel® Pentium 4 processor and the Intel® 850E chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the board. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.3, page 18
Processor usage	Section 1.3, page 18
Power supply connectors	Section 2.8.2.3, page 60

NOTE

BIOS revision MV85010A.86A.0016.P07 or greater required for the board to properly support 1.60A GHz/400 MHz/512KB and 1.7 GHz/400MHz/256KB Pentium® 4 or later processors.

NOTE

BIOS revision MV85010A.86A.0016.P07 or greater and board revisions A71904-300, A71906-300, A56420-300, A56423-300, A73829-300, or greater are required for the board to properly support 2.4 GHz Pentium 4 processors.

5. Support For Faster Intel® Pentium® 4 Processor

Section 1.6, Processor, will change in its entirety as follows:

1.6 Processor

CAUTION

Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D850EMD2/D850EMV2 Specification Update *for the most up-to-date list of supported processors for these boards.*

The desktop boards D850EMD2/D850EMV2 support a single Pentium 4 processor (in a µPGA478 socket) with a system bus of 400/533 MHz. Table 5 lists the supported processors.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium® 4 processor	1.6A, 1.7A, 1.8A, 2A, 2.20, and 2.40, 2.50, and 2.60 GHz	400 MHz	512 KB
Pentium 4 processor	1.4, 1.5, 1.6, 1.7, 1.8, 1.9, and 2 GHz	400 MHz	256 KB

The list of supported processors for the desktop boards D850EMD2/D850EMV2 is available from Intel's World Wide Web site. All supported onboard memory can be cached. See the processor's data sheet for cachability limits.

CAUTION

Use only an ATX12V-compliant power supply with these desktop boards. ATX12V power supplies have two power leads that provide required supplemental power for the Intel® Pentium® 4 processor and the Intel® 850E chipset. Always connect the 20-pin and 4-pin leads of the ATX12V power supply to the corresponding connectors on the board. Otherwise, the board and the processor could be damaged.

Do not use a standard ATX power supply. Doing so could damage the board and the processor.

For information about	Refer to
Processor support	Section 1.3, page 18
Processor usage	Section 1.3, page 18
Power supply connectors	Section 2.8.2.3, page 60

NOTE

BIOS revision MV85010A.86A.0016.P07 or greater required for the board to properly support 1.60A GHz/400 MHz/512KB and 1.7 GHz/400MHz/256KB Pentium 4 or later processors.

NOTE

BIOS revision MV85010A.86A.0016.P07 or greater and board revisions A71904-300, A71906-300, A56420-300, A56423-300, A73829-300, or greater are required for the board to properly support 2.4 GHz Pentium® 4 processors.

NOTE

BIOS revision MV85010A.86A.0038.P15 or greater and board revisions A71904-300, A71906-300, A56420-300, A56423-300, A73829-300, or greater are required for the board to properly support 2.50 GHz or greater Pentium 4 processors.

ERRATA

1. System Hang During POST May Occur When Using Certain USB Cameras

PROBLEM: During the system boot, certain USB cameras may cause a hang during POST if the camera is on during the boot process.

IMPLICATION: Some USB cameras may cause a system hang if the camera is on during system boot due to the BIOS incorrectly identifying the camera as a bootable device.

WORKAROUND: Ensure that the USB camera is off during the system boot process.

STATUS: This erratum may be fixed in a future BIOS revision.

2. VCCPVID Signal Noise May Cause Intermittent No Boot Condition, System Shut Down, or System Lock-ups

PROBLEM: Excessive noise on the VCCPVID voltage regulator trace on D850MD –3xx series desktop boards.

IMPLICATION: Due to the signal noise on the voltage regulator VCCPVID line, D850MD –3xx series boards may experience intermittent system shut downs, boot failures, or system lock-ups.

WORKAROUND: Users with D850MD –3xx series desktop boards can utilize Intel® Pentium® 4 processors with 256KB cache, in the µPGA 478 package.

STATUS: This erratum was fixed in board revisions AA A52481-401, A56430-401, A71258-401, A71266-401 and later.

3. Wake From an ACPI Sleep State Using Wake Methodologies May Fail

PROBLEM: The desktop board hardware leaves the Resume Well Power OK (RSM_PWROK) signal deasserted before and after the resume well power (VccSus3_3 and VccSus1_8) is valid, instead of asserting it for 10 ms after valid power, which is required by the Intel® 82801BA I/O Controller Hub 2 (ICH2) and Intel® 82801BAM I/O Controller Hub 2 Mobile (ICH2-M) Datasheet (order number 290687). The result is that LAN wake attempts may fail.

NOTE: Wake from LAN* using the MagicPacket* utility will not be affected by this errata.

IMPLICATION: Users that take advantage of LAN wake methods to wake systems from an ACPI sleep state may experience some wake failures.

WORKAROUND: None.

STATUS: This issue was fixed in BIOS revision MV85010A.86A.0038.P15.

4. System Boot Time May be Excessive When Using ECC Memory

PROBLEM: A blank screen may occur for as long as one minute during POST while the system is booting, when ECC memory is utilized.

IMPLICATION: When BIOS detects ECC memory during the system boot process, BIOS will run memory scans multiple times resulting in a delayed POST (up to one minute) making the system seem unresponsive.

WORKAROUND: None.

STATUS: This erratum will not be fixed.

SPECIFICATION CLARIFICATIONS

The Specification Clarifications listed in this section apply to the *Desktop Board D850MD Technical Product Specification* (Order Number A65145). All Specification Clarifications will be incorporated into a future version of that specification.

1. Change to Description of Section 2.6, Interrupts

Section 2.6, Interrupts, will change in its entirety as follows:

2.6 Interrupts

The Interrupts can go through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the Intel® ICH2 component. The PIC is supported in Windows* 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and support a total of 24 interrupts.

Table 17. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for Intel ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)
16	AGP video (through PIRQA) (Note 2)

continued

Table 17. Interrupts (continued)

IRQ	System Resource
17	AC' 97 Audio/User Available (through PIRQB) (Note 2)
18	User available (through PIRQC) (Note 2)
19	Intel® ICH2 USB Controller #1 (through PIRQD) (Note 2)
20	Intel ICH2 LAN (optional) (through PIRQE) (Note 2)
21	OHCI Controller #2/User available (through PIRQF) (Note 2)
22	EHCI Controller #1/User available (through PIRQG) (Note 2)
23	Intel ICH2 USB Controller #2/ User Available (through PIRQH) (Note 2)

Note 1: Default, but can be changed to another IRQ.

Note 2: Available in APIC mode only.

2. Change to Description of Section 2.7, PCI Interrupt Routing Map

Section 2.7, PCI Interrupt Routing Map, will change in its entirety as follows:

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The Intel ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D850MD and D850MD boards and therefore share the same interrupt. Table 18 shows an example of how the PIRQ signals are routed on the D850MD and D850MD boards.

For example, using Table 18 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 4. In PCI bus connector 4, INTA is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 4 now shares interrupts with these onboard interrupt sources.

Table 18. PCI Interrupt Routing Map

PCI Interrupt Source	Intel® ICH2 PIRQ Signal Name				
	PIRQF	PIRQG	PIRQH	PIRQB	Other
AGP connector				INTB	INTA to PIRQA
Intel ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
Intel ICH2 USB controller #2			INTC		
Intel ICH2 Audio / Modem				INTB	
Intel ICH2 LAN					INTA to PIRQE
OHCI controller 1 (Note 1)					INTD to PIRQA
OHCI controller 2 (Note 1)					INTC to PIRQB
EHCI controller (Note 1)					INTH to PIRQC
PCI Bus Connector 1	INTA	INTB	INTC	INTD	
PCI Bus Connector 2	INTD	INTA	INTB	INTC	
PCI Bus Connector 3	INTC	INTD	INTA	INTB	
PCI Bus Connector 4 (Note 2)	INTB	INTC	INTD	INTA	
PCI Bus Connector 5 (Note 2)	INTA	INTB	INTC	INTD	

Notes:

1. USB 2.0 option only
2. D850MD board only

NOTE

In PIC mode, the Intel ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12,14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In APIC mode, the allocation of PIRQ lines to IRQ signals is as shown in Table 18.