Intel® Desktop Board D845HV/D845WN

Technical Product Specification

August 2001

Order Number: A65136-001

The Intel® Desktop Boards D845HV/D845WN may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D845HV/D845WN Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D845HV/D845WN Technical Product Specification.	August 2001

This product specification applies to only standard D845HV and D845WN boards with BIOS identifier HV84510A.86A.

Changes to this specification will be published in the Intel Desktop Board D845HV/D845WN Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for these Intel® Desktop Boards: D845HV and D845WN. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the D845HV and D845WN boards and their components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the D845HV and D845WN boards
2	A map of the resources of the boards
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, and POST codes

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the D845HV and D845WN boards, and X is the instance of the particular part at that general location. For example, J5J1 is a connector, located at 5J. It is the first connector in the 5J area.
GB	Gigabyte (1,073,741,824 bytes)
GB/sec	Gigabytes per second
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

Contents

2 Technical Reference

3 Overview of BIOS Features

Tables

1 Product Description

What This Chapter Contains

1.1 Board Differences

This TPS describes these Intel® Desktop boards: D845HV and D845WN. The boards are identical with the exception of the items listed below. Table 1 summarizes the differences between these boards.

Table 1. Summary of Board Differences

D845HV	• microATX Form Factor (9.60 inches by 9.60 inches) • Three PCI bus connectors Refer also to Table 3, page 13 for a list of manufacturing options specific to D845HV board only
D845WN	• ATX Form Factor (12.00 inches by 9.60 inches) • Six PCI bus connectors

NOTE

Most of the illustrations in this document show only the D845HV board. When there are significant differences between the two boards, illustrations of both boards are provided.

1.2 Overview

1.2.1 Feature Summary

Table 2 summarizes the D845HV and D845WN boards' major features.

Table 2. Feature Summary

Form Factor	D845HV: microATX (9.60 inches by 9.60 inches) D845WN: ATX (12.00 inches by 9.60 inches)
Processor	• Support for an Intel® Pentium® 4 processor in an mPGA478 socket • 400 MHz system bus
Memory (Refer also to Table 3, page 13)	• Three 168-pin SDRAM Dual Inline Memory Module (DIMM) sockets • Support for single-sided or double-sided DIMMs (PC133 only) • Support for up to 3 GB system memory **NOTE:** *The D845HV/D845WN boards have been designed to support DIMMs based on 512 Mbit technology for a maximum onboard capacity of up to 3 GB, but this technology has not been validated on this board. Please refer to the following Intel web sites. For the D845HV board:* http://developer.intel.com/design/motherbd/hv/hv_mem.htm *For the D845WN board:* http://developer.intel.com/design/motherbd/wn/wn_mem.htm
Chipset	Intel® 845 Chipset, consisting of: • Intel® 82845 Memory Controller Hub (MCH) • Intel® 82801BA I/O Controller Hub (ICH2) • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
Video	AGP connector supporting 1.5 V 4X AGP cards
I/O Control (Refer also to Table 3, page 13)	SMSC LPC47M142 LPC Bus I/O controller
Peripheral Interfaces (Refer also to Table 3, page 13)	• Up to seven Universal Serial Bus (USB) ports • Two serial ports • One parallel port • IrDA†-compliant infrared port • Two IDE interfaces with UDMA 33, ATA-66/100 support • One diskette drive interface • PS/2† keyboard and mouse ports • Three fan connectors
Expansion Capabilities	• D845HV: Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 1) • D845WN: Six PCI bus add-in card connectors (SMBus routed to PCI bus connector 1)
BIOS	• Intel/AMI BIOS (resident in the Intel 82802AB 4 Mbit FWH) • Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and SMBIOS

continued

Table 2. Feature Summary (continued)

Instantly Available PC Technology	• Support for PCI Local Bus Specification Revision 2.2 • Suspend to RAM support • Wake on PCI, CNR, RS-232, front panel, PS/2 devices, and USB ports

For information about	Refer to
The board's compliance level with ACPI, Plug and Play, and SMBIOS.	Section 1.4, page 17

1.2.2 Manufacturing Options

Table 3 describes the D845HV and D845WN boards' manufacturing options. Not every manufacturing option is available in all marketing channels. Please contact your Intel representative to determine which manufacturing options are available to you.

Table 3. Manufacturing Options

Audio	Audio subsystem for AC 97 processing using the Analog Devices AD1885 codec
CNR	One Communication and Networking Riser (CNR) connector (slot shared with PCI bus connector 3 on the D845HV board and with PCI bus connector 6 on the D845WN board)
LAN	Intel® 82562ET 10/100 Mbit/sec Platform LAN Connect (PLC) device
Hardware Monitor Subsystem	• Voltage sense to detect out of range power supply voltages • Thermal sense to detect out of range thermal values • Two fan sense inputs used to monitor fan activity
The items listed below are component changes for an alternate configuration of the D845HV board	
• Delete the auxiliary front panel power/sleep/message-waiting LED connector (shown on page 68) • Delete the front chassis fan connector (shown on page 58) • Delete the Mic-in pre-amp for boards equipped with the audio subsystem (described on page 32) • Delete the SCSI hard drive activity LED connector (shown on pages 61 and 62) • Delete the serial port B connector (shown on page 68) • Delete the standby power indicator LED (shown on page 44) • Delete the third DIMM socket (shown on pages 14 and 15) • Delete the two USB connectors adjacent to the PS/2 connectors on the back panel (shown on page 52) • Delete the 47 Ω inductive speaker (described on page 126) • Replace I/O controller with SMSC LPC47M132 LPC bus I/O controller (functionally equivalent to SMSC LPC47M142 LPC bus I/O controller but without an integrated USB hub) (described on page 31)	

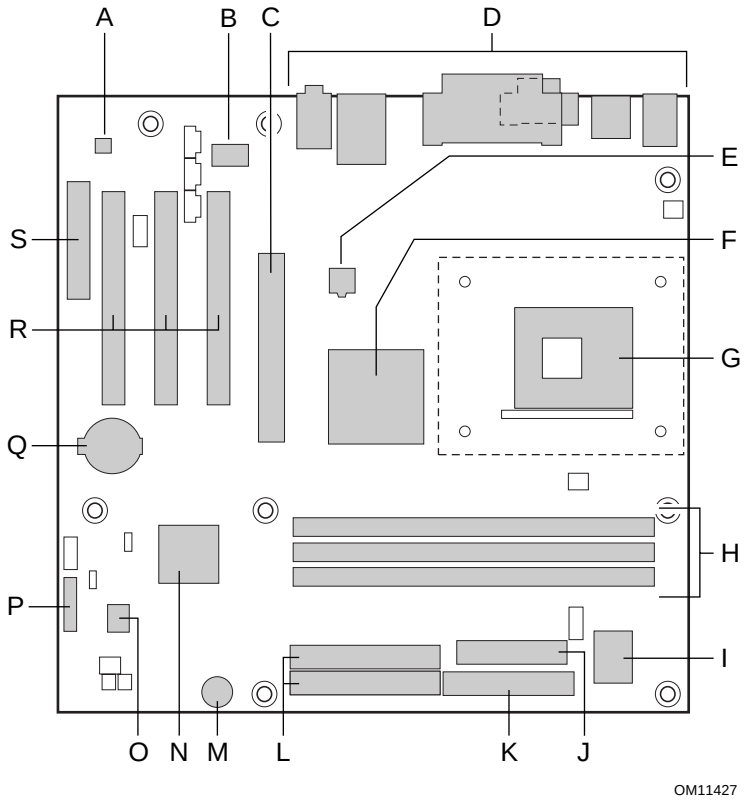
For information about	Refer to
Available configurations of the D845HV and D845WN boards	Section 1.3, page 17

NOTE

The LAN and the CNR manufacturing options are mutually exclusive.

1.2.3 Board Layouts

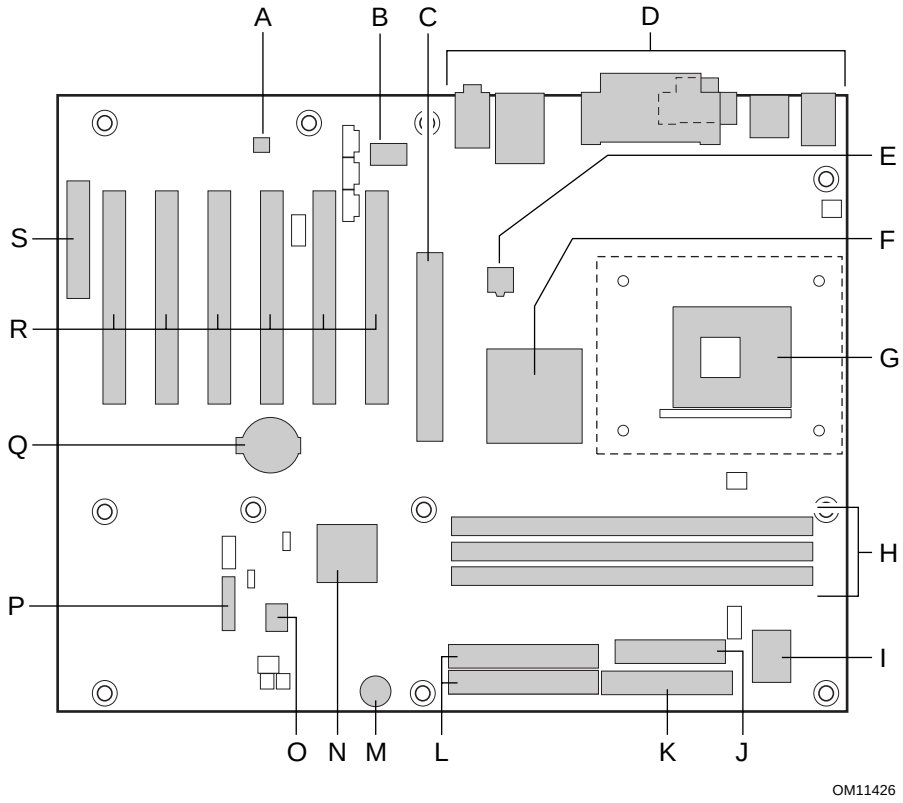
Figure 1 shows the location of the major components on the D845HV board.



A	Audio codec (optional)	K	Diskette drive connector
B	Intel 82562ET PLC Device (optional)	L	IDE connectors
C	AGP connector	M	Speaker (optional)
D	Back panel connectors	N	Intel 82801BA I/O Controller Hub (ICH2)
E	+12V power connector (ATX12V)	O	Intel 82802AB 4 Mbit Firmware Hub (FWH)
F	Intel 82845 Memory Controller Hub (MCH)	P	Front panel connector
G	mPGA478 processor socket	Q	Battery
H	DIMM sockets	R	PCI bus add-in card connectors
I	I/O Controller	S	CNR connector (optional)
J	Power Connector		

Figure 1. D845HV Board Components

Figure 2 shows the location of the major components on the D845WN board.



A	Audio codec (optional)	K	Diskette drive connector
B	Intel 82562ET PLC Device (optional)	L	IDE connectors
C	AGP connector	M	Speaker (optional)
D	Back panel connectors	N	Intel 82801BA I/O Controller Hub (ICH2)
E	+12V power connector (ATX12V)	O	Intel 82802AB 4 Mbit Firmware Hub (FWH)
F	Intel 82845 Memory Controller Hub (MCH)	P	Front panel connector
G	mPGA478 processor socket	Q	Battery
H	DIMM sockets	R	PCI bus add-in card connectors
I	I/O Controller	S	CNR connector (optional)
J	Power Connector		

Figure 2. D845WN Board Components

1.2.4 Block Diagram

Figure 3 is a block diagram of the major functional areas of the D845HV and D845WN boards.

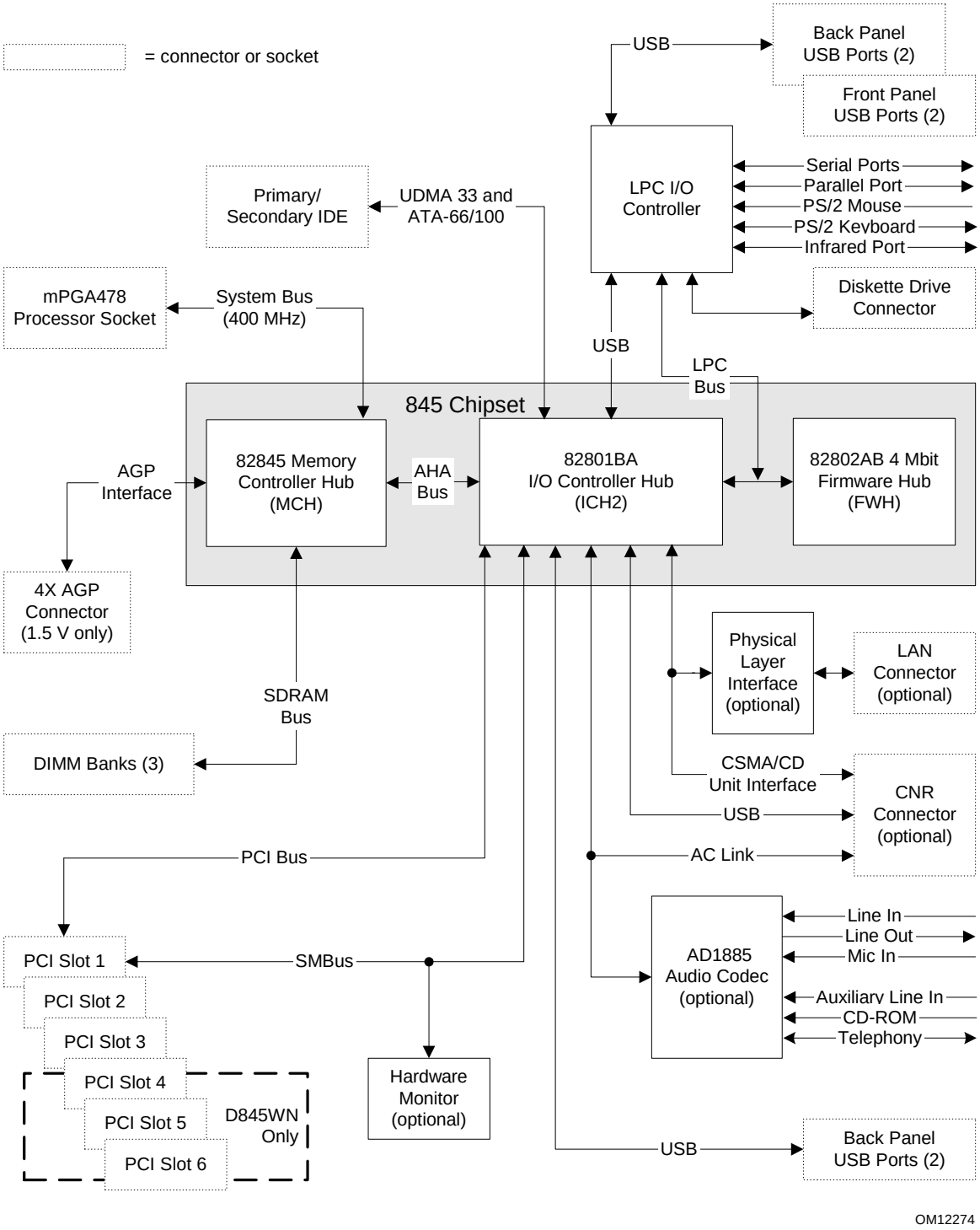


Figure 3. Block Diagram

1.3 Online Support

To find information about…	Visit this World Wide Web site:
Intel's D845HV and D845WN boards under "Product Info" or "Customer Support"	http://www.intel.com/design/motherbd http://support.intel.com/support/motherboards/desktop
Available configurations for the D845HV board	http://developer.intel.com/design/motherbd/hv/hv_available.htm
Available configurations for the D845WN board	http://developer.intel.com/design/motherbd/wn/wn_available.htm
Processor data sheets	http://www.intel.com/design/litcentr
Proper date access in systems with Intel® desktop boards	http://support.intel.com/support/year2000
ICH2 addressing	http://developer.intel.com/design/chipsets/datashts
Custom splash screens	http://intel.com/design/motherbd/gen_indx.htm
Audio software and utilities	http://www.intel.com/design/motherbd
LAN software and drivers	http://www.intel.com/design/motherbd

1.4 Operating System Support

The D845HV and D845WN boards support drivers for all of the onboard hardware and subsystems under the following operating systems:

- Microsoft Windows† 98SE
- Windows ME
- Windows NT† 4.0
- Windows† 2000
- Windows XP

For information about	Refer to
Supported drivers	Section 1.3

NOTE

Third party vendors may offer other drivers.

1.5 Design Specifications

Table 4 lists the specifications applicable to the D845HV and D845WN boards.

Table 4. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Revision 2.2, September 2000, Intel Corporation.	ftp://download.intel.com/ial/scalableplatforms/ac97r22.pdf
ACPI	*Advanced Configuration and Power Interface Specification*	Version 2.0, July 27, 2000, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, Phoenix Technologies Limited, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification*	Revision 2.0, May 4, 1998, Intel Corporation.	http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999, American Megatrends, Inc.	http://www.amij.com/amibios/bios.platforms.desktop.html
ATA/ ATAPI-5	*Information Technology-AT Attachment with Packet Interface - 5* (ATA/ATAPI-5)	Revision 3, February 29, 2000, Contact: T13 Chair, Seagate Technology.	http://www.t13.org
ATX	*ATX Specification*	Version 2.03, December 1998, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
ATX12V	*ATX / ATX12V Power Supply Design Guide*	Version 1.1, August 2000, Intel Corporation.	http://www.formfactors.org/developer/specs/atx/atxspecs.htm
CNR	*Communication and Network Riser (CNR) Specification*	Revision 1.1, October 18, 2000, Intel Corporation.	http://developer.intel.com/technology/cnr/index.htm

continued

Table 4. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
EPP	*IEEE Std 1284.1-1997* (Enhanced Parallel Port)	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Limited and International Business Machines Corporation.	http://www.phoenix.com/PlatSS/products/specs.html
IrDA	*IrDA Serial Physical Layer Specification*	Version 1.3, October 15, 1998, Infrared Data Association.	http://www.irda.org/standards/specifications.asp
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
MicroATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.formfactors.org/developer/specs/microatx/microatxspecs.htm
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corporation, Phoenix Technologies Limited, and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm
PXE	*Preboot Execution Environment*	Version 2.1, September 1999, Intel Corporation.	ftp://download.intel.com/ial/wfm/pxespec.pdf

continued

Table 4. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
SDRAM	*PC SDRAM Unbuffered DIMM Specification*	Revision 1.0, February 1998, Intel Corporation.	http://www.intel.com/technology/memory
	PC SDRAM Specification	Revision 1.7, November 1999, Intel Corporation.	http://www.intel.com/technology/memory
	PC Serial Presence Detect (SPD) Specification	Revision 1.2B, November 1999, Intel Corporation.	http://www.intel.com/technology/memory
SFX	*SFX/SFX12V Power Supply Design Guide*	Revision 2.0, May 2001, Intel Corporation.	http://www.formfactors.org/developer/specs/sfx/sfx12v.pdf
SMBIOS	*System Management BIOS*	Version 2.3.1, March 16, 1999, American Megatrends Incorporated, Award Software International Incorporated, Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://www.dmtf.org/download/standards/DSP0119.pdf
UHCI	*Universal Host Controller Interface Design Guide*	Revision 1.1, March 1996, Intel Corporation.	http://www.usb.org/developers
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC Corporation.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.6 Processor

CAUTION

Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop Board D845HV/D845WN Specification Update *for the most up-to-date list of supported processors for these boards.*

The D845HV and D845WN boards support a single Pentium 4 processor (in an mPGA478 socket) with a system bus of 400 MHz. The D845HV and D845WN boards support the processors listed in Table 5. All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

Table 5. Supported Processors

Type	Designation	System Bus	L2 Cache Size
Pentium 4 processor	1.4, 1.5, 1.6, 1.7, 1.8, 1.9, and 2.0 GHz	400 MHz	256 KB

NOTE

Use only ATX12V- or SFX12V-compliant power supplies with the D845HV and D845WN boards. ATX12V and SFX12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. Always connect the 20-pin and 4-pin leads of ATX12V and SFX12V power supplies to the corresponding connectors on the D845HV and D845WN boards, otherwise the board will not boot.

Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

For information about	Refer to
Processor support	Section 1.3, page 17
Processor usage	Section 1.3, page 17
Power supply connectors	Section 2.8.2.3, page 58

1.7 System Memory

⚠ CAUTION

Before installing or removing memory, make sure that AC power is disconnected by unplugging the power cord from the computer. Failure to do so could damage the memory and the board.

NOTE

Remove the AGP video card before installing or upgrading memory to avoid interference with the memory retention mechanism.

NOTE

The D845HV/D845WN boards have been designed to support DIMMs based on 512 Mbit technology for a maximum onboard capacity of up to 3 GB, but this technology has not been validated on this board. Please refer to the following Intel web sites for the latest lists of tested memory.
For the D845HV board:

http://developer.intel.com/design/motherbd/hv/hv_mem.htm

For the D845WN board:

http://developer.intel.com/design/motherbd/wn/wn_mem.htm

NOTE

To be fully compliant with all applicable Intel® SDRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.

The D845HV and D845WN boards both have three DIMM sockets and support the following memory features:

- 3.3 V (only) 168-pin SDRAM DIMMs with gold-plated contacts
- Unbuffered single-sided or double-sided DIMMs
- Maximum total system memory: 3 GB; minimum total system memory: 32 MB
- 133 MHz SDRAM DIMMs only
- Serial Presence Detect (SPD)
- Suspend to RAM
- Non-ECC and ECC DIMMs

NOTE

For ECC functionality, all installed DIMMs must be ECC. If both ECC and non-ECC DIMMs are used, ECC will not function.

For information about	Refer to
Obtaining the *PC Serial Presence Detect (SPD) Specification*	Section 1.5, page 18

Table 6 lists the supported DIMM configurations.

Table 6. Supported Memory Configurations

DIMM Capacity	Number of Sides	SDRAM Density	SDRAM Organization Front-side/Back-side	Number of SDRAM devices
32 MB	SS	64 Mbit	4 M x 16/empty	4
64 MB	DS	64 Mbit	4 M x 16/4 M x 16	8
64 MB	SS	64 Mbit	8 M x 8/empty	8
64 MB	SS	128 Mbit	8 M x 16/empty	4
96 MB	DS	64 Mbit	8 M x 8/4 M x 16	12 (Notes 1 and 2)
96 MB	DS	128/64 Mbit	8 M x 16/4 M x 16	8 (Notes 1 and 2)
128 MB	DS	64 Mbit	8 M x 8/8 M x 8	16 (Note 1)
128 MB	DS	128 Mbit	8 M x 16/8 M x 16	8 (Notes 1 and 2)
128 MB	SS	128 Mbit	16 M x 8/empty	8
128 MB	SS	256 Mbit	16 M x 16/empty	4
192 MB	DS	128 Mbit	16 M x 8/8 M x 16	12 (Notes 1 and 2)
192 MB	DS	128/64 Mbit	16 M x 8/8 M x 8	16 (Notes 1 and 2)
256 MB	DS	128 Mbit	16 M x 8/16 M x 8	16 (Notes 1 and 2)
256 MB	DS	256 Mbit	16 M x 16/16 M x 16	8 (Notes 1 and 2)
256 MB	SS	256 Mbit	32 M x 8/empty	8
512 MB	DS	256 Mbit	32 M x 8/32 M x 8	16 (Notes 1 and 2)

Notes:

1. If the number of SDRAM devices is greater than nine, the DIMM will be double sided.
2. Front side population/back side population indicated for SDRAM density and SDRAM organization.
3. In the second column, “DS” refers to double-sided memory modules (containing two rows of SDRAM) and “SS” refers to single-sided memory modules (containing one row of SDRAM).

NOTE

For D845HV boards with two DIMM sockets, the maximum total system memory is 2 GB.

1.8 Intel® 845 Chipset

The Intel 845 chipset consists of the following devices:

- Intel 82845 Memory Controller Hub (MCH) with Accelerated Hub Architecture (AHA) bus
- Intel 82801BA I/O Controller Hub (ICH2) with AHA bus
- Intel 82802AB Firmware Hub (FWH)

The MCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH2 is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS. The component combination provides the chipset interfaces as shown in Figure 4.

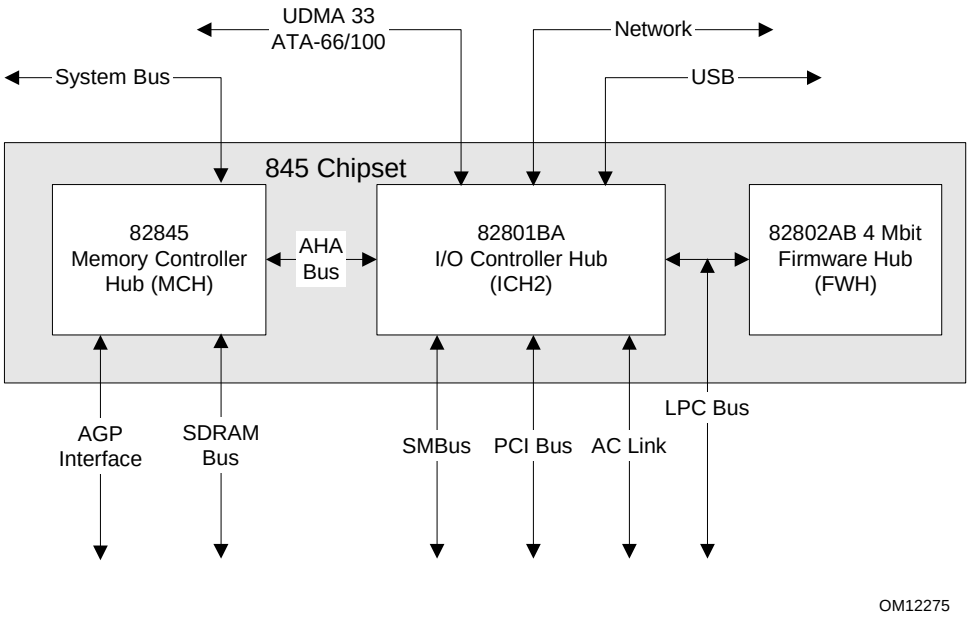


Figure 4. Intel 845 Chipset Block Diagram

For information about	Refer to
The Intel 845 chipset	http://developer.intel.com
Resources used by the chipset	Chapter 2

1.8.1 AGP

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

The AGP connector supports AGP add-in cards with 1.5 V Switching Voltage Level (SVL). Legacy 3.3 V AGP cards are not supported.

For information about	Refer to
The location of the AGP connector	Figure 1, page 14
The signal names of the AGP connector	Table 37, page 65

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.1, AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

For information about	Refer to
Obtaining the *Accelerated Graphics Port Interface Specification*	Section 1.5, page 18

1.8.2 USB

There are two USB configurations, depending on which I/O controller is used on the board, as follows:

- The USB configuration for boards with the SMSC LPC47M142 I/O controller is described in Section 1.8.2.1
- The USB configuration for boards with the SMSC LPC47M132 I/O controller is described in Section 1.8.2.2

The D845HV and D845WN boards fully support UHCI and use UHCI-compatible software drivers.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

1.8.2.1 USB Configuration for Boards with the SMSC LPC47M142 I/O Controller

The D845HV/D845WN boards support up to seven USB ports, as shown in Figure 5. The ICH2 provides three external ports: two ports are implemented with stacked back panel connectors and the other port is accessible through a CNR add-in card. The SMSC LPC47M142 I/O controller provides four external ports: two ports implemented with stacked back panel connectors and two ports routed to the front panel USB connector.

For more than seven USB devices, an external hub can be connected to any of the ports.

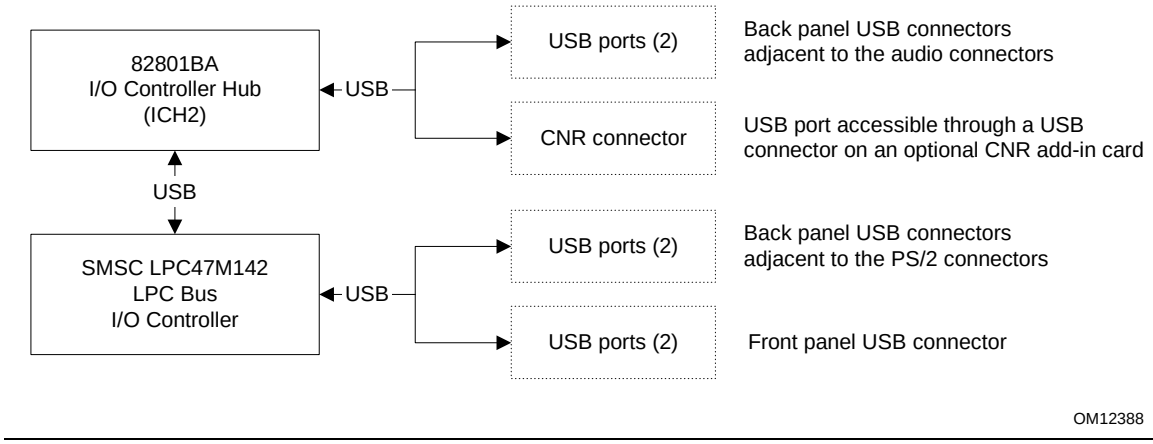


Figure 5. USB Port Configuration for Boards with the SMSC LPC47M142 I/O Controller

For information about	Refer to
The location of the USB connectors on the back panel	Figure 10, page 52
The signal names of the back panel USB connectors	Table 19, page 53
The location of the front panel USB connector	Figure 15, page 68
The signal names of the front panel USB connector	Table 43, page 69
The USB specification and UHCI	Section 1.5, page 18

1.8.2.2 USB Configuration for Boards with the SMSC LPC47M132 I/O Controller

D845HV boards equipped with the optional SMSC LPC47M132 I/O controller support up to four USB ports, as shown in Figure 6. The ICH2 provides four external ports: two ports are implemented with stacked back panel connectors and two are accessible through the front panel USB connector.

For more than four USB devices, an external hub can be connected to any of the ports.

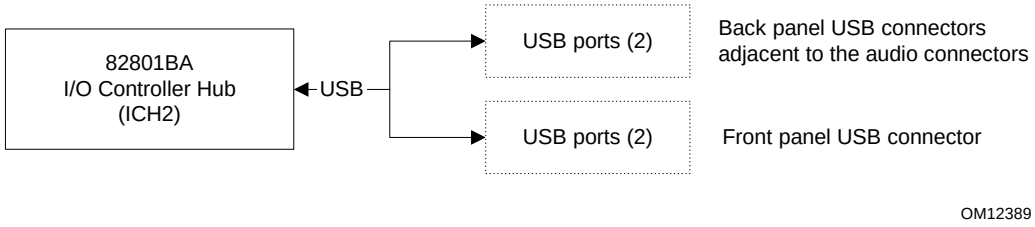


Figure 6. USB Port Configuration for Boards with the SMSC LPC47M132 I/O Controller

For information about	Refer to
The location of the USB connectors on the back panel	Figure 10, page 52
The signal names of the back panel USB connectors	Table 19, page 53
The location of the front panel USB connector	Figure 15, page 68
The signal names of the front panel USB connector	Table 43, page 69
The USB specification and UHCI	Section 1.5, page 18

1.8.3 IDE Support

1.8.3.1 IDE Interfaces

The ICH2's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): processor controls data transfer.
- 8237-style DMA: DMA offloads the processor, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to Ultra DMA and is device driver compatible.
- ATA-100: DMA protocol on IDE bus allows host and target throttling. The ICH2's ATA-100 logic can achieve read transfer rates up to 100 MB/sec and write transfer rates up to 88 MB/sec.

NOTE

ATA-66 and ATA-100 are faster timings and require a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Section 4.4.4.1 on page 105.

The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The D845HV and D845WN boards support Laser Servo (LS-120) diskette technology through the IDE interfaces. An LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 13, page 61
The signal names of the IDE connectors	Table 39, page 67
BIOS Setup program's Boot menu	Table 75, page 113

1.8.3.2 SCSI Hard Drive Activity LED Connector (Optional)

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows an add-in SCSI controller to use the same LED as the onboard IDE controller. For proper operation, this connector should be wired to the LED output of the add-in SCSI controller. The LED indicates when data is being read from, or written to, both the add-in SCSI controller and the IDE controller.

For information about	Refer to
The location of the SCSI hard drive activity LED connector	Figure 13, page 61, or Figure 14, page 62
The signal names of the SCSI hard drive activity LED connector	Table 40, page 67

1.8.4 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock provides a time-of-day clock and a multicentury calendar with alarm features. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTE

If the battery and AC power fail, custom defaults, if previously saved, will be loaded into CMOS RAM at power-on.

For information about	Refer to
Proper date access in systems with D845HV and D845WN boards	Section 1.3, page 17

1.8.5 Intel® 82802AB 4 Mbit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS program
- Logic that enables protection for storing and updating of platform information

1.9 I/O Controller

The SMSC LPC47M142 I/O controller provides the following features:

- Two serial ports
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB or 1.44 MB diskette drive
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support
- Two fan tachometer inputs
- Integrated USB hub
- IrDA compliant infrared port

The BIOS Setup program provides configuration options for the I/O controller.

NOTE

For the D845HV board only, there is a manufacturing option for an SMSC LPC47M132 I/O controller. This optional I/O controller provides identical functionality to the standard I/O controller, minus the integrated USB hub.

For information about	Refer to
SMSC LPC47M142 I/O controller	http://www.smsc.com

1.9.1 Serial Ports

The D845HV and D845WN boards have two serial port connectors. Serial port A is located on the back panel. Serial port B is accessible using a connector located near the main power connector. The serial ports' NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial ports can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

NOTE

The operation of serial port B and the infrared port are mutually exclusive. When serial port B is enabled in the BIOS Setup program, the IR option is disabled.

NOTE

For the D845HV board only, there is a manufacturing option that omits the connector for Serial port B.

For information about	Refer to
The location of the serial port A connector	Figure 10, page 52
The signal names of the serial port A connector	Table 21, page 54
The location of the serial port B connector	Figure 15, page 68
The signal names of the serial port B connector	Table 42, page 69

1.9.2 Infrared Support

On the front panel connector, there are four pins that support devices compliant with the *IrDA Serial Infrared Physical Layer Specification*, version 1.3. In the BIOS Setup program, infrared support is disabled by default. The IR connection can be used to transfer files to or from portable devices like laptops, PDAs, and printers. The Infrared Data Association (IrDA) specification supports data transfers of up to 115.2 kbits/sec at a distance of 1 meter.

NOTE

The infrared port operates in half duplex mode only.

NOTE

The operation of the infrared port and serial port B are mutually exclusive. When the IR option is enabled in the BIOS Setup program, serial port B is disabled.

For information about	Refer to
The location of the front panel connector	Figure 15, page 68
The signal names of the infrared port on the front panel connector	Table 45, page 70
The IrDA specification	Section 1.5, page 18

1.9.3 Parallel Port

The 25-pin D-Sub parallel port connector is located on the back panel. In the BIOS Setup program, the parallel port can be set to the following modes:

- Output only (PC AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 10, page 52
The signal names of the parallel port connector	Table 20, page 53
Setting the parallel port's mode	Table 66, page 102

1.9.4 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

For information about	Refer to
The location of the diskette drive connector	Figure 13, page 61
The signal names of the diskette drive connector	Table 38, page 66
The supported diskette drive capacities and sizes	Table 69, page 107

1.9.5 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 10, page 52
The signal names of the keyboard and mouse connectors	Table 18, page 53

1.9.6 I/O Controller Option

For the D845HV board only, there is a manufacturing option for an SMSC LPC47M132 I/O controller. This optional I/O controller provides identical functionality to the standard I/O controller, minus the integrated USB hub.

1.10 Audio Subsystem (Optional)

The optional audio subsystem includes these features:

- Split digital/analog architecture for improved S/N (signal-to-noise) ratio: ≥ 85 dB
- Power management support for ACPI 1.0 (driver dependant)
- 3-D stereo enhancement
- Mic in pre-amp that supports dynamic, condenser, and electret microphones

The audio subsystem supports the following audio interfaces:

- ATAPI-style connectors:
  - Telephony
  - Auxiliary line in
  - CD-ROM
- Front panel audio connector, including pins for:
  - Line out
  - Mic in
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in

The audio subsystem consists of the following devices:

- Intel 82801BA I/O Controller Hub (ICH2)
- Analog Devices AD1885 audio codec

Figure 7 is a block diagram of the audio subsystem.

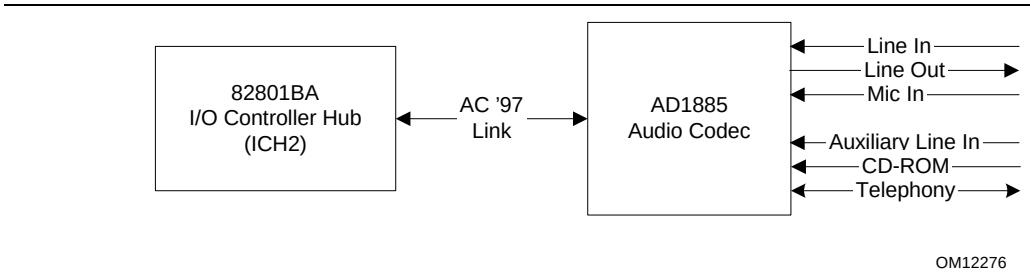


Figure 7. Audio Subsystem Block Diagram

For information about	Refer to
Upgrading the onboard audio subsystem using a CNR audio card	Section 1.12, page 35
The front panel audio connector	Section 2.8.3, page 68
The back panel audio connectors	Section 2.8.1, page 52

1.10.1 Audio Connectors

1.10.1.1 Front Panel Audio Connector

A 2 x 5-pin connector provides Mic in and line out signals for front panel audio connectors.

For information about	Refer to
The location of the connector	Section 2.8.3, page 68
The signal names of the front panel audio connector	Table 41, page 69

NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 72 for more information.

1.10.1.2 Telephony Connector

A 1 x 4-pin ATAPI-style connector connects the monaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modems, and answering machines.

For information about	Refer to
The location of the telephony connector	Figure 11, page 56
The signal names of the telephony connector	Table 26, page 57

1.10.1.3 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 11, page 56
The signal names of the auxiliary line in connector	Table 27, page 57

1.10.1.4 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 11, page 56
The signal names of the ATAPI CD-ROM connector	Table 28, page 57

1.10.2 Audio Subsystem Software

Audio software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining audio software and drivers	Section 1.3, page 17

1.11 LAN Subsystem (Optional)

The Network Interface Controller subsystem consists of the ICH2 (with integrated LAN Media Access Controller) and a physical layer interface device. Features of the LAN subsystem include:

- PCI Bus Master interface
- CSMA/CD Protocol Engine
- Serial CSMA/CD unit interface that supports the 82562ET (10/100 Mbit/sec Ethernet) on the CNR bus
- PCI Power Management
  - Supports ACPI technology
  - Supports LAN wake capabilities

1.11.1 Intel® 82562ET Platform LAN Connect Device

The Intel 82562ET component provides an interface to the back panel RJ-45 connector with integrated LEDs. This physical interface may alternately be provided through the CNR connector.

The Intel 82562ET provides the following functions:

- Basic 10/100 Ethernet LAN connectivity
- Supports RJ-45 connector with status indicator LEDs on the back panel
- Full device driver compatibility
- ACPI support
- Programmable transit threshold
- Configuration EEPROM that contains the MAC address

1.11.2 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec data rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11.3 LAN Subsystem Software

LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.3, page 17

1.12 CNR (Optional)

The CNR connector provides an interface that supports the audio, modem, USB, and LAN interfaces of the Intel 845 chipset. Figure 8 shows the signal interface between the riser and the ICH2.

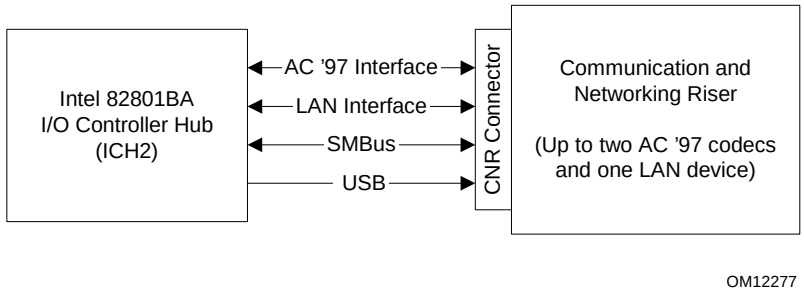


Figure 8. ICH2 and CNR Signal Interface

The interfaces supported by the CNR include the following:

- AC '97 interface: supports audio and/or modem functions on the CNR board.
- LAN interfaces: an eight-pin interface for use with Platform LAN Connection (PLC) based devices.
- SMBus interface: provides Plug-and-Play functionality for the CNR board.
- USB interface: provides a USB interface for the CNR board.

The CNR connector includes power signals required for power management and for CNR board operation. To learn more about the CNR, refer to the CNR specification.

The onboard two-channel audio subsystem can be upgraded to four- or six-channel audio using a CNR audio upgrade card in a slave configuration. CNR audio upgrade cards are available in multiple configurations from several different vendors supporting analog or S/P-DIF digital connections. A list of vendors supplying CNR audio upgrade cards compatible with the D845HV/D845WN boards' onboard audio subsystem, as well as an installation guide for these cards with SoundMAX with SPX are available on the following web site:

http://developer.intel.com/technology/cnr/

NOTE

If you install a CNR card that cannot support a multichannel audio upgrade, the D845HV and D845WN boards' integrated audio codec will be disabled. This only applies to D845HV and D845WN boards that have both the onboard audio subsystem and a CNR.

NOTE

The brand and type of audio codec used on the CNR card must match that of the D845HV/D845WN boards' codec (Analog Devices AD1885).

For information about	Refer to
Obtaining the CNR specification	Section 1.5, page 18

1.13 Hardware Management Subsystem

The hardware management features enable the boards to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Fan monitoring
- Thermal and voltage monitoring
- Chassis intrusion detection

For information about	Refer to
The WfM specification	Section 1.5, page 18

1.13.1 Hardware Monitor Component (Optional)

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature
- Power supply monitoring (+5 V, +3.3 V, +1.5 V, 3.3 VSB, Vccp) to detect levels above or below acceptable values
- SMBus interface

1.13.2 Fan Monitoring

The SMSC LPC47M142 I/O controller provides two fan tachometer inputs. Monitoring can be implemented using third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.14.2.2, page 42
The location of the fan connectors	Figure 12, page 58
The signal names of the fan connectors	Section 2.8.2.2, page 56

1.13.3 Chassis Intrusion and Detection

The boards support a chassis security feature that detects if the chassis cover is removed. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion connector. The mechanical switch is closed for normal computer operation.

For information about	Refer to
The location of the chassis intrusion connector	Figure 12, page 58
The signal names of the chassis intrusion connector	Table 33, page 60

NOTE

Chassis intrusion detection may be implemented using third-party software.

1.14 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - LAN wake capabilities
  - Instantly Available PC technology
  - Resume on Ring
  - Wake from USB
  - Wake from PS/2 devices
  - Power Management Event (PME#) wake-up support

1.14.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the D845HV and D845WN boards requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 10 on page 40)
- Support for a front panel power and sleep mode switch.

Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

For information about	Refer to
The D845HV and D845WN boards' compliance level with ACPI	Section 1.5, page 18

1.14.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the D845HV and D845WN boards along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S1 – Processor stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 52.5 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

1.14.1.2 Wake-up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. Wake-up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S4, S5
RTC alarm	S1, S3, S4, S5
LAN	S1, S3, S4, S5 (Note 1)
CNR	S1, S3, S4 (Note 2), S5 (Note 2)
PME#	S1, S3, S4, S5
Modem (back panel Serial Port A)	S1, S3
USB	S1, S3
PS/2 devices	S1, S3

Notes:

1. For LAN and PME#, S5 is disabled by default in the BIOS Setup program. Setting this option to Power On will enable a wake-up event from LAN in the S5 state.
2. Except from the CNR's USB interface.

NOTE

The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.14.1.3 Plug and Play

In addition to power management, ACPI provides control information so that operating systems can facilitate Plug and Play. ACPI is used only to configure devices that do not use other hardware configuration standards. PCI devices for example, are not configured by ACPI.

1.14.2 Hardware Support

⚠ CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 79 for additional information.

The D845HV and D845WN boards provide several power management hardware features, including:

- Power connector
- Fan connectors
- LAN wake capabilities
- Instantly Available PC technology
- Resume on Ring
- Wake from USB
- Wake from PS/2 keyboard
- PME# wake-up support

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal).

NOTE

The use of Resume on Ring and Wake from USB technologies from an ACPI state requires an operating system that provides full ACPI support.

1.14.2.1 Power Connector

When used with an ATX12V- or SFX12V-compliant power supply that supports remote power on/off, the D845HV and D845WN boards can turn off the system power through software control. When the system BIOS receives the correct command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the After Power Failure feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 12, page 58
The signal names of the power connector	Table 32, page 60
The BIOS Setup program's Boot menu	Table 75, page 113
The ATX specification	Section 1.5, page 18

1.14.2.2 Fan Connectors

Table 11 summarizes the function/operation of the fan connectors.

Table 11. Fan Connector Function/Operation

Connector	Description
Processor fan	• +12 V DC connection for a processor fan or active fan heatsink. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Wired to a fan tachometer input of the SMSC LPC47M142 I/O controller.
Front chassis fan (optional)	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state.
Rear chassis fan	• +12 V DC connection for a system or chassis fan. • Fan is on in the S0 or S1 state. Fan is off when the system is off or in the S3, S4, or S5 state. • Wired to a fan tachometer input of the SMSC LPC47M142 I/O controller.

For information about	Refer to
The location of the fan connectors	Figure 12, page 58
The signal names of the fan connectors	Section 2.8.2.2, page 56

1.14.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply. Refer to Section 2.11.3 on page 79 for additional information.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the D845HV and D845WN boards support LAN wake capabilities with ACPI in the following ways:

- the PCI bus PME# signal for PCI 2.2 compliant LAN designs
- the onboard LAN subsystem
- a CNR-based LAN subsystem

1.14.2.4 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply. Refer to Section 2.11.3 on page 79 for additional information.

Instantly Available PC technology enables the D845HV and D845WN boards to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 10 on page 40 lists the devices and events that can wake the computer from the S3 state.

The D845HV and D845WN boards support the *PCI Bus Power Management Interface Specification*. For information on the versions of this specification, see Section 1.5. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available PC technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

The optional standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 9 shows the location of the optional standby power indicator LED.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

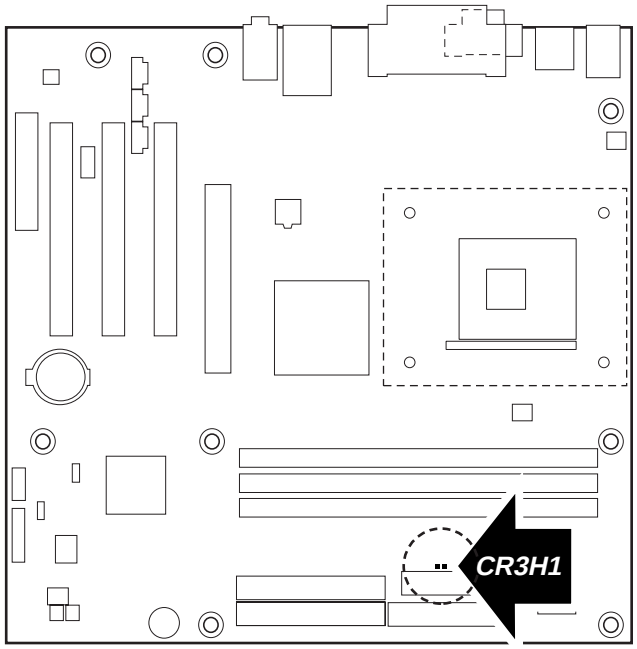


Figure 9. Location of the Optional Standby Power Indicator LED

1.14.2.5 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from ACPI S1 or S3 states
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.14.2.6 Wake from USB

USB bus activity wakes the computer from an ACPI S1 or S3 state.

NOTE

Wake from USB requires the use of a USB peripheral that supports Wake from USB.

1.14.2.7 Wake from PS/2 Devices

PS/2 device activity wakes the computer from an ACPI S1 or S3 state.

1.14.2.8 PME# Wake-up Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1, S3, S4, or S5 state (with BIOS support).

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 shows the I/O map, Table 14 lists the DMA channels, Table 15 defines the PCI configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 3145728 K	100000 - BFFFFFFF	3071 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 13. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD / STAT byte
0070 - 0071	2 bytes	System CMOS / Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	APM control
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
0228 - 022F*	8 bytes	LPT3
0278 - 027F*	8 bytes	LPT2
02E8 - 02EF*	8 bytes	COM4 / video (8514A)
02F8 - 02FF*	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0377, bits 6:0	7 bits	Secondary IDE channel status port
0378 - 037F	8 bytes	LPT1
03B0 - 03BB	12 bytes	Intel 82845 MCH
03C0 - 03DF	32 bytes	Intel 82845 MCH
03E8 - 03EF	8 bytes	COM3
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge / level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB**	4 bytes	PCI configuration address register
0CF9***	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers

continued

Table 13. I/O Map (continued)

Address (hex)	Description
96 contiguous bytes starting on a 128-byte divisible boundary	ICH2 (ACPI + TCO)
64 contiguous bytes starting on a 64-byte divisible boundary	D845HV/D845WN board resource
64 contiguous bytes starting on a 64-byte divisible boundary	Onboard audio controller
32 contiguous bytes starting on a 32-byte divisible boundary	ICH2 (USB controller #1)
16 contiguous bytes starting on a 16-byte divisible boundary	ICH2 (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary	Intel 82801BA PCI bridge
256 contiguous bytes starting on a 256-byte divisible boundary	ICH2 audio mixer
64 contiguous bytes starting on a 64-byte divisible boundary	ICH2 audio bus mixer
256 contiguous bytes starting on a 256-byte divisible boundary	ICH2 modem mixer
32 contiguous bytes starting on a 32-byte divisible boundary	ICH2 (USB controller #2)
96 contiguous bytes starting on a 128-byte divisible boundary	LPC47M142

* Default, but can be changed to another address range.

** Dword access only.

*** Byte access only.

NOTE

Some additional I/O addresses are not available due to ICH2 address aliassing.

For information about	Refer to
ICH2 addressing	Section 1.3 on page 17

2.4 DMA Channels

Table 14. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8 or 16 bits	Open
1	8 or 16 bits	Parallel port
2	8 or 16 bits	Diskette drive
3	8 or 16-bits	Parallel port (for ECP or EPP)
4	8 or 16 bits	DMA controller
5	16 bits	Open
6	16 bits	Open
7	16 bits	Open

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82845 component
00	01	00	PCI to AGP bridge
00	1E	00	Hub link to PCI bridge
00	1F	00	Intel 82801BA ICH2 PCI to LPC bridge
00	1F	01	IDE controller
00	1F	02	USB
00	1F	03	SMBus controller
00	1F	04	USB
00	1F	05	AC '97 audio controller (optional)
00	1F	06	AC '97 modem controller (optional)
01	00	00	Add-in AGP adapter card
02	08	00	LAN controller (optional)
02	09	00	PCI bus connector 1
02	0A	00	PCI bus connector 2
02	0B	00	PCI bus connector 3
02	0C	00	PCI bus connector 4 (Note)
02	0D	00	PCI bus connector 5 (Note)
02	0E	00	PCI bus connector 6 (Note)

Note: D845WN board only.

2.6 Interrupts

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note)
4	COM1 (Note)
5	LPT2 (Plug and Play option) / Audio / User available
6	Diskette drive
7	LPT1 (Note)
8	Real-time clock
9	Reserved for ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

Note: Default, but can be changed to another IRQ.

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D845HV and D845WN boards and therefore share the same interrupt. Table 17 shows an example of how the PIRQ signals are routed on the D845HV and D845WN boards.

For example, using Table 17 as a reference, assume an add-in card using INTB is plugged into PCI bus connector 3. In PCI bus connector 3, INTB is connected to PIRQB, which is already connected to the SMBus. The add-in card in PCI bus connector 3 now shares interrupts with these onboard interrupt sources.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH2 PIRQ Signal Name				
	PIRQF	**PIRQG**	**PIRQH**	**PIRQB**	**Other**
AGP connector				INTB	INTA to PIRQA
ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
ICH2 USB controller					INTC to PIRQH
ICH2 Audio / Modem				INTB	
ICH2 LAN					INTA to PIRQE
PCI Bus Connector 1	INTA	INTB	INTC	INTD	
PCI Bus Connector 2	INTD	INTA	INTB	INTC	
PCI Bus Connector 3	INTC	INTD	INTA	INTB	
PCI Bus Connector 4 (Note)	INTB	INTC	INTD	INTA	
PCI Bus Connector 5 (Note)	INTA	INTB	INTC	INTD	
PCI Bus Connector 6 (Note)	INTB	INTC	INTD	INTA	

Note: D845WN board only.

NOTE

The ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

⚠ CAUTION

Only the back panel, the front panel audio, and the front panel USB connectors of the D845HV and D845WN boards have overcurrent protection. The D845HV and D845WN boards' internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into the following groups:

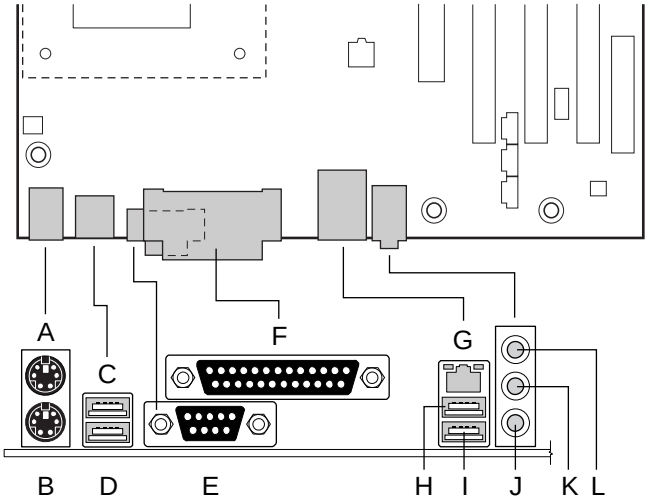
- Back panel I/O connectors (see page 52)
  - PS/2 keyboard and mouse
  - USB
  - Parallel port
  - Serial port A
  - LAN
  - Audio (Line out, Line in, and Mic in)
- Internal I/O connectors (see page 55)
  - Audio (telephony, auxiliary line input, and ATAPI CD-ROM)
  - Fans
  - Power
  - Add-in boards (CNR, PCI, and AGP)
  - IDE
  - Diskette drive
  - SCSI LED
- External I/O connectors (see page 68)
  - Front panel audio
  - Front panel USB
  - Serial port B
  - Auxiliary front panel power/sleep/message-waiting LED
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch, and auxiliary front panel power LED)

NOTE

When installing the board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, the IDE connector, and the DIMM sockets.

2.8.1 Back Panel Connectors

Figure 10 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations. The figure legend below lists the colors used.



Item	Description	Color	For more information see:
A	PS/2 mouse port	Green	Table 18
B	PS/2 keyboard port	Purple	Table 18
C	USB port (optional)	Black	Table 19
D	USB port (optional)	Black	Table 19
E	Serial port A	Teal	Table 21
F	Parallel port	Burgundy	Table 20
G	LAN (optional)	Black	Table 22
H	USB port	Black	Table 19
I	USB port	Black	Table 19
J	Mic in (optional)	Pink	Table 25
K	Audio line out (optional)	Lime green	Table 24
L	Audio line in (optional)	Light blue	Table 23

Figure 10. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

Table 18. PS/2 Mouse/Keyboard Connector

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	+5 V (Fused)
5	Clock
6	Not connected

Table 19. USB Connectors

Pin	Signal Name
1	+5 V (Fused)
2	USB#
3	USB
4	Ground

Table 20. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 – 25	Ground	Ground	Ground

Table 21. Serial Port A Connector

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 22. LAN Connector (optional)

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 23. Audio Line In Connector (Optional)

Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 24. Audio Line Out Connector (Optional)

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 25. Mic In Connector (Optional)

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

2.8.2 Internal I/O Connectors

The internal I/O connectors are divided into the following functional groups:

- Audio (see page 56)
  - Telephony
  - Auxiliary line in
  - ATAPI CD-ROM
- Power and hardware control (see page 58)
  - Fans
  - ATX12V
  - Main power
- Add-in boards and peripheral interfaces (see page 61)
  - CNR (communication and networking riser)
  - PCI bus (three on the D845HV board; six on the D845WN board)
  - AGP
  - IDE (two)
  - Diskette drive
  - SCSI LED

2.8.2.1 Expansion Slots

The board has the following expansion slots:

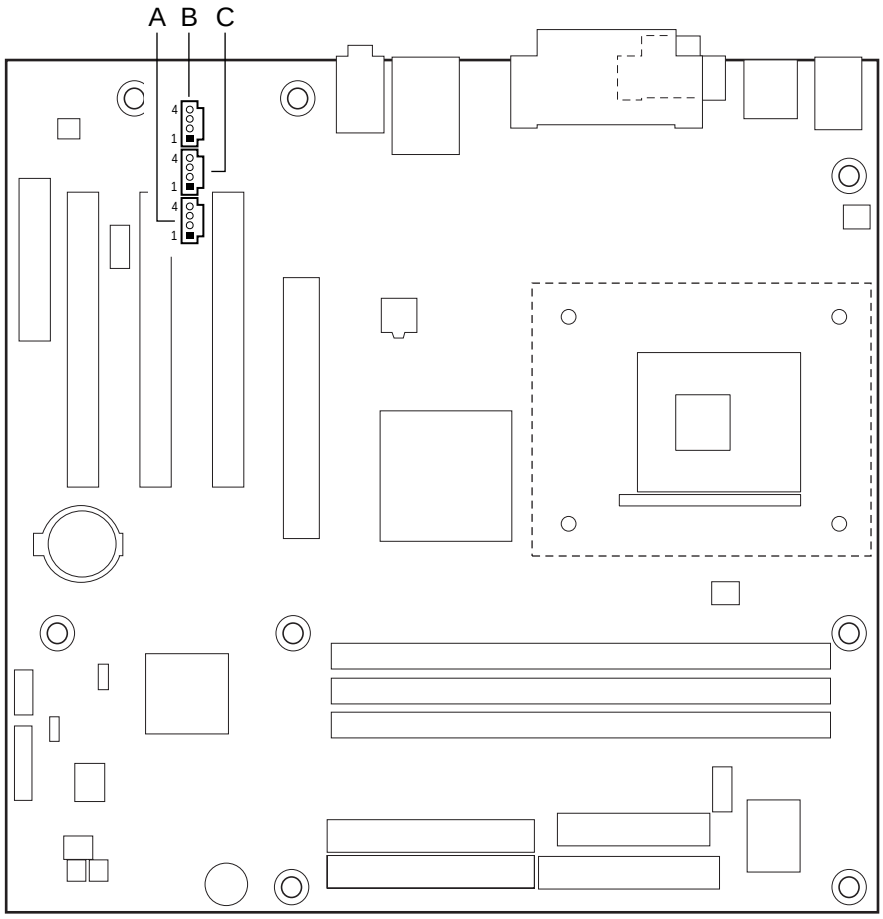
- One AGP connector. The AGP connector is keyed for 1.5 V AGP cards only. Do not install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.
- PCI rev 2.2 compliant local bus slots (three on the D845HV board, six on the D845WN board). The SMBus is routed to PCI bus connector 1 only (ATX expansion slot 6). PCI add-in cards with SMBus support can access sensor data and other information residing on the board.
- One CNR (optional), shared with PCI bus connector 3 (ATX expansion slot 1) on the D845HV board or with PCI bus connector 6 (ATX expansion slot 1) on the D845WN board.

NOTE

This document references back-panel slot numbering with respect to processor location on the board. The AGP slot is not numbered. PCI slots are identified as PCI slot #x, starting with the slot closest to the processor. The CNR slot shares an ATX expansion; slot 3 on the D845HV board and slot 6 on the D845WN. The ATX/MicroATX specifications identify expansion slot locations with respect to the far edge of a full-sized ATX chassis. The ATX specification and the board's silkscreen are opposite and could cause confusion. The ATX numbering convention is made without respect to slot type (PCI vs. AGP), but refers to an actual slot location on a chassis. Figure 13 on page 61 illustrates the board's PCI slot numbering.

2.8.2.2 Audio Connectors (Optional)

Figure 11 shows the location of the audio connectors.



Item	Description	Color	For more information see:
A	Telephony (optional)	Green	Table 26
B	Auxiliary line in, ATAPI style (optional)	White	Table 27
C	ATAPI CD-ROM (optional)	Black	Table 28

Figure 11. Audio Connectors

NOTE

The front panel audio connector is described in Section 2.8.3, beginning on page 68.

Table 26. Telephony Connector (Optional)

Pin	Signal Name
1	Audio_Mono_In
2	Ground
3	Ground
4	Audio_Mono_Out

Table 27. Auxiliary Line In Connector (Optional)

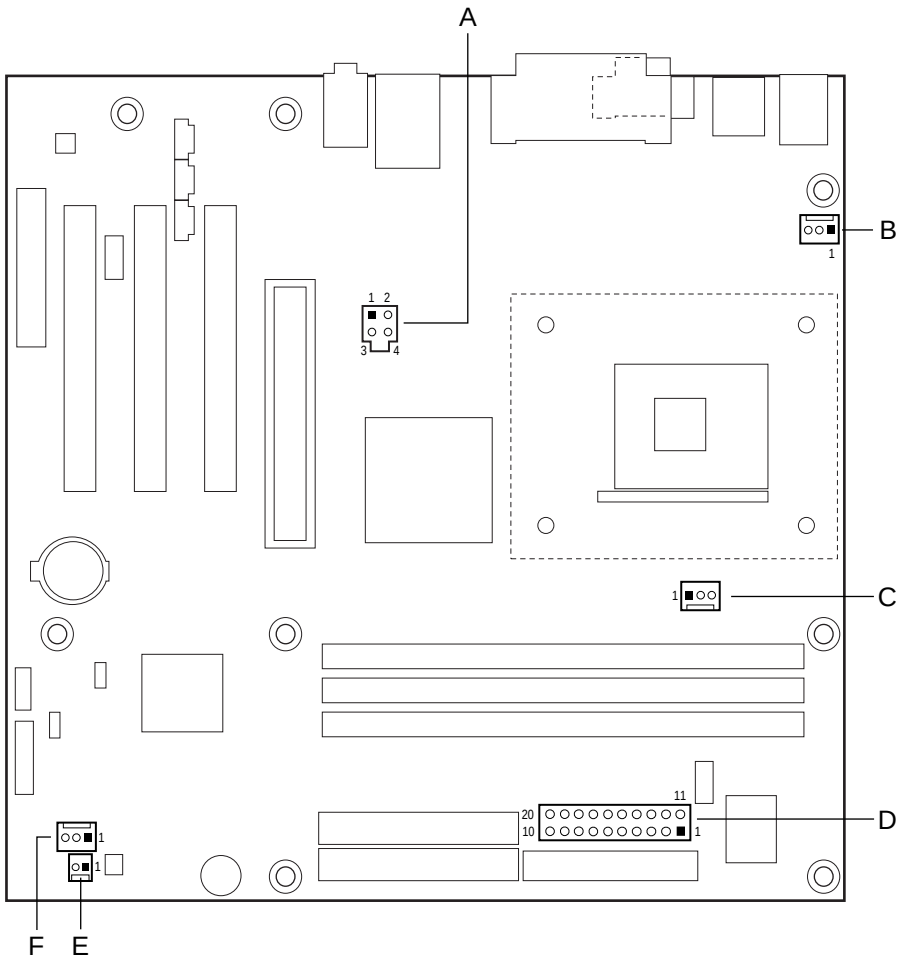
Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 28. ATAPI CD-ROM Connector (Optional)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

2.8.2.3 Power and Hardware Control Connectors

Figure 12 shows the location of the power and hardware control connectors.



Item	Description	For more information see:
A	ATX12V power	Table 29
B	Rear chassis fan	Table 30
C	Processor fan	Table 31
D	Main power	Table 32
E	Chassis intrusion	Table 33
F	Front chassis fan (optional)	Table 34

Figure 12. Power and Hardware Control Connectors

For information about	Refer to
The power connector	Section 1.14.2.1, page 41
The functions of the fan connectors	Section 1.14.2.2, page 42

NOTE

Use only ATX12V- or SFX12V-compliant power supplies with the D845HV and D845WN boards. ATX12V and SFX12V power supplies have an additional power lead that provides required supplemental power for the Intel Pentium 4 processor. Always connect the 20-pin and 4-pin leads of ATX12V and SFX12V power supplies to the corresponding connectors on the D845HV and D845WN boards, otherwise the board will not boot.

Do not use a standard ATX power supply. The board will not boot with a standard ATX power supply.

Table 29. ATX12V Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	3	+12 V
2	Ground	4	+12 V

NOTE

The board will not boot if the ATX12V power connector is not attached to the board.

Table 30. Rear Chassis Fan Connector

Pin	Signal Name
1	Ground
2	VREG_12V_POWER
3	REAR_FAN_TACH

Table 31. Processor Fan Connector

Pin	Signal Name
1	Ground
2	VREG_12V_POWER
3	FAN_TACH

Table 32. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (power supply remote on/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power Good)	18	No connect
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 33. Chassis Intrusion Connector

Pin	Signal Name
1	Intruder
2	Ground

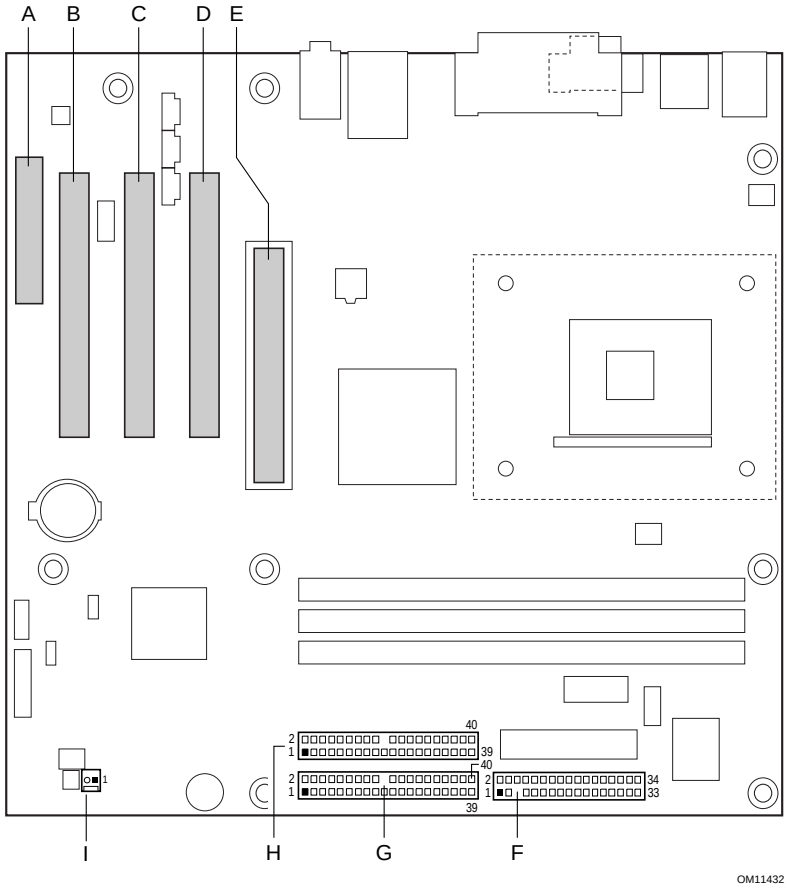
Table 34. Front Chassis Fan Connector (Optional)

Pin	Signal Name
1	Ground
2	+12 V
3	No connect

2.8.2.4 Add-in Board and Peripheral Interface Connectors

Figure 13 shows the location of the add-in board connector and peripheral connectors for the D845HV board. Note the following considerations for the PCI bus connectors (for both boards):

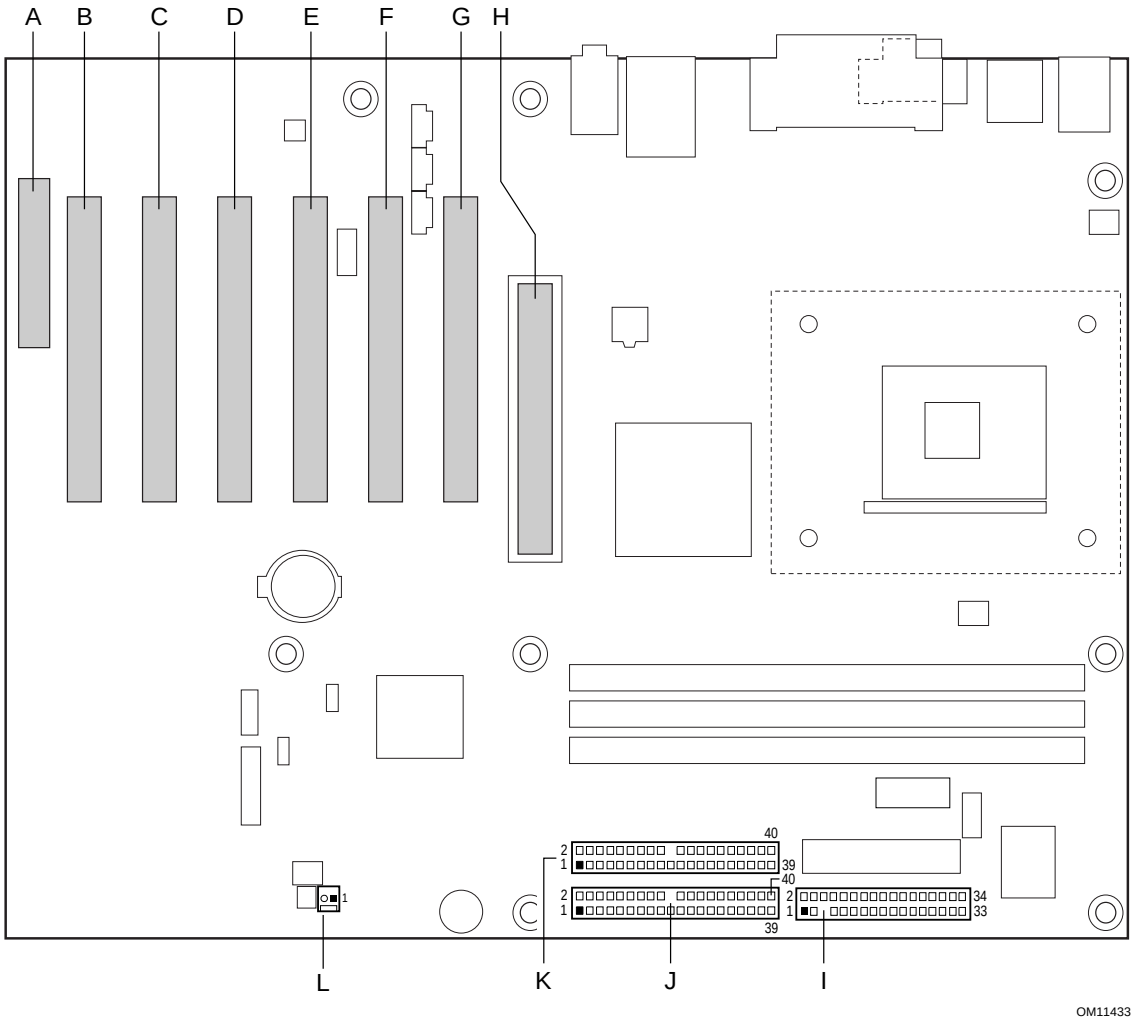
- All of the PCI bus connectors are bus master capable.
- PCI bus connector 1 has SMBus signals routed to it. This enables PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	For more information see:
A	Communication and networking riser (CNR)	Table 35
B	PCI bus connector 3	Table 36
C	PCI bus connector 2	Table 36
D	PCI bus connector 1	Table 36
E	AGP connector	Table 37
F	Diskette drive	Table 38
G	Primary IDE	Table 39
H	Secondary IDE	Table 39
I	SCSI LED (Optional)	Table 40

Figure 13. D845HV Add-in Board and Peripheral Interface Connectors

Figure 14 shows the location of the add-in board connector and peripheral connectors for the D845WN board.



Item	Description	For more information see:
A	Communication and networking riser (CNR)	Table 35
B	PCI bus connector 6	Table 36
C	PCI bus connector 5	Table 36
D	PCI bus connector 4	Table 36
E	PCI bus connector 3	Table 36
F	PCI bus connector 2	Table 36
G	PCI bus connector 1	Table 36
H	AGP connector	Table 37
I	Diskette drive	Table 38
J	Primary IDE	Table 39
K	Secondary IDE	Table 39
L	SCSI LED (Optional)	Table 40

Figure 14. D845WN Add-in Board and Peripheral Interface Connectors

Table 35. CNR Connector

Pin	Signal Name	Pin	Signal Name
A1	Reserved	B1	Reserved
A2	Reserved	B2	Reserved
A3	Ground	B3	Reserved
A4	Reserved	B4	Ground
A5	Reserved	B5	Reserved
A6	Ground	B6	Reserved
A7	LAN_TXD2	B7	Ground
A8	LAN_TXD0	B8	LAN_TXD1
A9	Ground	B9	LAN_RSTSYNC
A10	LAN_CLK	B10	Ground
A11	LAN_RXD1	B11	LAN_RXD2
A12	Reserved	B12	LAN_RXD0
A13	USB+	B13	Ground
A14	Ground	B14	Reserved
A15	USB-	B15	+5 V (dual)
A16	+12 V	B16	USB_OC
A17	Ground	B17	Ground
A18	+3.3 V (dual)	B18	-12 V
A19	+5 V	B19	+3.3 V
A20	Ground	B20	Ground
A21	EEDI	B21	EED0
A22	EECS	B22	EECK
A23	SMB_A1	B23	Ground
A24	SMB_A2	B24	SMB_A0
A25	SMB_SDA	B25	SMB_SCL
A26	AC97_RESET	B26	CDC_DWN_ENAB
A27	Reserved	B27	Ground
A28	AC97_SDATA_IN1	B28	AC97_SYNC
A29	AC97_SDATA_IN0	B29	AC97_SDATA_OUT
A30	Ground	B30	AC97_BITCLK

For information about	Refer to
The CNR	Section 1.12, page 35

Table 36. PCI Bus Connectors

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	Not connected (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	Not connected (PRSNT1#)*	A40	Reserved **	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved ***	B41	+3.3 V
A11	Reserved	B11	Not connected (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64#	B60	ACK64#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

** On PCI bus connector 1, this pin is connected to the SMBus clock line.

*** On PCI bus connector 1, this pin is connected to the SMBus data line.

Table 37. AGP Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12 V	B1	Not connected	A34	Vddq	B34	Vddq
A2	TYPEDET#	B2	+5 V	A35	AD22	B35	AD21
A3	Reserved	B3	+5 V	A36	AD20	B36	AD19
A4	Not connected	B4	Not connected	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vddq	B40	Vddq
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V (aux)
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	Not connected	A47	STOP#	B47	Vddq
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vddq	B52	Vddq
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Reserved	B22	Reserved	A55	Ground	B55	Ground
A23	Ground	B23	Ground	A56	AD9	B56	AD10
A24	Reserved	B24	+3.3 V (aux)	A57	C/BE0#	B57	AD8
A25	Vcc3.3	B25	Vcc3.3	A58	Vddq	B58	Vddq
A26	AD30	B26	AD31	A59	AD_STB0#	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vddq	B64	Vddq
A32	AD_STB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	VRREFG_C	B66	VREFC_G

NOTE

The AGP connector is keyed for 1.5 V AGP cards only. Do not attempt to install a legacy 3.3 V AGP card. The AGP connector is not mechanically compatible with legacy 3.3 V AGP cards.

Table 38. Diskette Drive Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	Not connected
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	Not connected
17	Not connected	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	Not connected	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

Table 39. PCI IDE Connectors

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select pull-up)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

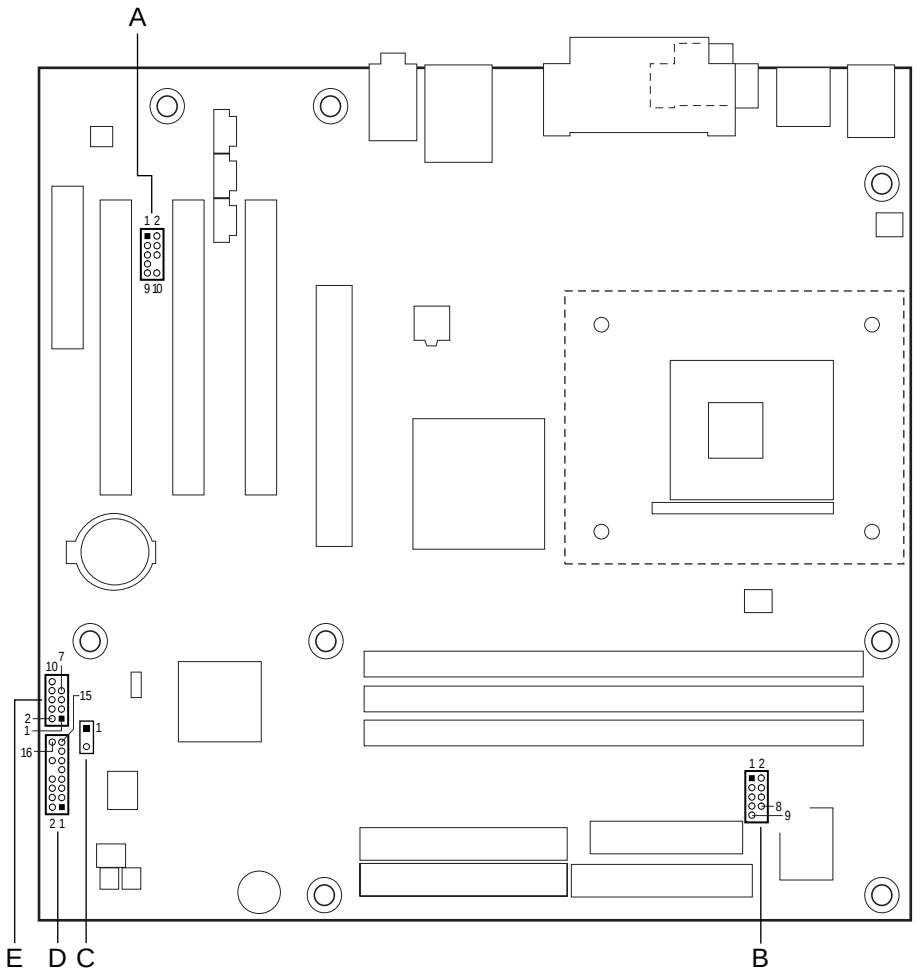
Signal names in brackets ([ ]) are for the secondary IDE connector.

Table 40. SCSI LED Connector (Optional)

Pin	Signal Name
1	SCSI_ACT#
2	No connect

2.8.3 External I/O Connectors

Figure 15 shows the locations of the external I/O connectors.



Item	Description	For more information see:
A	Front panel audio	Table 41
B	Serial Port B (optional)	Table 42
C	Auxiliary front panel power/sleep/message-waiting LED (optional)	Table 44
D	Front panel	Table 45
E	Front panel USB	Table 43

Figure 15. External I/O Connectors

Table 41. Front Panel Audio Connector

Pin	Signal Name	Pin	Signal Name
1	MIC_IN_FP	2	AUD_JACK_GND
3	MIC_BIAS	4	V_5P0_AUD_ANALOG
5	R_FNTOUT	6	R_RETIN
7	Not connected	8	Not connected
9	L_FNT_OUT	10	L_RETIN

⟹ NOTE

The front panel audio connector is alternately used as a jumper block for routing audio signals. Refer to Section 2.9.1 on page 72 for more information.

Table 42. Serial Port B Connector (Optional)

Pin	Signal Name	Pin	Signal Name
1	DCD (Data Carrier Detect)	2	RXD# (Receive Data)
3	TXD# (Transmit Data)	4	DTR (Data Terminal Ready)
5	Ground	6	DSR (Data Set Ready)
7	RTS (Request to Send)	8	CTS (Clear to Send)
9	RI (Ring Indicator)	10	Not connected

Table 43. Front Panel USB Connector

Pin	Signal Name	Pin	Signal Name
1	USB_FNT_PWR	2	USB_FNT_PWR
3	USB_FNTA#	4	USB_FNTB#
5	USB_FNTA	6	USB_FNTB
7	Ground	8	Ground
9	Not connected	10	Not connected

2.8.3.1 Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector (Optional)

Pins 1 and 3 of this connector duplicate the signals on pins 2 and 4 of the front panel connector.

Table 44. Auxiliary Front Panel Power/Sleep/Message-Waiting LED Connector

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	Not connected		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.8.3.2 Front Panel Connector

This section describes the functions of the front panel connector. Table 45 lists the signal names of the front panel connector.

Table 45. Front Panel Connector

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
Hard Drive Activity LED				**Power LED**			
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_ GRN	Out	Front panel green LED
3	HAD#	Out	Hard disk active LED	4	HDR_BLNK_ YEL	Out	Front panel yellow LED
Reset Switch				**On/Off Switch**			
5	Ground		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	Ground		Ground
Infrared Port				**Miscellaneous**			
9	+5 V	Out	Power	10	N/C		
11	IRRX	In	IrDA serial input	12	Ground		Ground
13	Ground		Ground	14	(pin removed)		Not connected
15	IRTX	Out	IrDA serial output	16	+5 V	Out	Power

2.8.3.2.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the optional SCSI hard drive activity LED connector.

For information about	Refer to
The SCSI hard drive activity LED connector	Section 1.8.3.2, page 28

2.8.3.2.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the D845HV/D845WN board resets and runs the POST.

2.8.3.2.3 Infrared Port Connector

Pins 9, 11, 13, and 15 can be connected to an IrDA module. After the IrDA interface is configured in the BIOS Setup program, files can be transferred to or from portable devices such as laptops, PDAs, and printers using application software.

NOTE

The infrared port operates in half duplex mode only.

NOTE

The operation of the infrared port and serial port B are mutually exclusive. When the IR option is enabled in the BIOS Setup program, serial port B is disabled.

2.8.3.2.4 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a one- or two-color LED. Table 46 shows the possible states for a one-color LED. Table 47 shows the possible states for a two-color LED.

Table 46. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 47. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.3.2.5 Power Switch Connector

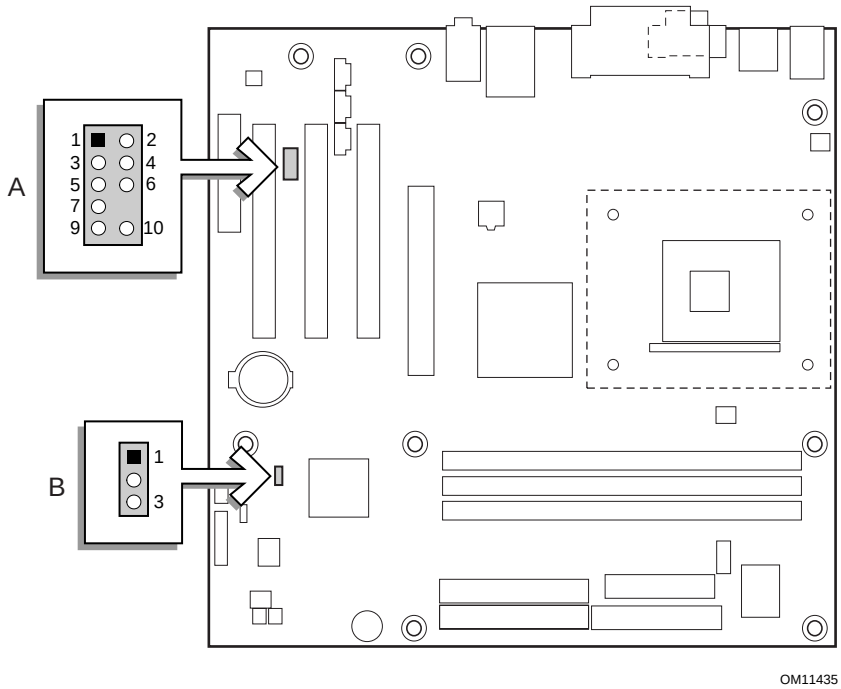
Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the D845HV/D845WN board.) At least two seconds must pass before the power supply will recognize another on/off signal.

2.9 Jumper Blocks

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 16 shows the location of the jumper blocks on the D845HV and D845WN boards.



Item	Description	Reference Designator
A	Front panel audio connector / jumper block	J8B4 (D845HV board) J7B2 (D845WN board)
B	BIOS Setup configuration jumper block	J9G1 (D845HV board) J7G1 (D845WN board)

Figure 16. Location of the Jumper Block

2.9.1 Front Panel Audio Connector/Jumper Block

This connector has two functions:

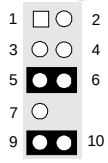
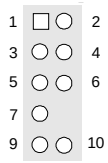
- With jumpers installed, the audio line out signals are routed to the back panel audio line out connector.
- With jumpers removed, the connector provides audio line out and mic in signals for front panel audio connectors.

Table 48 describes the two configurations of this connector/jumper block.

⚠ CAUTION

Do not place jumpers on this block in any configuration other than the one described in Table 48. Other jumper configurations are not supported and could damage the board.

Table 48. Front Panel Audio Connector / Jumper Block

Jumper Setting		Configuration
	5 and 6 9 and 10	Audio line out signals are routed to the back panel audio line out connector. The back panel audio line out connector is shown in Figure 10 on page 52.
	No jumpers installed	Audio line out and mic in signals are available for front panel audio connectors. Table 41 on page 69 lists the names of the signals available on this connector when no jumpers are installed.

NOTE

When the jumpers are removed and this connector is used for front panel audio, the back panel audio line out and mic in connectors are disabled.

2.9.2 BIOS Setup Configuration Jumper Block

The 3-pin jumper block determines the BIOS Setup program's mode. Table 49 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configuration mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

Table 49. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 95
The maintenance menu of the BIOS Setup program	Section 4.2, page 96
BIOS recovery	Section 3.7, page 91

2.10 Mechanical Considerations

2.10.1 D845HV Form Factor

The D845HV board is designed to fit into either a microATX or an ATX-form-factor chassis. Figure 17 illustrates the mechanical form factor for the D845HV board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 9.60 inches [243.84 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.4).

NOTE

When installing the board in a microATX chassis, make sure that peripheral devices are installed at least 1.5 inches above the main power connector, the diskette drive connector, and the IDE connector, and the DIMM sockets.

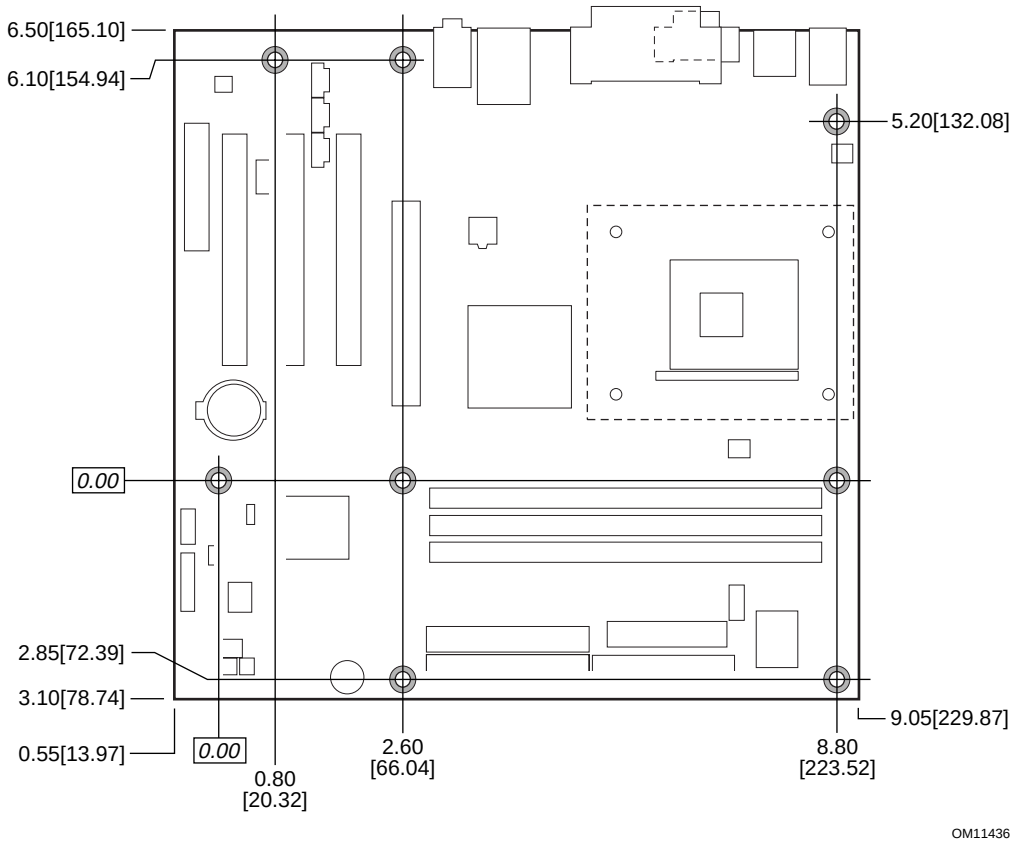


Figure 17. D845HV Board Dimensions

2.10.2 D845WN Form Factor

The D845WN board is designed to fit into an ATX-form-factor chassis. Figure 18 illustrates the mechanical form factor for the D845WN board. Dimensions are given in inches [millimeters]. The outer dimensions are 12.00 inches by 9.60 inches [304.48 millimeters by 243.84 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification (see Section 1.4).

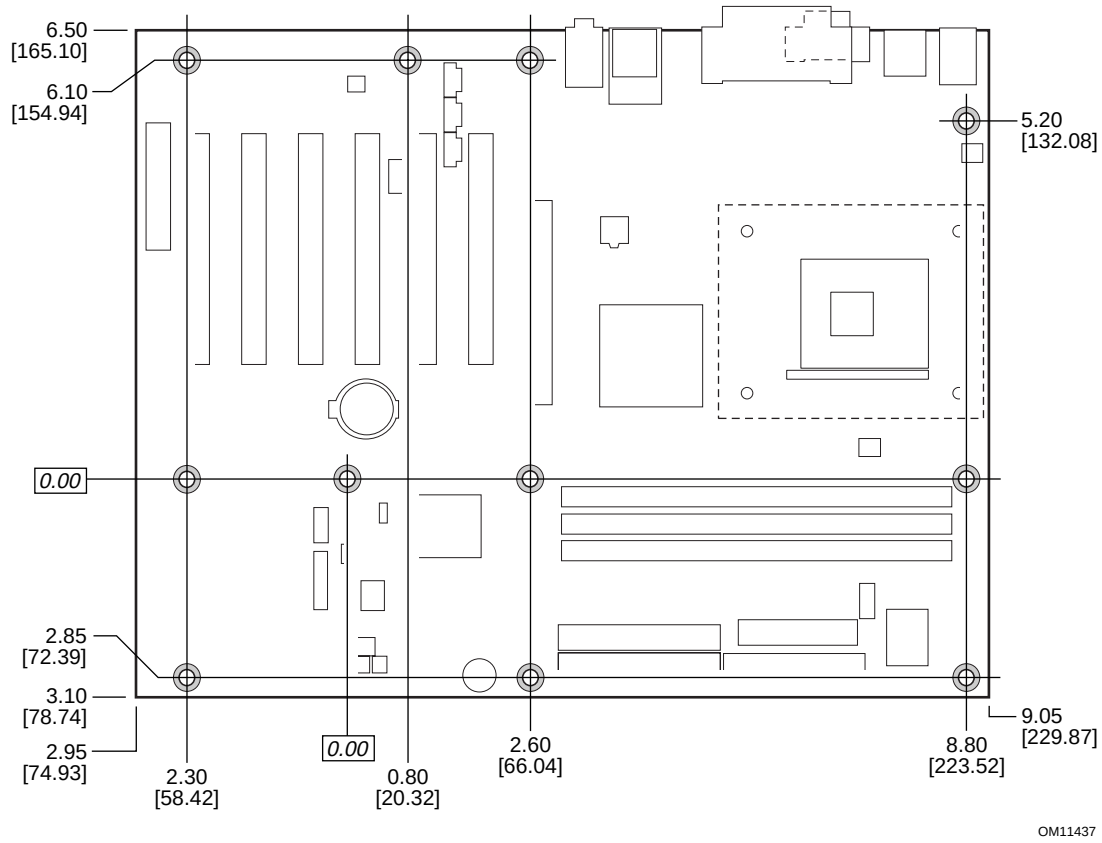


Figure 18. D845WN Board Dimensions

2.10.3 I/O Shield

The back panel I/O shield for D845HV and D845WN boards must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 19 shows the critical dimensions of the chassis-dependent I/O shield for boards with the onboard LAN subsystem. Figure 20 shows the critical dimensions of the I/O for boards without the onboard LAN subsystem. Dimensions are given in inches to a tolerance of ±0.02 inches.

The figure also indicates the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the ATX specification. See Section 1.4 for information about the ATX specification.

NOTE

The I/O shield drawings in this document are for reference only. An I/O shield compliant with the ATX chassis specification 2.01 is available from Intel.

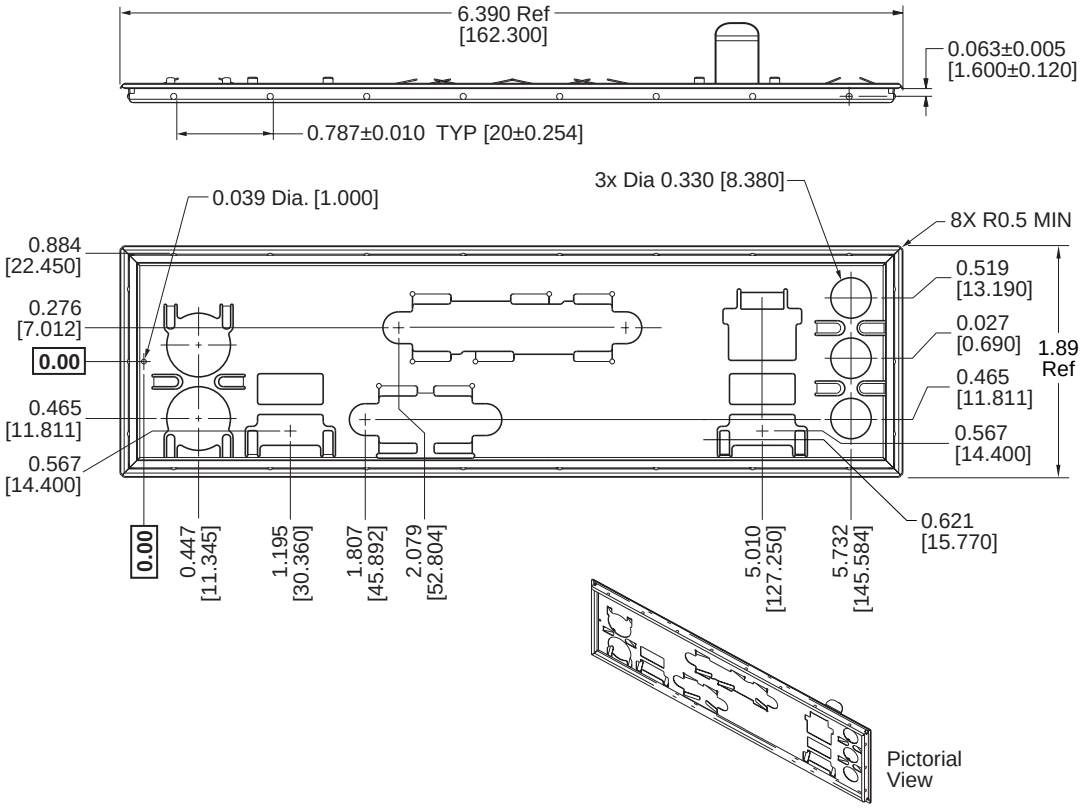


Figure 19. I/O Shield Dimensions (for boards with the LAN Subsystem)

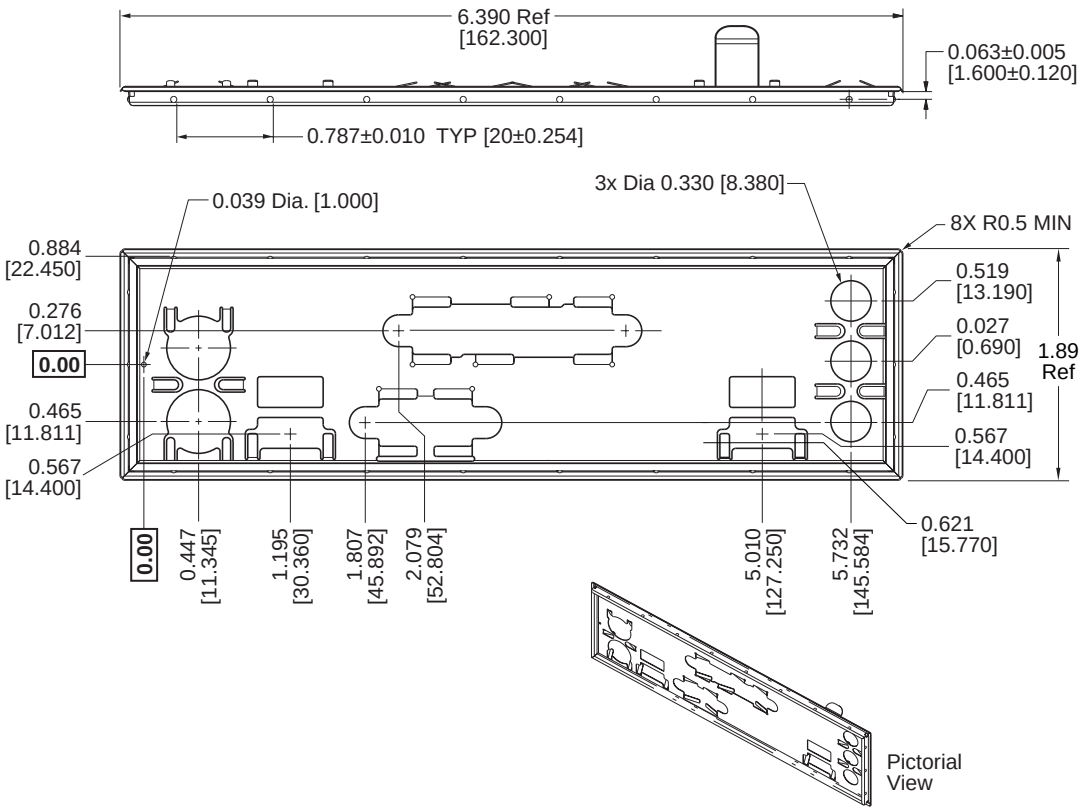


Figure 20. I/O Shield Dimensions (for boards without the LAN Subsystem)

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 50 lists voltage and current measurements for a computer that contains the D845HV/D845WN board and the following:

- 1.7 GHz Intel Pentium 4 processor with a 256 KB cache
- 256 MB SDRAM
- 3.5-inch diskette drive
- 20 GB IDE hard disk drive
- 32X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98SE desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with the computer is connected to a typical 250 W power supply, at nominal input voltage and frequency, with a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX / ATX12V Power Supply Design Guide, Version 1.1 (see Section 1.5 on page 18 for specification information).

Table 50. Power Usage

Mode	AC Power	DC Current at:				
		+3.3 V	+5 V	+12 V	-12 V	+5 VSB
ACPI S0	163 W	11.5 A	4.0 A	7.6 A	1.0 A	0.200 A
ACPI S1	26 W	4.7 A	0.008 A	0.750 A	0.038 A	0.164 A
ACPI S3	2 W	0.0 A	0.0 A	0.0 A	0.0 A	0.394 A

2.11.2 Add-in Board Considerations

The D845HV and D845WN boards are designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards is as follows:

- For a fully loaded D845HV board (all four expansion slots filled), the total +5 V current draw must not exceed 8 A.
- For a fully loaded D845WN board (all seven expansion slots filled), the total +5 V current draw must not exceed 14 A.

2.11.3 Standby Current Requirements

⚠ CAUTION

If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the D845HV and D845WN boards may lose register settings stored in memory, etc. Calculate the standby current requirements using the steps described below.

Power supplies used with the D845HV and D845WN boards must be able to provide enough standby current to support the Instantly Available PC (ACPI S3 sleep state) configuration as outlined in Table 51 below.

Values are determined by specifications such as PCI 2.2. Actual measured values may vary.

To estimate the amount of standby current required for a particular system configuration, standby current requirements of all installed components must be added to determine the total standby current requirement. Refer to the descriptions in Table 51 and review the following steps.

1. Note the total D845HV or D845WN board standby current requirement.
2. Add to that the total PS/2 port standby current requirement if a wake-enabled device is connected.
3. Add, from the PCI 2.2 slots (wake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
4. Add, from the PCI 2.2 slots (nonwake enabled) row, the total number of wake-enabled devices installed (PCI and AGP) and multiply by the standby current requirement.
5. Add all additional wake-enabled devices' and nonwake-enabled devices' standby current requirements as applicable.
6. Add all the required current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

Table 51. Standby Current Requirements

Instantly Available PC Current Support (Estimated for Integrated Board Components)	Description	Standby Current Requirements (mA)
	Total for D845HV board	394
Instantly Available PC Stand-by Current Support • **Estimated for add-on components** • **Add to Instantly Available PC total current requirement** **(See instructions above)**	PS/2 ports (Note)	345
	PCI 2.2 slots (wake enabled)	375
	PCI 2.2 slots (nonwake enabled)	20
	CNR (Note)	375
	USB ports (Note)	500

Note: Dependent upon system configuration

NOTE

IBM PS/2 Port Specification (Sept 1991) states:

- *275 mA for keyboard*
- *70 mA for the mouse (nonwake-enable device)*

PCI/AGP requirements are calculated by totaling the following:

- *One wake-enabled device @ 375 mA, plus*
- *Five nonwake-enabled devices @ 20 mA each, plus*

USB requirements are calculated as:

- *One wake-enabled device @ 500 mA*
- *USB hub @ 100 mA*
- *Three USB nonwake-enabled devices connected @ 2.5 mA each*

NOTE

Both USB ports are capable of providing up to 500 mA during normal G0/S0 operation. Only one USB port will support up to 500 mA of stand-by-current (wake-enabled device) during G1/S3 suspended operation. The other port may provide up to 7.5 mA (three nonwake-enabled devices.) during G1/S3 suspended operation.

2.11.4 Fan Connector Current Capability

Table 52 lists the current capability of the fan connectors on the D845HV and D845WN boards.

Table 52. Fan Connector Current Capability

Fan Connector	Maximum Available Current
Processor fan	1.20 A
Front chassis fan (optional)	0.50 A
Rear chassis fan	0.35 A

2.11.5 Power Supply Considerations

CAUTION

The +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 78 for additional information.

System integrators should refer to the power usage values listed in Table 50 when selecting a power supply for use with the D845HV or D845WN boards.

Measurements account only for current sourced by the D845HV or D845WN boards while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.5, page 18

2.12 Thermal Considerations

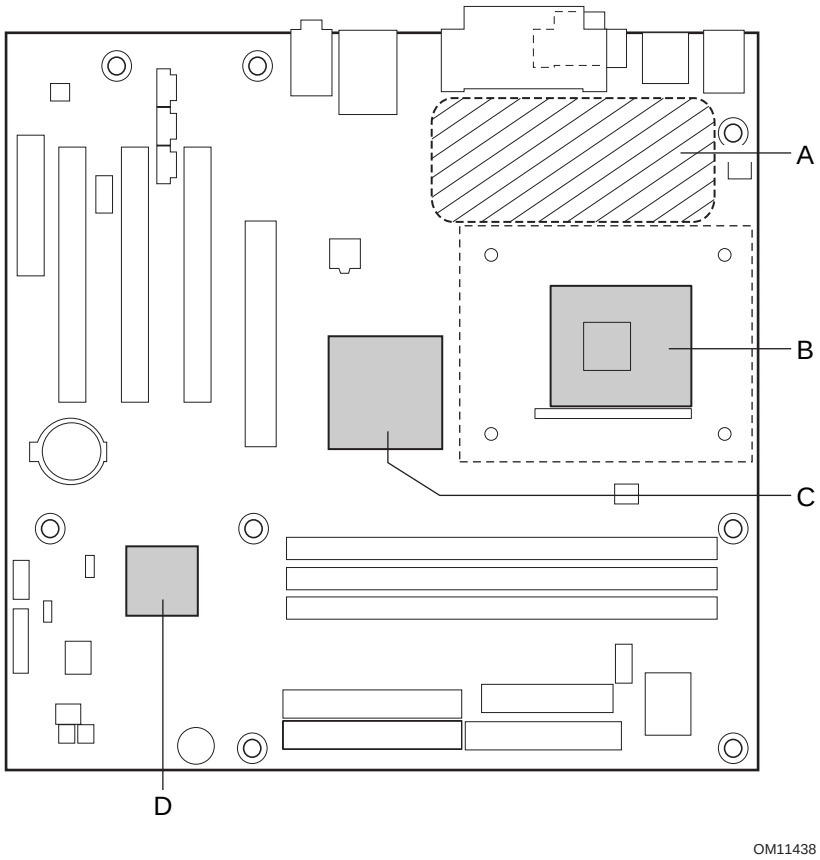
⚠ CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

⚠ CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (item A in Figure 21) can reach a temperature of up to 85 °C in an open chassis.

Figure 21 shows the locations of the localized high temperature zones.



A Processor voltage regulator area
B Processor
C Intel 82845 MCH
D Intel 82801BA ICH2

Figure 21. Localized High Temperature Zones

Table 53 provides maximum case temperatures for D845HV/D845WN board components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the D845HV/D845WN boards.

Table 53. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium 4 processor	For processor case temperature, see processor datasheets and processor specification updates
Intel 82845 MCH	83 °C (under bias)
Intel 82801BA ICH2	109 °C (under bias)

For information about	Refer to
Intel Pentium 4 processor datasheets and specification updates	Section 1.3, page 17

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 55 ºC. The MTBF calculations for the boards are as follows:

- D845HV board MTBF: 147370.4687 hours
- D845WN board MTBF: 126077.3308 hours

2.14 Environmental

Table 54 lists the environmental specifications for the D845HV and D845WN boards.

Table 54. D845HV/D845WN Board Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz: 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz: 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz: 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the D845HV and D845WN boards' compliance with U.S. and international safety and electromagnetic compatibility (EMC) regulations.

2.15.1 Safety Regulations

Table 55 lists the safety regulations the D845HV and D845WN boards comply with when correctly installed in a compatible host system.

Table 55. Safety Regulations

Regulation	Title
UL 1950/CSA C22.2 No. 950, 3rd edition	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)
IEC 60950, 2nd Edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 56 lists the EMC regulations the D845HV and D845WN boards comply with when correctly installed in a compatible host system.

Table 56. EMC Regulations

Regulation	Title
FCC (Class B)	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, Radiofrequency Devices. (USA)
ICES-003 (Class B)	Interference-Causing Equipment Standard, Digital Apparatus. (Canada)
EN55022: 1998 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (European Union)
EN55024: 1998	Information Technology Equipment – Immunity Characteristics Limits and methods of measurement. (European Union)
AS/NZS 3548 (Class B)	Australian Communications Authority, Standard for Electromagnetic Compatibility. (Australia and New Zealand)
CISPR 22, 3rd Edition (Class B)	Limits and methods of measurement of Radio Disturbance Characteristics of Information Technology Equipment. (International)
CISPR 24: 1997	Information Technology Equipment – Immunity Characteristics – Limits and Methods of Measurements. (International)

2.15.3 Product Certification Markings (Board Level)

The D845HV and D845WN boards have the following product certification markings:

- UL joint US/Canada Recognized Component mark: Consists of lower case c followed by a stylized backward UR and followed by a small US. Includes adjacent UL file number for Intel desktop boards: E210882 (component side).
- FCC Declaration of Conformity logo mark for Class B equipment; to include Intel name and D845HV and D845WN model designation (solder side).
- CE mark: Declaring compliance to European Union (EU) EMC directive (89/336/EEC) and Low Voltage directive (73/23/EEC) (component side). The CE mark should also be on the shipping container.
- Australian Communications Authority (ACA) C-Tick mark: consists of a stylized C overlaid with a check (tick) mark (component side), followed by Intel supplier code number, N-232. The C-tick mark should also be on the shipping container.
- Korean EMC certification logo mark: consists of MIC lettering within a stylized elliptical outline.
- Printed wiring board manufacturer's recognition mark: consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0) (solder side).
- PB part number: Intel bare circuit board part number (solder side). Also includes SKU number starting with AA followed by additional alphanumeric characters.
  - For the D845HV board, the PB number A63118-003.
  - For the D845WN board, the PB number is A64163-002.
- Battery "+ Side Up" marking: located on the component side of the board in close proximity to the battery holder.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The D845HV and D845WN boards use an Intel/AMI BIOS that is stored in the Firmware Hub (FWH) and can be updated using a disk-based program. The FWH contains the BIOS Setup program, POST, the PCI auto-configuration utility, and Plug and Play support.

The D845HV and D845WN boards support system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected system memory.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOSs are identified as HV84510A.86A.

When the D845HV or D845WN board's jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
The D845HV and D845WN boards' compliance level with Plug and Play	Section 1.5, page 18

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card. Autoconfiguration information is stored in ESCD format.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.4.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to ATA-66/100 and recognizes any ATAPI compliant devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.4 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use ATA-66/100 features the following items are required:

- An ATA-66/100 peripheral device
- An ATA-66/100 compatible cable
- ATA-66/100 operating system device drivers

NOTE

ATA-66/100 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an ATA-66/100 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is reduced to that of the slowest device.

NOTE

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The D845HV and D845WN boards' compliance level with SMBIOS	Section 1.4, page 17

3.5 Legacy USB Support

Legacy USB support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.

5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

Legacy USB support is for keyboards, mice, and hubs only. Other USB devices are not supported in legacy mode.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the upgrade utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 17

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program.

3.6.2 Custom Splash Screen

During POST, an Intel splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS upgrade utility. Information about this capability is available on the Intel Support World Wide Web site.

For information about	Refer to
The Intel World Wide Web site	Section 1.3, page 17

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Update Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

Even if the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Section 2.9, page 72
The Boot menu in the BIOS Setup program	Section 4.6.1, page 112
Contacting Intel customer support	Section 1.3, page 17

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the CD-ROM drive, the system will attempt to boot from the next defined drive.

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 1.5, page 18

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Using an optimized BIOS, such as the Intel® Rapid BIOS

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

3.9.2 Intel Rapid BIOS Boot

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot Menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enabled Intel Rapid BIOS Boot. This feature bypasses memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTE

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced Menu in the IDE Configuration Submenu of the BIOS Setup program).

For information about	Refer to
IDE Configuration Submenu in the BIOS Setup program	Section 4.4.4, page 104

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 57 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 57. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 110

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 58 lists the BIOS Setup program menu features.

Table 58. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and BIS credentials and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

For information about	Refer to
Boot Integrity Services (BIS)	Section 1.5, page 18

NOTE

In this chapter, all examples of the BIOS Setup program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 72 tells how to put the board in configuration mode.

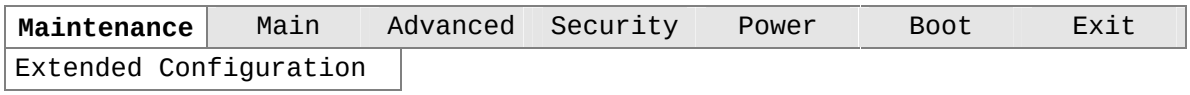
Table 59 lists the function keys available for menu screens.

Table 59. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.



The menu shown in Table 60 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 72 for configuration mode setting information.

Table 60. Maintenance Menu

Feature	Options	Description
Clear All Passwords	• **Yes (default)** • No	Clears the user and supervisor passwords.
Clear BIS Credentials	• **Yes (default)** • No	Clears the Wired for Management Boot Integrity Service (BIS) credentials.
Extended Configuration	• **Default (default)** • User-Defined	Invokes the Extended Configuration submenu.
CPU Information	No options	Displays CPU Information.
CPU Stepping Signature	No options	Displays CPU's Stepping Signature.
CPU Microcode Update Revision	No options	Displays CPU's Microcode Update Revision.

4.2.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar and then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 61 is for setting video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 61. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User Defined	User Defined allows setting memory control and video memory cache mode. If selected here, will also display in the Advanced Menu as: "Extended Menu: *Used*."
Video Memory Cache Mode	• USWC • **UC (default)**	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining. Selects UnCacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining.
SDRAM Auto-Configuration	• **Auto (default)** • User Defined	Sets extended memory configuration options to *Auto* or *User Defined*.
CAS# Latency	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.
SDRAM RAS# Active to Precharge	• 7 • 6 • **5** • **Auto (default)**	Corresponds to tRAS.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 62 describes the Main menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 62. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed.
System Bus Speed	No options	Displays the system bus speed.
Cache RAM	No options	Displays the size of second-level cache and whether it is ECC-capable.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 0 Memory Bank 1 Memory Bank 2	No options	Displays the amount and type of RAM in the memory banks.
Language	• **English (default)** • Español • Deutsch • Italiano • Français	Selects the current default language used by the BIOS.
Memory Configuration	• Non-ECC • **ECC (default)**	Allows the user to enable error reporting if the system and all installed memory support ECC. If non-ECC memory is installed, BIOS will detect and change the setting to Non-ECC.
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 63 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 63. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If *Used* is displayed, *User-Defined* has been selected in Extended Configuration under the Maintenance Menu.
PCI Configuration	Select to display submenu	Configures individual PCI slot's IRQ priority.
Boot Configuration	Select to display submenu	Configures Plug and Play and the Numlock key, and resets configuration data.
Peripheral Configuration	Select to display submenu	Configures peripheral ports and devices.
IDE Configuration	Select to display submenu	Specifies type of connected IDE devices.
Diskette Configuration	Select to display submenu	Configures the diskette drive.
Event Log Configuration	Select to display submenu	Configures Event Logging.
Video Configuration	Select to display submenu	Configures video features.

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar and then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu shown in Table 64 is used to configure the IRQ priority of PCI slots individually.

Table 64. PCI Configuration Submenu

Feature	Options	Description
PCI Slot1 IRQ Priority (Note 1)	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 1.
PCI Slot2 IRQ Priority (Note 1)	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 2.
PCI Slot3 IRQ Priority (Note 1)	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 3.
PCI Slot4 IRQ Priority (Note 1 and Note 2)	• **Auto (default)** • 9 • 10 • 11	Allows selection of IRQ priority for PCI bus connector 4.
PCI Slot5 IRQ Priority (Note 1 and Note 2)	No options	Displays the IRQ for PCI bus connector 5. This IRQ will be the same as the setting selected for PCI bus connector 1. (PCI bus connectors 1 and 5 share the same interrupt.)
PCI Slot6 IRQ Priority (Note 1 and Note 2)	No options	Displays the IRQ for PCI bus connector 6. This IRQ will be the same as the setting selected for PCI bus connector 4. (PCI bus connectors 4 and 6 share the same interrupt.)

Notes:

1. Additional interrupts may be available if certain onboard devices (such as the serial and parallel ports) are disabled.
2. This option appears only on the D845WN board.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 65 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 65. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Reset Config Data	• **No (default)** • Yes	*No* does not clear the PCI/PnP configuration data stored in flash memory on the next boot. *Yes* clears the PCI/PnP configuration data stored in flash memory on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar and then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 66 is used for configuring computer peripherals.

Table 66. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	• Disabled • Enabled • **Auto (default)**	Configures serial port A. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O address (This feature is present only when Serial Port A is set to *Enabled*)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for serial port A, if serial port A is Enabled.
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for serial port A, if serial port A is Enabled.
Serial Port B	• Disabled • Enabled • **Auto (default)**	Configures serial port B. *Auto* assigns the first free COM port, normally COM 2, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• **Normal (default)** • IrDA SIR-A • ASK_IR	Configures the second UART in the I/O controller to function as either a COM port wired to the serial port B connector (Normal option) or as an infrared port wired to the front panel connector (IrDA SIR-A or ASK_IR option).
Base I/O address (This feature is displayed only if Serial Port B is set to *Enabled*.)	• **2F8 (default)** • 3E8 • 2E8	Specifies the base I/O address for serial port B, if serial port B is set to *Enabled*.

continued

Table 66. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Interrupt (This feature is displayed only if Serial Port B is set to *Enabled*.)	• **IRQ 3 (default)** • IRQ 4	Specifies the interrupt for serial port B, if serial port B is set to *Enabled*.
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address (This feature is present only when Parallel Port is set to *Enabled*)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
DMA (This feature is present only when Parallel Port Mode is set to *ECP*)	• 1 • **3 (default)**	Specifies the DMA channel.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem. For boards with no onboard audio subsystem, this option does not appear; however, this option does appear if a CNR card with an audio subsystem is installed.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the onboard LAN device. For boards with no onboard LAN audio subsystem, this option will not appear; however, this option does appear if a CNR card with a LAN subsystem is installed.
Modem Device	• Disabled • **Enabled (default)**	Enables or disables a modem device on a CNR card. This option appears only when a CNR card with a modem is installed.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables Legacy USB support.

4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar and then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The menu represented in Table 67 is used to configure IDE device options.

Table 67. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
PCI IDE Bus Master	• Disabled • **Enabled (default)**	Enables/disables the use of DMA for hard drive BIOS INT13 reads and writes.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	Select to display sub-menu	Reports type of connected IDE device.
Primary IDE Slave	Select to display sub-menu	Reports type of connected IDE device.
Secondary IDE Master	Select to display sub-menu	Reports type of connected IDE device.
Secondary IDE Slave	Select to display sub-menu	Reports type of connected IDE device.

4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration, and then the master or slave to be configured.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**
Diskette Configuration
Event Log Configuration
Video Configuration

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 68 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 68. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows capabilities to be changed. *Auto* fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	No options	Displays the capacity of the drive.
Multi-Sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.

continued

Table 68. Primary/Secondary IDE Master/Slave Submenus (continued)

Feature	Options	Description
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Specifies the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4 • Mode 5	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for ATA-100 peripherals).

4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar and then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 69 is used for configuring the diskette drive.

Table 69. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½" (default)** • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write protection for the diskette drive.

4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar and then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 70 is used to configure the event logging features.

Table 70. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	[Enter]	Displays the event log.
Clear All Event Logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
ECC Event Logging	• Disabled • **Enabled (default)**	Enables logging of ECC events.
Mark Events As Read	• **Yes (default)** • No	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar and then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 71 is for configuring the video features.

Table 71. Video Configuration Submenu

Feature	Options	Description
AGP Aperture Size	• **64 MB (default)** • 256 MB	Sets the aperture size for the AGP video controller.
Primary Video Adapter	• **AGP (default)** • PCI	Selects primary video adapter to be used during boot.

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 72 is for setting passwords and security features.

Table 72. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• **Yes (default)** • No	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets BIOS Setup Utility access rights for user level.
Unattended Start (Note 1, Note 3, and Note 4)	• **Disabled (default)** • Enabled	*Enabled* allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password has been set.
3. If both Legacy USB and Unattended Start are set to enabled in the BIOS setup menu, USB aware operating systems can unlock as PS/2 style keyboard and mouse without requiring the user to enter a password.
4. When Unattended Start is enabled in the BIOS setup menu, a USB aware operating system may override user password protection if used in conjunction with a USB keyboard and mouse without requiring the user to enter a password.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The menu represented in Table 73 is for setting the power management features.

Table 73. Power Menu

Feature	Options	Description
ACPI	Select to display submenu	Sets the ACPI power management options.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC power loss occurs. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred. *Power On* restores power to the computer.
Wake on LAN	• **Stay Off (default)** • Power On	Specifies how the computer responds to a LAN wake up event.
Wake on PME	• **Stay Off (default)** • Power On	Specifies how the computer responds to a PCI power management event.
Wake on Modem Ring	• **Stay Off (default)** • Power On	Specifies how the computer responds to an incoming call on an installed modem when the power is off.

4.6.1 ACPI Submenu

To access this menu, select Power from the menu bar at the top of the screen and then ACPI.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit
				ACPI		

The submenu represented in Table 74 is for setting the ACPI power options.

Table 74. ACPI Submenu

Feature	Options	Description
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI sleep state.
Wake on LAN from S5	• **Stay Off (default)** • Power On	In ACPI soft-off mode only, determines how the system responds to a LAN wake-up event.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The menu represented in Table 75 is used to set the boot features and the boot sequence.

Table 75. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM graphic instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
Boot Device Priority	Select to display submenu	Specifies the boot sequence from the available types of boot devices.
Hard Disk Drives	Select to display submenu	Specifies the boot sequence from the available hard disk drives.
Removable Devices	Select to display submenu	Specifies the boot sequence from the available removable devices.
ATAPI CD-ROM Drives	Select to display submenu	Specifies the boot sequence from the available ATAPI CD-ROM drives.

4.7.1 Boot Device Priority Submenu

To access this menu, select Boot on the menu bar and then Boot Devices Priority.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 76 is for setting boot devices priority.

Table 76. Boot Device Priority Submenu

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device	• Removable Dev. • Hard Drive • ATAPI CD-ROM • Intel® Boot Agent • Disabled	Specifies the boot sequence according to the device type. The computer will attempt to boot from up to five devices as specified here. Only one of the devices can be an IDE hard disk drive. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The default settings for the first through fourth boot devices are, respectively: • Removable Dev. • Hard Drive • ATAPI CD-ROM • Intel Boot Agent

4.7.2 Hard Disk Drives Submenu

To access this menu, select Boot on the menu bar and then Hard Disk Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 77 is for setting hard disk drive priority.

Table 77. Hard Disk Drives Submenu

Feature	Options	Description
1st Hard Disk Drive (Note)	Dependent on installed hard drives	Specifies the boot sequence from the available hard disk drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to twelve hard disk drives, the maximum number of hard disk drives supported by the BIOS.

4.7.3 Removable Devices Submenu

To access this menu, select Boot on the menu bar, then Removable Devices.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 78 is for setting removable device priority.

Table 78. Removable Devices Submenu

Feature	Options	Description
1st Removable Device (Note)	Dependent on installed removable devices	Specifies the boot sequence from the available removable devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four removable devices, the maximum number of removable devices supported by the BIOS.

4.7.4 ATAPI CD-ROM Drives Submenu

To access this menu, select Boot on the menu bar and then ATAPI CD-ROM Drives.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					Boot Device Priority	
					Hard Disk Drives	
					Removable Devices	
					ATAPI CD-ROM Drives	

The submenu represented in Table 79 is for setting ATAPI CD-ROM drive priority.

Table 79. ATAPI CD-ROM Drives Submenu

Feature	Options	Description
1st ATAPI CDROM (Note)	Dependent on installed ATAPI CD-ROM drives	Specifies the boot sequence from the available ATAPI CD-ROM drives. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device.

Note: This boot device submenu appears only if at least one boot device of this type is installed. This list will display up to four ATAPI CD-ROM drives, the maximum number of ATAPI CD-ROM drives supported by the BIOS.

4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 80 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 80. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 81 lists the error messages and provides a brief description of each.

Table 81. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.
HDC Failure	Error occurred trying to access hard disk controller.

continued

Table 81. BIOS Error Messages (continued)

Error Message	Explanation
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM / CMOS / PASSWORD cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST-codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires a PCI bus add-in card, often called a POST card. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

NOTE

The POST card must be installed in PCI bus connector 1.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 82 defines the uncompressed INIT code checkpoints, Table 83 describes the boot block recovery code checkpoints, and Table 84 lists the runtime code uncompressed in F000 shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 82. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is Disabled. Onboard KBC, RTC enabled (if present). Init code Checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find Main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 83. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard Floppy Controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in Shadow RAM and give control to recovery code in F000 Shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel Recovery) Module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS-120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 84. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is Disabled. To check soft reset/power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking/unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA/VGA not found then do display memory R/W test.
2F	EGA/VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate Display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 84. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation/ shadow. Memory test above 1M to follow.
52	Memory testing/initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation/shadow.
58	Memory size adjusted for relocation/shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error/stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 84. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after Coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 84. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 85 describes the bus initialization checkpoints.

Table 85. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 86 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 86. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 87 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 87. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

5.4 Speaker (Optional)

A 47 Ω inductive speaker is mounted on the D845HV and the D845WN board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker on the D845HV board	Figure 1, page 14
The location of the onboard speaker on the D845WN board	Figure 2, page 15

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 88). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 88. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)