Intel® Desktop Board D815BN
Technical Product Specification

September 2000

Order Number A29192–001

The Intel® Desktop Board D815BN may contain design defects or errors known as errata that may cause the product to deviate from published specifications. Current characterized errata are documented in the Intel Desktop Board D815BN Specification Update.

Revision History

Revision	Revision History	Date
-001	First release of the Intel® Desktop Board D815BN Technical Product Specification	September 2000

This product specification applies to only standard D815BN boards with BIOS identifier BN81510A.86A.

Changes to this specification will be published in the Intel Desktop Board D815BN Specification Update before being incorporated into a revision of this document.

Preface

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for the Intel® Desktop Board D815BN. It describes the standard product and available manufacturing options.

Intended Audience

The TPS is intended to provide detailed, technical information about the D815BN board and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically *not* intended for general audiences.

What This Document Contains

Chapter	Description
1	A description of the hardware used on the D815BN board
2	A map of board resources
3	The features supported by the BIOS Setup program
4	The contents of the BIOS Setup program's menus and submenus
5	A description of the BIOS error messages, beep codes, power-on self-test (POST) codes, and diagnostic LEDs

Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

NOTE

Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

WARNING

Warnings indicate conditions, which if not observed, can cause personal injury.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#)
(NxnX)	When used in the description of a component, N indicates component type, xn are the relative coordinates of its location on the D815BN board, and X is the instance of the particular part at that general location. For example, J6A3 is a connector, located at 6A. It is the first connector in the 6A area.
GB	Gigabyte (1,073,741,824 bytes)
KB	Kilobyte (1024 bytes)
Kbit	Kilobit (1024 bits)
kbits/sec	1000 bits per second
MB	Megabyte (1,048,576 bytes)
MB/sec	Megabytes per second
Mbit	Megabit (1,048,576 bits)
Mbit/sec	Megabits per second
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
†	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

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4 BIOS Setup Program

5 Error Messages and Beep Codes

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1 Product Description

What This Chapter Contains

1.1 Overview

1.1.1 Feature Summary

Table 1 summarizes the D815BN board's major features.

Table 1. Feature Summary

Form Factor	microATX (9.6 inches by 8.5 inches)
Processor	Support for either an Intel® Pentium® III processor in a Flip Chip Pin Grid Array (FC-PGA) package or an Intel® Celeron™ processor in an FC-PGA package or a PPGA package
Memory	• Three 168-pin SDRAM Dual Inline Memory Module (DIMM) sockets • Support for up to 512 MB system memory • Single- or double-sided DIMMs supported
Chipset	Intel® 815 chipset, consisting of: • Intel® 82815 Graphics and Memory Controller Hub (GMCH) • Intel® 82801AA I/O Controller Hub (ICH) • Intel® 82802AB 4 Mbit Firmware Hub (FWH)
I/O Control	SMSC LPC47M142 I/O LPC bus controller
Video	• Intel® 82815 integrated graphics support • AGP universal connector supporting 1X, 2X, and 4X AGP cards or a Graphics Performance Accelerator (GPA) • Digital Video Output (DVO) connector
Peripheral Interfaces	• Four Universal Serial Bus (USB) ports • One serial port • One parallel port • Two IDE interfaces with Ultra DMA, ATA-33/66 support • One diskette drive interface • PS/2† keyboard and mouse ports
Expansion Capabilities	• Three PCI bus add-in card connectors (SMBus routed to PCI bus connector 2) • One GPA/AGP universal connector
BIOS	• Intel/AMI BIOS (resident in the Intel 82802AB 4 Mbit FWH) • Intel® Rapid BIOS boot • Support for Advanced Configuration and Power Interface (ACPI), Advanced Power Management (APM), Plug and Play, and SMBIOS
Diagnostic LEDs	Four dual-color LEDs on the back panel
Instantly Available PC	• Support for *PCI Local Bus Specification Revision 2.2* • Suspend to RAM support • Wake on PS/2 keyboard

For information about	Refer to
The board's compliance level with ACPI, APM, Plug and Play, and SMBIOS.	Section 1.3, page 16
The *PCI Local Bus Specification Revision 2.2*	Section 1.3, page 16

1.1.2 Manufacturing Options

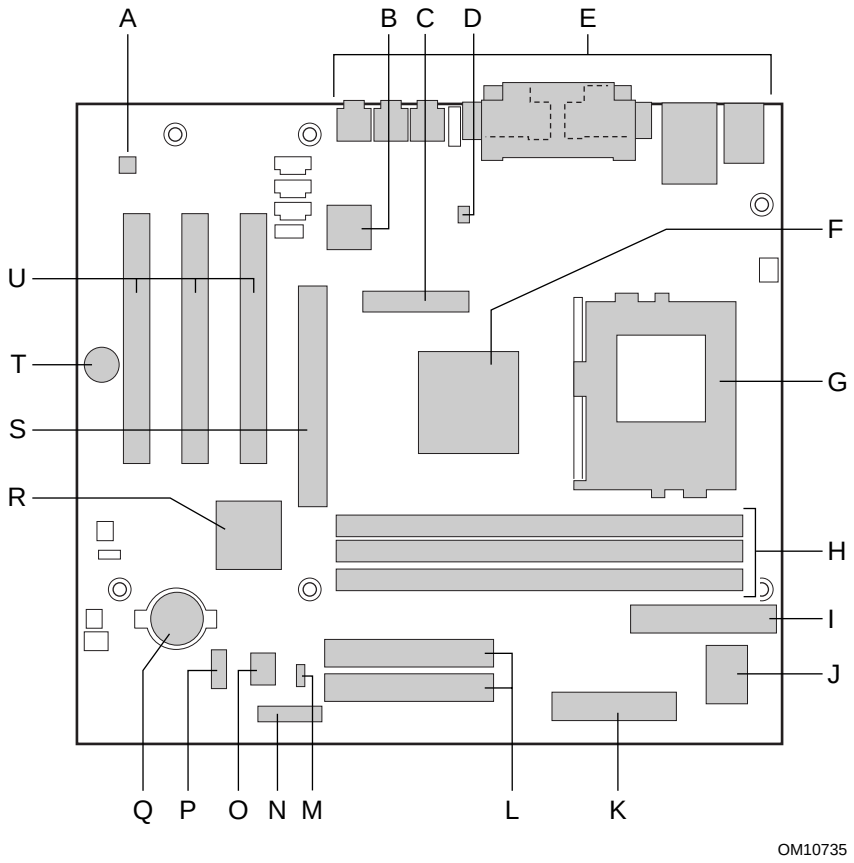
Table 2 describes the D815BN board's manufacturing options.

Table 2. Manufacturing Options

Audio	Audio Codec '97 (AC '97) compatible audio subsystem, consisting on the following: • Intel 82801AA ICH (AC link output) • Analog Devices AD1885 analog codec
LAN	Intel® 82559 LAN controller
Hardware Monitor	Voltage and temperature sensing to detect out of range values

1.1.3 D815BN Board Layout

Figure 1 shows the location of the major components on the D815BN board.



A	AD1885 analog codec (optional)	L	IDE connectors
B	Intel 82559 LAN controller (optional)	M	Front panel power LED connector
C	DVO connector	N	Auxiliary Front panel connector
D	Hardware monitor (optional)	O	Intel 82802AB 4 Mbit Firmware Hub (FWH)
E	Back panel connectors	P	Front panel USB connector
F	Intel 82815 Graphics and Memory Controller Hub (GMCH)	Q	Battery
G	Processor socket	R	Intel 82801AA I/O Controller Hub (ICH)
H	DIMM sockets	S	AGP universal connector
I	Diskette drive connector	T	Speaker
J	SMSC LPC47M142 I/O controller	U	PCI bus add-in card connectors
K	Power connector		

Figure 1. D815BN Board Components

1.1.4 Block Diagram

Figure 2 is a block diagram of the major functional areas of the D815BN board.

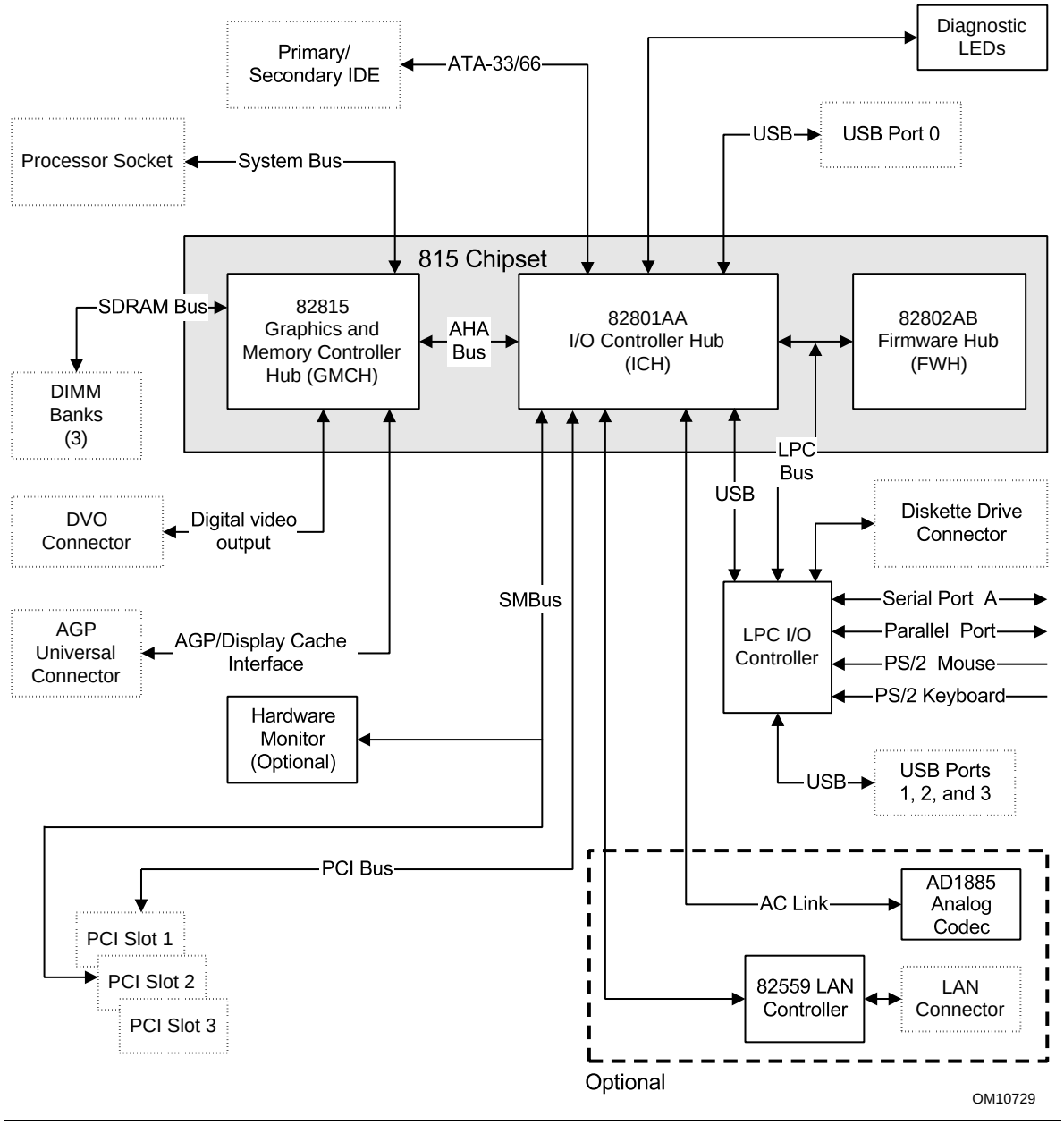


Figure 2. Block Diagram

1.2 Online Support

Find information about the Intel® D815BN board under "Product Info" or "Customer Support" at these World Wide Web sites:

http://www.intel.com/design/motherbd
http://support.intel.com/support/motherboards/desktop

Find "Processor Data Sheets" or information about "Proper Date Access in Systems with Intel® Motherboards" at these World Wide Web sites:

http://www.intel.com/design/litcentr
http://support.intel.com/support/year2000

Find information about the ICH addressing in the 82801AA datasheet at this World Wide Web site:
http://developer.intel.com/design/chipsets/datashts/

1.3 Design Specifications

Table 3 lists the specifications applicable to the D815BN board.

Table 3. Specifications

Reference Name	Specification Title	Version, Revision Date, and Ownership	The information is available from…
AC '97	*Audio Codec '97*	Version 2.1, May 1998, Intel Corporation.	http://developer.intel.com/ial/scalableplatforms/audio/index.htm
ACPI	*Advanced Configuration and Power Interface Specification*	Version 1.0b, February 8, 1999, Intel Corporation, Microsoft Corporation, and Toshiba Corporation.	http://www.teleport.com/~acpi/
AGP	*Accelerated Graphics Port Interface Specification*	Version 2.0, May 4, 1998, Intel Corporation.	Accelerated Graphics Implementers Forum at: http://www.agpforum.org/
AMI BIOS	*American Megatrends BIOS Specification*	AMIBIOS 99, 1999 American Megatrends, Inc.	http://www.amibios.com (Select AMIBIOS, then Desktops)
APM	*Advanced Power Management BIOS Interface Specification*	Version 1.2, February 1996, Intel Corporation, Microsoft Corporation.	http://www.microsoft.com/hwdev/busbios/amp_12.htm
ATA-3	*Information Technology - AT Attachment-3 Interface, X3T10/2008D*	Version 6, October 1995, ASC X3T10 Technical Committee.	ATA Anonymous FTP Site: ftp://www.dt.wdc.com/ata/ata-3/

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
ATAPI	*Information Technology AT Attachment with Packet Interface Extensions T13/1153D*	Version 18, August 19, 1998, Contact: T13 Chair, Seagate Technology.	T13 Anonymous FTP Site: ftp://fission.dt.wdc.com/x3t13/project/d1153r18.pdf
ATX	*ATX Specification*	Version 2.01, February 1997, Intel Corporation.	http://developer.intel.com/design/motherbd/atx.htm
BIS	*Boot Integrity Services Application Programming Interface*	Version 1.0, December 28, 1998, Intel Corporation.	http://developer.intel.com/ial/wfm/wfmspecs.htm
EPP	*Enhanced Parallel Port IEEE std 1284.1-1997*	Version 1.7, 1997, Institute of Electrical and Electronic Engineers.	http://standards.ieee.org/reading/ieee/std_public/description/busarch/1284.1-1997_desc.html
El Torito	*Bootable CD-ROM Format Specification*	Version 1.0, January 25, 1995, Phoenix Technologies Ltd., and IBM Corporation.	http://www.ptltd.com/products/specs-cdrom.pdf
GPA (formerly AIMM)	*AGP Inline Memory Module*	Version 1.0, April 2000, Intel Corporation	http://developer.intel.com/technology/memory/aimm/index.htm Intel document order number 298177-004
LPC	*Low Pin Count Interface Specification*	Version 1.0, September 29, 1997, Intel Corporation.	http://www.intel.com/design/chipsets/industry/lpc.htm
microATX	*microATX Motherboard Interface Specification*	Version 1.0, December 1997, Intel Corporation.	http://www.teleport.com/~ffsupprt/spec/microatxspecs.htm
	SFX Power Supply Design Guide	Version 1.1, February 1998, Intel Corporation.	ftp://download.intel.com/support/motherboards/microatx/SFX_PS.PDF
PCI	*PCI Local Bus Specification*	Version 2.2, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
	PCI Bus Power Management Interface Specification	Version 1.1, December 18, 1998, PCI Special Interest Group.	http://www.pcisig.com/
Plug and Play	*Plug and Play BIOS Specification*	Version 1.0a, May 5, 1994, Compaq Computer Corp., Phoenix Technologies Ltd., and Intel Corporation.	http://www.microsoft.com/hwdev/respec/pnpspecs.htm

continued

Table 3. Specifications (continued)

Reference Name	Specification Title	Version, Revision Date and Ownership	The information is available from…
PXE	*Preboot Execution Environment Specification*	Version 2.1, September 1999, Intel Corporation (with contributions from SystemSoft Corporation).	http://developer.intel.com/ial/WfM/wfmspecs.htm
SDRAM	*PC SDRAM Unbuffered DIMM Specification*	Revision 1.0, February 1998, Intel Corporation.	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
	PC SDRAM Specification	Revision 1.7, November 1999, Intel Corporation.	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
	PC SDRAM DIMM Serial Presence Detect (SPD) Specification	Revision 1.2B, November 1999 Intel Corporation.	http://developer.intel.com/technology/memory/pcsdram/spec/index.htm
SMBIOS	*System Management BIOS Reference Specification*	Version 2.3.1, March 16, 1999 American Megatrends Inc., Award Software International Inc., Compaq Computer Corporation, Dell Computer Corporation, Hewlett-Packard Company, Intel Corporation, International Business Machines Corporation, Phoenix Technologies Limited, and SystemSoft Corporation.	http://developer.intel.com/ial/WfM/wfm20/design/smbios
UHCI	*Universal Host Controller Interface Design Guide*	Version 1.1, March 1996, Intel Corporation.	http://developer.intel.com/design/USB/UHCI11D.htm
USB	*Universal Serial Bus Specification*	Version 1.1, September 23, 1998, Compaq Computer Corporation, Intel Corporation, Microsoft Corporation, and NEC.	http://www.usb.org/developers
WfM	*Wired for Management Baseline*	Version 2.0, December 18, 1998, Intel Corporation.	http://developer.intel.com/ial/WfM/wfmspecs.htm

1.4 Processor

CAUTION

The D815BN board supports processors that have a 19.4 A maximum current draw with a 1.65 to 2.0 V core voltage. Using a processor not in compliance with the above guidelines can damage the processor, the D815BN board, and the power supply. See the processor's data sheet for voltage and current usage requirements.

The D815BN board supports a single Pentium III or Celeron processor. The system bus speed is automatically selected. The D815BN board supports the processors listed in Table 4.

Table 4. Supported Processors

Type	Designation	System Bus Frequency	L2 Cache Size
Pentium III processor in an FC-PGA package	533EB, 600EB, 667, 733, 800B, 866, 933, and 1.0	133 MHz	256 KB
	500E, 550E, 600E, 650, 700, 750, 800, and 850	100 MHz	256 KB
Celeron processor in an FC-PGA package	533A, 566, 600, 633, 667, and 700	66 MHz	128 KB
Celeron processor in a PPGA package	500 and 533	66 MHz	128 KB

All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

For information about	Refer to
Processor support	Section 1.2, page 16
Processor data sheets	Section 1.2, page 16

1.5 System Memory

The D815BN board has three DIMM sockets and supports the following memory features:

- 3.3 V (only) 168-pin SDRAM DIMMs with gold-plated contacts
- Unbuffered single- or double-sided DIMMs
- Maximum system memory: 512 MB; minimum system memory: 32 MB
- 133 MHz SDRAM or 100 MHz SDRAM
- Serial Presence Detect (SPD) and non-SPD memory
- Non-ECC and ECC DIMMs (ECC DIMMs will operate in non-ECC mode only.)
- Suspend to RAM

Table 5 lists the supported DIMM configurations. In the second column of Table 5:

- "DS" refers to double-sided memory modules (containing two rows of SDRAM)
- "SS" refers to single-sided memory modules (containing one row of SDRAM)

When installing memory, note the following:

- Non-SPD DIMMs will always revert to a 100 MHz SDRAM bus with 3-3-3 timing.
- Mixing non-SPD DIMMs with SPD DIMMs will always revert to a 100 MHz SDRAM bus with 3-3-3 timing.
- The BIOS will not initialize installed memory above 512 MB. At boot, the BIOS displays a message indicating that any installed memory above 512 MB has not been initialized.
- Mixed memory speed configurations (133 and 100 MHz) will default to 100 MHz.
- 133 MHz SDRAM operation requires a 133 MHz system bus frequency processor.
- The board should be populated with no more than four rows of 133 MHz SDRAM (two double-sided or one double-sided plus two single-sided DIMMs).
- 100 MHz SDRAM may be populated with six rows of SDRAM (three double-sided DIMMs).

NOTE

If more than four rows of 133 MHz SDRAM are populated, the BIOS will initialize installed memory up to 512 MB at 100 MHz.

Table 5. Supported Memory Configurations

DIMM Capacity	Number of Sides	SDRAM Density	SDRAM Organization		Number of SDRAM Devices
			Front-side	Back-side	
32 MB	DS	16 Mbit	2 M X 8	2 M X 8	16 (Note 1)
32 MB	SS	64 Mbit	4 M X 16	Empty	4
48 MB	DS	64/16 Mbit	4 M X 16	2 M X 8	12 (Notes 1 and 2)
64 MB	DS	64 Mbit	4 M X 16	4 M X 16	8
64 MB	SS	64 Mbit	8 M X 8	Empty	8
64 MB	SS	128 Mbit	8 M X 16	Empty	4
96 MB	DS	64 Mbit	8 M X 8	4 M x 16	12 (Notes 1 and 2)
96 MB	DS	128/64 Mbit	8 M X 16	4 M x 16	8 (Notes 1 and 2)
128 MB	DS	64 Mbit	8 M X 8	8 M X 8	16 (Note 1)
128 MB	DS	128 Mbit	8 M X 16	8 M X 16	8 (Notes 1 and 2)
128 MB	SS	128 Mbit	16 M X 8	Empty	8
128 MB	SS	256 Mbit	16 M X 16	Empty	4
192 MB	DS	128 Mbit	16 M X 8	8 M x 16	12 (Notes 1 and 2)
192 MB	DS	128/64 Mbit	16 M X 8	8 M x 8	16 (Notes 1 and 2)
256 MB	DS	128 Mbit	16 M X 8	16 M X 8	16 (Notes 1 and 2)
256 MB	DS	256 Mbit	16 M X 16	16 M X 16	8 (Notes 1 and 2)
256 MB	SS	256 Mbit	32 M X 8	Empty	8
512 MB	DS	256 Mbit	32 M X 8	32 M X 8	16 (Notes 1 and 2)

Notes:

1 If the number of SDRAM devices is greater than nine, the DIMM will be double sided.

2 Front side population/back side population indicated for SDRAM density and SDRAM organization.

⚠ CAUTION

To be fully compliant with all applicable Intel® SDRAM memory specifications, the motherboard should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. If your memory modules do not support SPD, you will see a notification to this effect on the screen at power up. The BIOS will attempt to configure the memory controller for normal operation. However, DIMMs may not function under the determined frequency.

For information about	Refer to
The PC Serial Presence Detect Specification	Section 1.3, page 16

1.6 Intel® 815 Chipset

The Intel 815 chipset consists of the following devices:

- 82815 Graphics and Memory Controller Hub (GMCH) with Accelerated Hub Architecture (AHA) bus
- 82801AA I/O Controller Hub (ICH) with AHA bus
- 82802AB Firmware Hub (FWH)

The GMCH is a centralized controller for the system bus, the memory bus, the AGP bus, and the Accelerated Hub Architecture interface. The ICH is a centralized controller for the board's I/O paths. The FWH provides the nonvolatile storage of the BIOS as well as hardware-dependent security features. The chipset provides the interfaces shown in Figure 3.

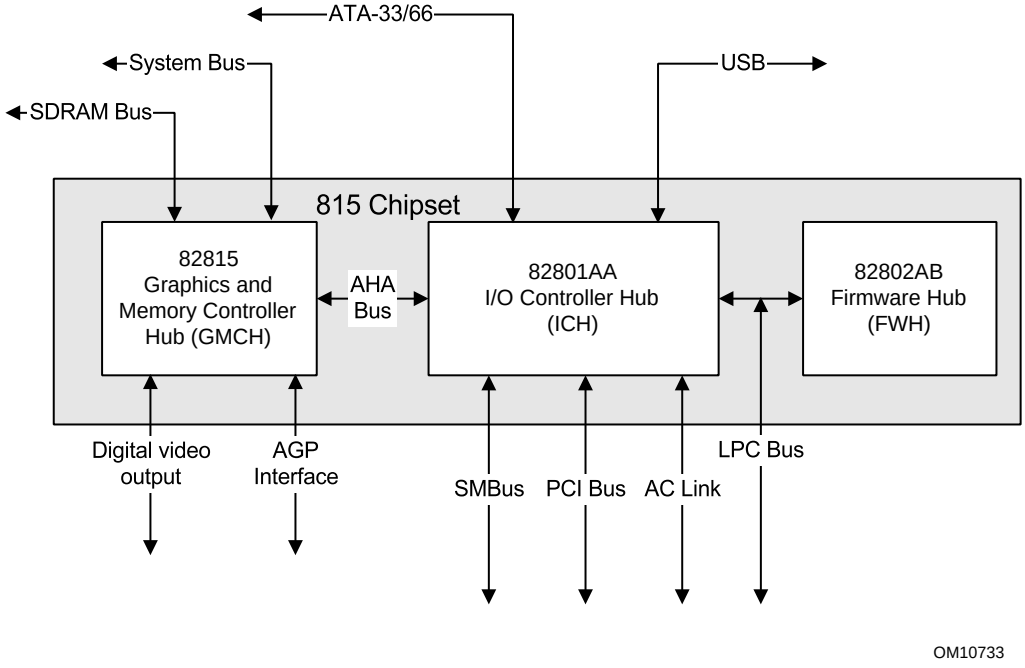


Figure 3. Intel 815 Chipset Block Diagram

For information about	Refer to
The Intel 815 chipset	http://developer.intel.com
The resources used by the chipset	Chapter 2
The chipset's compliance with AC '97, ACPI, and APM	Section 1.3, page 16

1.6.1 Intel® 82815 Graphics and Memory Controller Hub (GMCH)

The GMCH provides the following:

- An integrated synchronous DRAM memory controller with autodetection of SDRAM
- An interface for a single AGP device or a Graphics Performance Accelerator (GPA) card
- An interface for a digital video output (DVO) connector for a flat panel digital CRT or TV out
- Support for ACPI Rev 1.0 and APM Rev 1.2 compliant power management

1.6.2 Intel® 82801AA I/O Controller Hub (ICH)

The ICH provides the following:

- 33 MHz PCI bus interface with support for three *PCI Local Bus Specification* Rev. 2.2-compliant slots
- Support for up to four PCI master devices
- One Advanced Graphics Port
- Low Pin Count (LPC) interface that supports an LPC-compatible I/O controller
- Support for two master/DMA devices
- Integrated IDE controller that supports Ultra DMA (33 MB/sec) and ATA-66 mode (66 MB/sec)
- Universal Serial Bus interface with one USB controller providing two ports in a UHCI implementation
- Power management logic for ACPI Rev 1.0b compliance
- System Management Bus (SMBus clock and data lines also routed to PCI bus connector 2)
- Real-Time Clock with 256-byte battery-backed CMOS RAM
- AC'97 digital link for Audio and telephony codecs, including:
  - AC'97 2.1 compliance
  - Logic for PCM in, PCM out, mic input, modem in, and modem out
  - Separate PCI functions for audio and modem

1.6.2.1 IDE Interfaces

The ICH's IDE controller has two independent bus-mastering IDE interfaces that can be independently enabled. The IDE interfaces support the following modes:

- Programmed I/O (PIO): CPU controls data transfer.
- 8237-style DMA: DMA offloads the CPU, supporting transfer rates of up to 16 MB/sec.
- Ultra DMA: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 33 MB/sec.
- Ultra ATA-66: DMA protocol on IDE bus supporting host and target throttling and transfer rates of up to 66 MB/sec. ATA-66 protocol is similar to ATA-33 and is device driver compatible. ATA-66 uses faster timings and requires a specialized cable to reduce reflections, noise, and inductive coupling.

The IDE interfaces also support ATAPI devices (such as CD-ROM drives) and ATA devices using the transfer modes listed in Table 64 on page 101.

The BIOS supports logical block addressing (LBA) and extended cylinder head sector (ECHS) translation modes. The drive reports the transfer rate and translation mode to the BIOS.

The D815BN board supports laser servo (LS-120) diskette technology through its IDE interfaces. The LS-120 drive can be configured as a boot device by setting the BIOS Setup program's Boot menu to one of the following:

- ARMD-FDD (ATAPI removable media device – floppy disk drive)
- ARMD-HDD (ATAPI removable media device – hard disk drive)

For information about	Refer to
The location of the IDE connectors	Figure 8, page 60
The signal names of the IDE connectors	Table 39, page 64
BIOS Setup program's Boot menu	Table 70, page 108

1.6.2.2 USB

The D815BN board has four USB ports. The ICH includes a USB controller and the LPC47M142 features a USB hub and drives three USB ports. One USB peripheral can be connected to each port. For more than four USB devices, an external hub can be connected to any of the ports. Two of the USB ports are implemented with stacked back panel connectors; the other two are accessible via the front panel USB connector at location J8B1. The D815BN board fully supports UHCI and uses UHCI-compatible software drivers.

NOTE

Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device or a low-speed USB device is attached to the cable. Use shielded cable that meets the requirements for full-speed devices.

For information about	Refer to
The location of the USB connectors on the back panel	Figure 6, page 52
The signal names of the back panel USB connectors	Table 20, page 53
The location of the front panel USB connector	Figure 9, page 65
The signal names of the front panel USB connector	Table 41, page 66
The USB specification and UHCI	Section 1.3, page 16

1.6.2.3 Real-Time Clock, CMOS SRAM, and Battery

The real-time clock provides a time-of-day clock and a multicentury calendar with alarm features. The real-time clock supports 256 bytes of battery-backed CMOS SRAM in two banks that are reserved for BIOS use.

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied.

The time, date, and CMOS values can be specified in the BIOS Setup program. The CMOS values can be returned to their defaults by using the BIOS Setup program.

NOTES

If the battery and AC power fail, the last saved defaults, custom or standard, will be loaded into CMOS RAM at power-on.

The recommended method of accessing the date in systems with D815BN boards is indirectly from the Real-Time Clock (RTC) via the BIOS. The BIOS on D815BN boards contains a century checking and maintenance feature. This feature checks the two least significant digits of the year stored in the RTC during each BIOS request (INT 1Ah) to read the date and, if less than 80 (i.e., 1980 is the first year supported by the PC), updates the century byte to 20. This feature enables operating systems and applications using the BIOS date/time services to reliably manipulate the year as a four-digit value.

For information about	Refer to
Proper date access in systems with D815BN boards	Section 1.2, page 16

1.6.3 Intel® 82802AB 4 Mbit Firmware Hub (FWH)

The FWH provides the following:

- System BIOS
- System security and manageability logic that enables protection for storing and updating of platform information

1.7 I/O Controller

The SMSC LPC47M142 I/O controller provides the following features:

- Low pin count (LPC) interface
- 3.3 V operation
- One serial port
- One parallel port with Extended Capabilities Port (ECP) and Enhanced Parallel Port (EPP) support
- One USB hub supporting three USB ports
- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- PS/2-style mouse and keyboard interfaces
- Interface for one 1.2 MB, 1.44 MB, or 2.88 MB diskette drive
- Intelligent power management, including a programmable wake up event interface
- PCI power management support
- Fan control:
  - — Two fan tachometer inputs
  - — Two fan control outputs

The BIOS Setup program provides configuration options for the I/O controller.

For information about	Refer to
SMSC LPC47M142 I/O controller	http://www.smsc.com

1.7.1 Serial Port

The D815BN board has one serial port, which is located on the back panel. The serial port's NS16C550-compatible UART supports data transfers at speeds up to 115.2 kbits/sec with BIOS support. The serial port can be assigned as COM1 (3F8h), COM2 (2F8h), COM3 (3E8h), or COM4 (2E8h).

For information about	Refer to
The location of the serial port connector	Figure 6, page 52
The signal names of the serial port connector	Table 23, page 54

1.7.2 Parallel Port

The connector for the multimode bidirectional parallel port is a 25-pin D-sub connector located on the back panel. In the BIOS Setup program, the parallel port can be configured for the following:

- Output only (PC AT†-compatible mode)
- Bi-directional (PS/2 compatible)
- EPP
- ECP

For information about	Refer to
The location of the parallel port connector	Figure 6, page 52
The signal names of the parallel port connector	Table 22, page 54

1.7.3 Diskette Drive Controller

The I/O controller supports one diskette drive that is compatible with the 82077 diskette drive controller and supports both PC-AT and PS/2 modes.

For information about	Refer to
The location of the diskette drive connector	Figure 8, page 60
The signal names of the diskette drive connector	Table 38, page 63
The supported diskette drive capacities and sizes	Table 65, page 103

1.7.4 Keyboard and Mouse Interface

PS/2 keyboard and mouse connectors are located on the back panel. The +5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an overcurrent condition is removed.

NOTE

The keyboard is supported in the bottom PS/2 connector and the mouse is supported in the top PS/2 connector. Power to the computer should be turned off before a keyboard or mouse is connected or disconnected.

The keyboard controller contains the AMI keyboard and mouse controller code, provides the keyboard and mouse control functions, and supports password protection for power-on/reset. A power-on/reset password can be specified in the BIOS Setup program.

For information about	Refer to
The location of the keyboard and mouse connectors	Figure 6, page 52
The signal names of the keyboard and mouse connectors	Table 18, page 53

1.8 Graphics Subsystem

The 815 chipset supports three graphics options: using the integrated GMCH graphics controller, using an add-in AGP adapter, or using an add-in PCI adapter.

When using the GMCH graphics controller, a Graphics Performance Accelerator (GPA) card can be installed (in the AGP connector) for enhanced 2D and 3D graphics performance. The GPA card has a 32-bit 133 MHz SDRAM display cache; which is controlled by the GMCH graphics memory controller.

When an add-in AGP adapter is installed, the GMCH graphics controller is disabled.

For information about	Refer to
GPA card support	Section 1.8.3.1, page 30

1.8.1 Integrated Graphics Controller

The GMCH features the following:

- Integrated graphics controller
  - 3D hyper-pipelined architecture
  - Full 2D hardware acceleration
  - Motion video acceleration
- 3D graphics visual and texturing enhancement
- Display
  - Integrated 24-bit 230 MHz RAMDAC
  - Compliant with *Display Data Channel Standard*, Version 3.0, Level 2B protocol
- Video
  - Hardware motion compensation for software MPEG2 decode
  - Software DVD at 30 fps
- Integrated graphics memory controller

Table 6 lists the refresh frequencies supported by the graphics subsystem.

Table 6. Supported Graphics Refresh Frequencies

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
320 x 200	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
320 x 240	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 480	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
352 x 576	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
400 x 300	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
512 x 384	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 400	256 colors	70	D
	64 K colors	70	D3
	16 M colors	70	D
640 x 480	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 75, 85	KD3O
	64 K colors	70, 72	KDO
640 x 480	16 M colors	60, 70, 72, 75, 85	KDO
800 x 600	256 colors	60, 70, 72, 75, 85	KDO
	64 K colors	60, 70, 72, 75, 85	KD3O
	16 M colors	60, 70, 72, 75, 85	KDO
1024 x 768	256 colors	60, 70, 75, 85	KDO
	64 K colors	60, 70, 75	KD3O
	64 K colors	85	KD3
	16 M colors	60, 70, 75, 85	KD

continued

Table 6. Supported Graphics Refresh Frequencies (continued)

Resolution	Color Palette	Available Refresh Frequencies (Hz)	Notes
1152 x 864	256 colors	60, 70, 72, 75	KDO
	256 colors	85	KD
	64 K colors	60, 70	KD3O
	64 K colors	72, 75, 85	KD3
	16 M colors	60	KDO
	16 M colors	75, 85	KD
1280 x 768	256 colors	60 (reduced blanking)	KDOF
	64 K colors	60 (reduced blanking)	KD3F
	16 M colors	60 (reduced blanking)	KDF
1280 x 1024	256 colors	60	KDO
	256 colors	70, 72, 75, 85	KD
	64 K colors	60, 70, 72, 75, 85	KD3
	16 M colors	60, 70, 75, 85	KD
1600 x 1200	256 colors	60, 70, 72, 75	KD

Notes: K = Desktop
D = DirectDraw†
3 = Direct3D† and OpenGL†
O = Overlay
F = Digital Display Device only. A mode will be supported on both analog CRTs and digital display devices (the KD3O flags above apply to both types of displays), unless indicated otherwise.

For information about	Refer to
Obtaining graphics software and utilities	Section 1.2, page 16

1.8.2 Digital Video Output (DVO) Connector

The board routes the Intel 82815 GMCH DVO port to an onboard 40-pin DVO connector. When a Digital Visual Interface (DVI) or TV out card is installed in a back panel slot and cabled to the DVO connector, the system supports DVI-compliant digital displays or TV out functionality. Use of the DVO connector requires use of the onboard GMCH graphics controller.

For information about	Refer to
The location of the DVO connector	Figure 7, page 56
The signal names of the DVO connector	Table 31, page 58

1.8.3 AGP Universal Connector

The AGP universal connector supports either:

- A GPA card with 133 MHz SDRAM display cache
- An AGP add-in card with 3.3 V or 1.5 V I/O

NOTE

The cable connectors inserted in the ATAPI connectors may interfere with the installation of some AGP cards. This is due to the location of the ATAPI connectors and depends on the AGP card layout. Interference does not occur when using the legacy-style 2-mm CD ROM connector.

For information about	Refer to
The location of the AGP universal connector	Figure 8, page 60
The signal names of the AGP universal connector	Table 37, page 62

1.8.3.1 Graphics Performance Accelerator (GPA) Card Support

The BIOS detects if a GPA card is present in the AGP connector and initializes up to 4 MB of display cache on the card. The GMCH graphics memory controller accesses the display cache over a single channel 32-bit SDRAM interface.

NOTE

In earlier documentation, the GPA card was referred to as the Add-In Memory Module (AIMM).

1.8.3.2 AGP Add-in Card Support

AGP is a high-performance interface for graphics-intensive applications, such as 3D applications. While based on the *PCI Local Bus Specification*, Rev. 2.1, AGP is independent of the PCI bus and is intended for exclusive use with graphical display devices. AGP overcomes certain limitations of the PCI bus related to handling large amounts of graphics data with the following features:

- Pipelined memory read and write operations that hide memory access latency
- Demultiplexing of address and data on the bus for nearly 100 percent efficiency

For information about	Refer to
Obtaining the *Accelerated Graphics Port Interface Specification*	Section 1.3, page 16

1.9 Audio Subsystem (Optional)

The board includes an Audio Codec ’97 (AC ’97) compatible SoundMAX† audio subsystem consisting of these devices:

- Intel 82801AA I/O Controller Hub (ICH)
- Analog Devices AD1885 analog codec

Figure 4 is a block diagram of the audio subsystem.

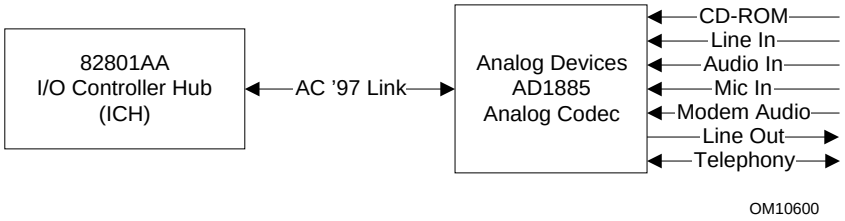


Figure 4. Block Diagram of Audio Subsystem

Features of the audio subsystem include:

- Power management support for APM 1.2 and ACPI 1.0 (driver dependant)
- 3D stereo enhancement

1.9.1 AD1885 Audio Codec

The AD1885 is a fully AC ’97 compliant codec. The codec’s features include:

- PC 99 compliant:
  - ≥80 dB FSA dynamic range (S/N ratio)
  - Playback sample rates up to 48 kHz
  - Frequency response: 20 Hz to 20 kHz
- 64 voice synthesizer
- Software compatible with Windows† 98 Gold and SE, Windows 2000, and Windows NT† 4.0
- Full-duplex operation at asynchronous hardware record/playback sample rates

1.9.2 Audio Connectors

The audio connectors include the following:

- Legacy-style 2-mm CD-ROM
- ATAPI CD-ROM
- ATAPI-style connectors:
  - Telephony
  - Auxiliary line in
- Back panel audio connectors:
  - Line out
  - Line in
  - Mic in

For information about	Refer to
The back panel audio connectors	Section 2.8.1, page 52

CAUTION

The pins on both the legacy-style 2-mm and the ATAPI CD-ROM connectors are wired to the same inputs on the audio mixer. Do not attach CD-ROM drives to both connectors. Otherwise, the board could be damaged.

NOTE

The cable connectors inserted in the ATAPI connectors may interfere with the installation of some AGP cards. This is due to the location of the ATAPI connectors and depends on the AGP card layout. Interference does not occur when using the legacy-style 2-mm CD ROM connector.

1.9.2.1 Legacy-style 2-mm CD-ROM Audio Connector

A 1 x 4-pin legacy-style 2-mm connector connects an internal CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the legacy-style 2-mm connector	Figure 7, page 56
The signal names of the legacy-style 2-mm connector	Table 30, page 57

1.9.2.2 ATAPI CD-ROM Audio Connector

A 1 x 4-pin ATAPI-style connector connects an internal ATAPI CD-ROM drive to the audio mixer.

For information about	Refer to
The location of the ATAPI CD-ROM connector	Figure 7, page 56
The signal names of the ATAPI CD-ROM connector	Table 29, page 57

1.9.2.3 Telephony Connector

A 1 x 4-pin ATAPI-style connector connects the monoaural audio signals of an internal telephony device to the audio subsystem. A monaural audio-in and audio-out signal interface is necessary for telephony applications such as speakerphones, fax/modems, and answering machines.

For information about	Refer to
The location of the telephony connector	Figure 7, page 56
The signal names of the telephony connector	Table 27, page 57

1.9.2.4 Auxiliary Line In Connector

A 1 x 4-pin ATAPI-style connector connects the left and right channel signals of an internal audio device to the audio subsystem.

For information about	Refer to
The location of the auxiliary line in connector	Figure 7, page 56
The signal names of the auxiliary line in connector	Table 28, page 57

1.10 LAN Subsystem (Optional)

The Intel 82559 Fast Ethernet Wired for Management (WfM) PCI LAN subsystem provides both 10Base-T and 100Base-TX connectivity. Features include:

- 32-bit, 33 MHz direct bus mastering on the PCI bus
- 10Base-T and 100Base-TX capability using a single RJ-45 connector with connection and activity status LEDs
- IEEE 802.3u Auto-Negotiation for the fastest available connection
- Jumperless configuration; the LAN subsystem is completely software-configurable

For information about	Refer to
The WfM specification	Table 3, page 16

1.10.1 Intel® 82559 PCI LAN Controller

The Intel 82559 PCI LAN controller's features include:

- CSMA/CD Protocol Engine
- PCI bus interface
- DMA engine for movement of commands, status, and network data across the PCI bus
- Integrated physical layer interface, including:
  - — Complete functionality necessary for the 10Base-T and 100Base-TX network interfaces; when in 10 Mbit/sec mode, the interface drives the cable directly
  - — A complete set of Media Independent Interface (MII) management registers for control and status reporting

— IEEE 802.3u Auto-Negotiation for automatically establishing the best operating mode when connected to other 10Base-T or 100Base-TX devices, whether half- or full-duplex capable

— Integrated power management features, including support for wake on network event (from an ACPI S3 state using the PCI bus PME# signal)

For information about	Refer to
The LAN subsystem's PCI specification compliance	Section 1.3, page 16

1.10.2 LAN Subsystem Software

The Intel 82559 Fast Ethernet WfM PCI LAN software and drivers are available from Intel's World Wide Web site.

For information about	Refer to
Obtaining LAN software and drivers	Section 1.2, page 16

1.10.3 RJ-45 LAN Connector LEDs

Two LEDs are built into the RJ-45 LAN connector. Table 7 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 7. LAN Connector LED States

LED Color	LED State	Condition
Green	Off	10 Mbit/sec data rate is selected.
	On	100 Mbit/sec date rate is selected.
Yellow	Off	LAN link is not established.
	On (steady state)	LAN link is established.
	On (brighter and pulsing)	The computer is communicating with another computer on the LAN.

1.11 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Hardware monitor (optional)
- Chassis intrusion detect connector
- Fan monitoring and control (using the SMSC LPC47M142 I/O controller)

For information about	Refer to
The WfM specification	Section 1.3, page 16
Fan control functions of the SMSC LPC47M142 I/O controller	Section 1.11.3, page 35

1.11.1 Hardware Monitor Component (Optional)

The hardware monitor component provides low-cost instrumentation capabilities. The features of the component include:

- Internal ambient temperature sensing
- Remote thermal diode sensing for direct monitoring of processor temperature (if supported in the processor)
- Power supply monitoring (+12 V, +5 V, +3.3 V, +2.5 V, 3.3 VSB, V_{CCP}) to detect levels above or below acceptable values
- SMBus interface

1.11.2 Chassis Intrusion Detect Connector

The board supports a chassis security feature that detects if the chassis cover is removed and sounds an alarm through the onboard speaker. For the chassis intrusion circuit to function, the chassis' power supply must be connected to AC power. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion detect connector. The mechanical switch is closed for normal computer operation.

For information about	Refer to
The location of the chassis intrusion detect connector	Figure 7, page 56
The signal names of the chassis intrusion detect connector	Table 34, page 59

1.11.3 Fan Control and Monitoring

The SMSC LPC47M142 I/O controller provides two fan control output and two fan tachometer inputs. Monitoring and control can be implemented using third-party software.

For information about	Refer to
The functions of the fan connectors	Section 1.12.2.2, page 40
The location of the fan connectors	Figure 7, page 56
The signal names of the fan connectors	Section 2.8.2, page 56

1.12 Power Management

Power management is implemented at several levels, including:

- Software support:
  - Advanced Power Management (APM)
  - Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan connectors
  - Wake on LAN† technology
  - Instantly Available technology
  - Wake on Ring
  - Resume on Ring
  - Wake on Keyboard
  - Wake on PME#

1.12.1 Software Support

The software support for power management includes:

- APM
- ACPI

If the D815BN board is used with an ACPI-aware operating system, the BIOS can provide ACPI support. Otherwise, it defaults to APM support.

1.12.1.1 APM

APM makes it possible for the computer to enter an energy-saving standby mode. The standby mode can be initiated in the following ways:

- Time-out period specified in the BIOS Setup program
- From the operating system, such as the Standby menu item in Windows 98

In standby mode, the D815BN board can reduce power consumption by spinning down hard drives, and reducing power to, or turning off of, VESA† DPMS-compliant monitors. Power management mode can be enabled or disabled in the BIOS Setup program.

While in standby mode, the system retains the ability to respond to external interrupts and service requests, such as incoming faxes or network messages. Any keyboard or mouse activity brings the system out of standby mode and immediately restores power to the monitor.

The BIOS enables APM by default but the operating system must support an APM driver for the power management features to work. For example, Windows 98 supports the power management features upon detecting that APM is enabled in the BIOS.

For information about	Refer to
Enabling or disabling power management in the BIOS Setup program	Section 4.6, page 106
The D815BN board's compliance level with APM	Section 1.3, page 16

1.12.1.2 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with the D815BN board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration) and APM support normally contained in the BIOS
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 30-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake up events (see Table 10 on page 39)
- Support for a front panel power and sleep mode switch. Table 8 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 8. Effects of Pressing the Power Switch

If the system is in this state…	…and the power switch is pressed for	…the system enters this state
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than four seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than four seconds	Power-off (ACPI G2/G5 – Soft off)

For information about	Refer to
The D815BN board's compliance level with ACPI	Section 1.3, page 16

1.12.1.2.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 9 lists the power states supported by the D815BN board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 9. Power States and Targeted System Power

Global States	Sleeping States	CPU States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state	Full power > 30 W
G1 – sleeping state	S1 – CPU stopped	C1 – stop grant	D1, D2, D3 – device specification specific.	5 W < power < 30 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake up logic.	Power < 5 W (Note 2)
G2/G5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake up logic, except when provided by battery or external source.	No power to the system so that service can be performed.

Notes: 1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.

2. Dependent on the standby power consumption of wake-up devices used in the system.

1.12.1.2.2 Wake Up Devices and Events

Table 10 lists the devices or specific events that can wake the computer from specific states.

Table 10. Wake Up Devices and Events

These devices/events can wake up the computer…	…from this state
Power switch	S1, S3, S5
RTC alarm	S1, S3, S5
Onboard LAN	S1, S3, S5 (Note)
PME#	S1, S3, S5 (Note)
Modem (back panel serial port)	S1, S3
PS/2 keyboard, USB keyboard, or USB mouse	S1, S3

Note: For LAN and PME#, S5 is disabled by default in the BIOS Setup program. In BIOS Setup, setting the On ACPI S5 option to Power On will enable a wake-up event from LAN in the S5 state.

NOTE

The use of these wake up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

1.12.1.2.3 Plug and Play

In addition to power management, ACPI provides controls and information so that the operating system can facilitate Plug and Play device enumeration and configuration. ACPI is used only to enumerate and configure D815BN board devices that do not have other hardware standards for enumeration and configuration.

1.12.2 Hardware Support

CAUTION

If the Wake on LAN and Instantly Available technology features are used, ensure that the power supply provides adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 74 for additional information.

The board provides several hardware features that support power management, including:

- Power connector
- Fan connectors
- Wake on LAN technology
- Instantly Available technology
- Wake on Ring
- Resume on Ring
- Wake from PS/2 keyboard
- PME# wakeup support

Wake on LAN technology and Instantly Available technology require power from the +5 V standby line. The sections discussing these features describe the incremental standby power requirements for each.

Resume on Ring enables telephony devices to access the computer when it is in a power-managed state. The method used depends on the type of telephony device (external or internal) and the power management mode being used (APM or ACPI).

NOTE

The use of Resume on Ring technology from an ACPI state requires an operating system that provides full ACPI support.

1.12.2.1 Power Connector

When used with an ATX-compliant power supply that supports remote power on/off, the D815BN board can turn off the system power through software control. To enable soft-off control in software, advanced power management must be enabled in the BIOS Setup program and in the operating system. When the system BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer.

With soft-off enabled, if power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the After Power Failure feature in the BIOS Setup program's Boot menu.

For information about	Refer to
The location of the power connector	Figure 7, page 56
The signal names of the power connector	Table 33, page 58
The BIOS Setup program's Boot menu	Table 70, page 108
The ATX specification	Section 1.3, page 16

1.12.2.2 Fan Connectors

The D815BN board has two fan connectors. The functions of these connectors are described in Table 11.

Table 11. Fan Connector Descriptions

Connector	Function
System fan (fan 1)	Provides +12 V DC for a system or chassis fan. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided.
Processor fan (fan 2)	Provides +12 V DC for a processor fan or active fan heatsink. The fan voltage can be switched on or off, depending on the power management state of the computer. A tachometer feedback connection is also provided.

For information about	Refer to
The location of the fan connectors	Figure 7, page 56
The signal names of the fan connectors	Section 2.8.2, page 56

1.12.2.3 Wake on LAN Technology

⚠ CAUTION

For Wake on LAN technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Wake on LAN technology can damage the power supply. Refer to Section 2.11.3 on page 74 for additional information.

Wake on LAN technology enables remote wakeup of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet† frame, the LAN subsystem asserts a wakeup signal that powers up the computer. Depending on the LAN implementation, the D815BN board supports Wake on LAN technology in the following ways:

- Through the PCI bus PME# signal for PCI 2.2 compliant LAN designs
- Through the onboard LAN subsystem when enabled in Setup (ACPI only)

Network adapters that are PCI 2.2 compliant assert the wakeup signal through the PCI bus signal PME# (pin A19 on the PCI bus connectors).

1.12.2.4 Instantly Available Technology

⚠ CAUTION

For Instantly Available technology, the 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available technology can damage the power supply. Refer to Section 2.11.3 on page 74 for additional information.

Instantly Available technology enables the D815BN board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, the fans are off, and the front panel LED is amber if dual-color, or off if single-color.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 10 on page 39 lists the devices and events that can wake the computer from the S3 state.

The D815BN board supports the *PCI Bus Power Management Interface Specification.* For information on the versions of this specification, see Section 1.3. Add-in boards that also support this specification can participate in power management and can be used to wake the computer.

The use of Instantly Available technology requires operating system support and PCI 2.2 compliant add-in cards and drivers.

The standby power LED shows that power is still present at the DIMM and PCI bus connectors, even when the computer appears to be off. Figure 5 shows the location of the standby power indicator LED.

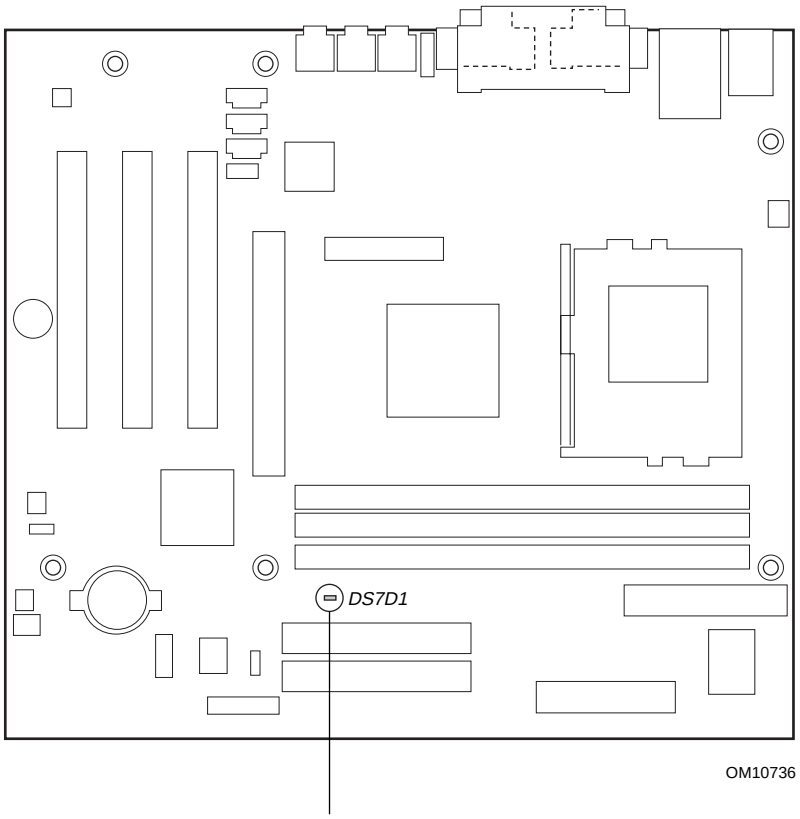


Figure 5. Location of Standby Power LED

1.12.2.5 Wake on Ring

The operation of Wake on Ring can be summarized as follows:

- Powers up the computer from the APM soft-off mode.
- Requires two calls to access the computer:
  - First call restores the computer.
  - Second call enables access (when supporting software is installed).
- Detects incoming call differently for external as opposed to internal modems:
  - For external modems, D815BN board hardware monitors the ring indicator (RI) input of the serial port.
  - For internal modems, the D815BN board is awakened using the PME# signal.

1.12.2.6 Resume on Ring

The operation of Resume on Ring can be summarized as follows:

- Resumes operation from either the APM sleep mode or the ACPI S1 state
- Requires only one call to access the computer
- Detects incoming call similarly for external and internal modems
- Requires modem interrupt be unmasked for correct operation

1.12.2.7 Wake from PS/2 Keyboard and Mouse

PS/2 keyboard and mouse activity wakes the computer from an ACPI S1 or S3 state.

1.12.2.8 PME# Wakeup Support

When the PME# signal on the PCI bus is asserted, the computer wakes from an ACPI S1 or S3 state.

2 Technical Reference

What This Chapter Contains

2.1 Introduction

Sections 2.2 - 2.6 contain several standalone tables. Table 12 describes the system memory map, Table 13 shows the I/O map, Table 14 lists the DMA channels, Table 15 defines the PCI configuration space map, and Table 16 describes the interrupts. The remaining sections in this chapter are introduced by text found with their respective section headings.

2.2 Memory Map

Table 12. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 524288 K	100000 - 1FFFFFFF	511 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Available high DOS memory (open to the PCI bus)
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

2.3 I/O Map

Table 13. I/O Map

Address (hex)	Size	Description
0000 - 000F	16 bytes	DMA controller
0020 - 0021	2 bytes	Programmable Interrupt Control (PIC)
0040 - 0043	4 bytes	System timer
0060	1 byte	Keyboard controller byte—reset IRQ
0061	1 byte	System speaker
0064	1 byte	Keyboard controller, CMD / STAT byte
0070 - 0071	2 bytes	System CMOS / Real Time Clock
0072 - 0073	2 bytes	System CMOS
0080 - 008F	16 bytes	DMA controller
0092	1 byte	Fast A20 and PIC
00A0 - 00A1	2 bytes	PIC
00B2 - 00B3	2 bytes	APM control
00C0 - 00DF	32 bytes	DMA
00F0	1 byte	Numeric data processor
0170 - 0177	8 bytes	Secondary IDE channel
01F0 - 01F7	8 bytes	Primary IDE channel
One of these ranges: 0220 - 022F 0240 - 024F	16 bytes	Audio (Sound Blaster Pro† -compatible)
0228 - 022F*	8 bytes	LPT3
0278 - 027F*	8 bytes	LPT2
02E8 - 02EF*	8 bytes	COM4 / video (8514A)
02F8 - 02FF*	8 bytes	COM2
0376	1 byte	Secondary IDE channel command port
0378 - 037F	8 bytes	LPT1
0388 - 038B	6 bytes	SoundMAX
03B0 - 03BB	12 bytes	Intel 82815 GMCH
03C0 - 03DF	32 bytes	Intel 82815 GMCH
03E8 - 03EF	8 bytes	COM3

continued

Table 13. I/O Map (continued)

Address (hex)	Size	Description
03F0 - 03F5	6 bytes	Diskette channel 1
03F6	1 byte	Primary IDE channel command port
03F8 - 03FF	8 bytes	COM1
04D0 - 04D1	2 bytes	Edge / level triggered PIC
LPTn + 400	8 bytes	ECP port, LPTn base address + 400h
0CF8 - 0CFB**	4 bytes	PCI configuration address register
0CF9***	1 byte	Turbo and reset control register
0CFC - 0CFF	4 bytes	PCI configuration data register
FFA0 - FFA7	8 bytes	Primary bus master IDE registers
FFA8 - FFAF	8 bytes	Secondary bus master IDE registers
96 contiguous bytes starting on a 128-byte divisible boundary		ICH (ACPI + Total Cost of Ownership)
64 contiguous bytes starting on a 64-byte divisible boundary		D815BN board resource
256 contiguous bytes starting on a 32-byte divisible boundary		ICH (audio mixer)
64 contiguous bytes starting on a 64-byte divisible boundary		ICH (audio bus master)
32 contiguous bytes starting on a 32-byte divisible boundary		ICH (USB)
16 contiguous bytes starting on a 16-byte divisible boundary		ICH (SMBus)
4096 contiguous bytes starting on a 4096-byte divisible boundary		Intel 82801AA PCI bridge
96 contiguous bytes starting on a 128-byte divisible boundary		LPC47M142 PME# status
32 contiguous bytes starting on a 32-byte divisible boundary		Intel 82559 LAN controller (optional)

* Default, but can be changed to another address range.

** Dword access only.

*** Byte access only.

NOTE

Some additional I/O addresses are not available due to ICH addresses aliassing. For information about the ICH addressing, refer to Section 1.2 on page 16.

2.4 DMA Channels

Table 14. DMA Channels

DMA Channel Number	Data Width	System Resource
0	8- or 16-bits	Audio
1	8- or 16-bits	Audio / parallel port
2	8- or 16-bits	Diskette drive
3	8- or 16-bits	Parallel port (for ECP or EPP) / audio
4	8- or 16-bits	DMA controller
5	16-bits	Open
6	16-bits	Open
7	16-bits	Open

2.5 PCI Configuration Space Map

Table 15. PCI Configuration Space Map

Bus Number (hex)	Device Number (hex)	Function Number (hex)	Description
00	00	00	Memory controller of Intel 82815 component
00	01	00	PCI to AGP bridge
00	02	00	Intel 82815 GMCH (graphics memory controller hub)
00	1E	00	Hub link to PCI bridge
00	1F		Intel 82801AA ICH PCI to LPC bridge
00	1F	01	IDE controller
00	1F	02	USB
00	1F	03	SMBus controller
00	1F	04	USB
00	1F	05	AC '97 audio controller (optional)
00	1F	06	AC '97 modem controller (optional)
01	01	00	Intel 82559 LAN controller (optional)
01	08	00	PCI bus connector 1 (J4C1)
01	09	00	PCI bus connector 2 (J4B1)
01	0A	00	PCI bus connector 3 (J4A1)
02 (Note)	00	00	Add-in AGP adapter card

Note: If an add-in AGP card is installed, it occupies PCI Bus 02.

2.6 Interrupts

Table 16. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note)
4	COM1 (Note)
5	LPT2 (Plug and Play option) / Audio / User available
6	Diskette drive
7	LPT1 (Note)
8	Real-time clock
9	Reserved for ICH system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

Note: Default, but can be changed to another IRQ

2.7 PCI Interrupt Routing Map

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The ICH has four programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D815BN board and therefore share the same interrupt. Table 17 shows an example of how the PIRQ signals are routed on the D815BN board.

For example, using Table 17 as a reference, assume an add-in card using INTA is plugged into PCI bus connector 2. In PCI bus connector 2, INTA is connected to PIRQB, which is already connected to the SMBus.

Table 17. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name			
	PIRQA	**PIRQB**	**PIRQC**	**PIRQD**
GMCH	INTA	INTB		
ICH USB controller				INTD
SMBus controller		INTB		
ICH audio / modem		INTB		
Intel 82559 LAN controller				INTA
PCI bus connector 1 (J4C1)	INTA	INTB	INTC	INTD
PCI bus connector 2 (J4B1)	INTD	INTA	INTB	INTC
PCI bus connector 3 (J4A1)	INTC	INTD	INTA	INTB

NOTE

The ICH can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal.

2.8 Connectors

⚠ CAUTION

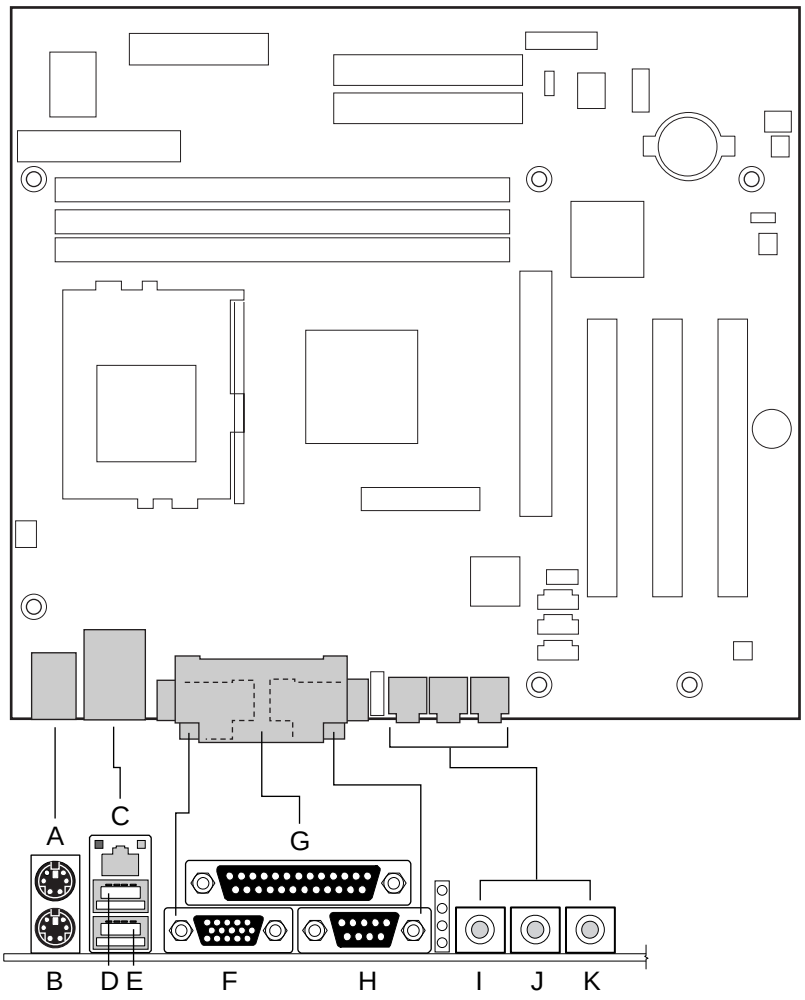
Only the back panel connectors of the D815BN board have overcurrent protection. The D815BN board's internal connectors are not overcurrent protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the interconnecting cable, and the external devices themselves.

This section describes the board's connectors. The connectors can be divided into the following groups:

- Back panel I/O connectors (see page 52)
  - PS/2 keyboard and mouse
  - LAN
  - USB (2)
  - VGA
  - Parallel port
  - Serial port
  - Audio (line out, line in, and mic in)
- Audio, video, power, and hardware control connectors (see page 56)
  - Audio (telephony, auxiliary line input, ATAPI CD-ROM, legacy-style CD-ROM)
  - Digital video out
  - Fans (2)
  - Power
  - Chassis intrusion
- Add-in board and peripheral interface connectors (see page 60)
  - Add-in boards (three PCI bus connectors and one AGP universal connector)
  - Diskette drive
  - IDE (2)
- External I/O connectors (see page 65)
  - SCSI hard drive activity LED
  - Front panel USB
  - Auxiliary front panel power LED
  - Front panel (power/sleep/message-waiting LED, power switch, hard drive activity LED, reset switch)

2.8.1 Back Panel Connectors

Figure 6 shows the location of the back panel connectors. The back panel connectors are color-coded in compliance with PC 99 recommendations, as listed in the figure.



Item	Description	Color	For more information see:
A	PS/2 mouse port	Green	Table 18
B	PS/2 keyboard port	Purple	Table 18
C	LAN	Black	Table 19
D	USB port 0	Black	Table 20
E	USB port 1	Black	Table 20
F	VGA port	Dark blue	Table 21
G	Parallel port	Burgundy	Table 22
H	Serial port	Teal	Table 23
I	Audio line out	Lime green	Table 24
J	Audio line in	Light blue	Table 25
K	Mic in	Pink	Table 26

Figure 6. Back Panel Connectors

NOTE

The back panel audio line out connector is designed to power headphones or amplified speakers only. Poor audio quality occurs if passive (non-amplified) speakers are connected to this output.

Table 18. PS/2 Mouse/Keyboard Connectors

Pin	Signal Name
1	Data
2	Not connected
3	Ground
4	Fused +5 V
5	Clock
6	Not connected

Table 19. LAN Connector

Pin	Signal Name
1	TX+
2	TX-
3	RX+
4	Ground
5	Ground
6	RX-
7	Ground
8	Ground

Table 20. USB Connectors

Pin	Signal Name
1	+5 V (fused)
2	USBP0# [USBP1#]
3	USBP0 [USBP1]
4	Ground

Signal names in brackets ([ ]) are for USB port 1.

Table 21. VGA Port Connector

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
1	Red	6	Ground	11	No connect
2	Green	7	Ground	12	MONID1
3	Blue	8	Ground	13	HSYNC
4	No connect	9	Fused VCC	14	VSYNC
5	Ground	10	Ground	15	MONID2

Table 22. Parallel Port Connector

Pin	Standard Signal Name	ECP Signal Name	EPP Signal Name
1	STROBE#	STROBE#	WRITE#
2	PD0	PD0	PD0
3	PD1	PD1	PD1
4	PD2	PD2	PD2
5	PD3	PD3	PD3
6	PD4	PD4	PD4
7	PD5	PD5	PD5
8	PD6	PD6	PD6
9	PD7	PD7	PD7
10	ACK#	ACK#	INTR
11	BUSY	BUSY#, PERIPHACK	WAIT#
12	PERROR	PE, ACKREVERSE#	PE
13	SELECT	SELECT	SELECT
14	AUDOFD#	AUDOFD#, HOSTACK	DATASTB#
15	FAULT#	FAULT#, PERIPHREQST#	FAULT#
16	INIT#	INIT#, REVERSERQST#	RESET#
17	SLCTIN#	SLCTIN#	ADDRSTB#
18 - 25	GND	GND	GND

Table 23. Serial Port Connector

Pin	Signal Name
1	DCD (Data Carrier Detect)
2	RXD# (Receive Data)
3	TXD# (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request to Send)
8	CTS (Clear to Send)
9	RI (Ring Indicator)

Table 24. Audio Line Out Connector

Pin	Signal Name
Tip	Audio left out
Ring	Audio right out
Sleeve	Ground

Table 25. Audio Line In Connector

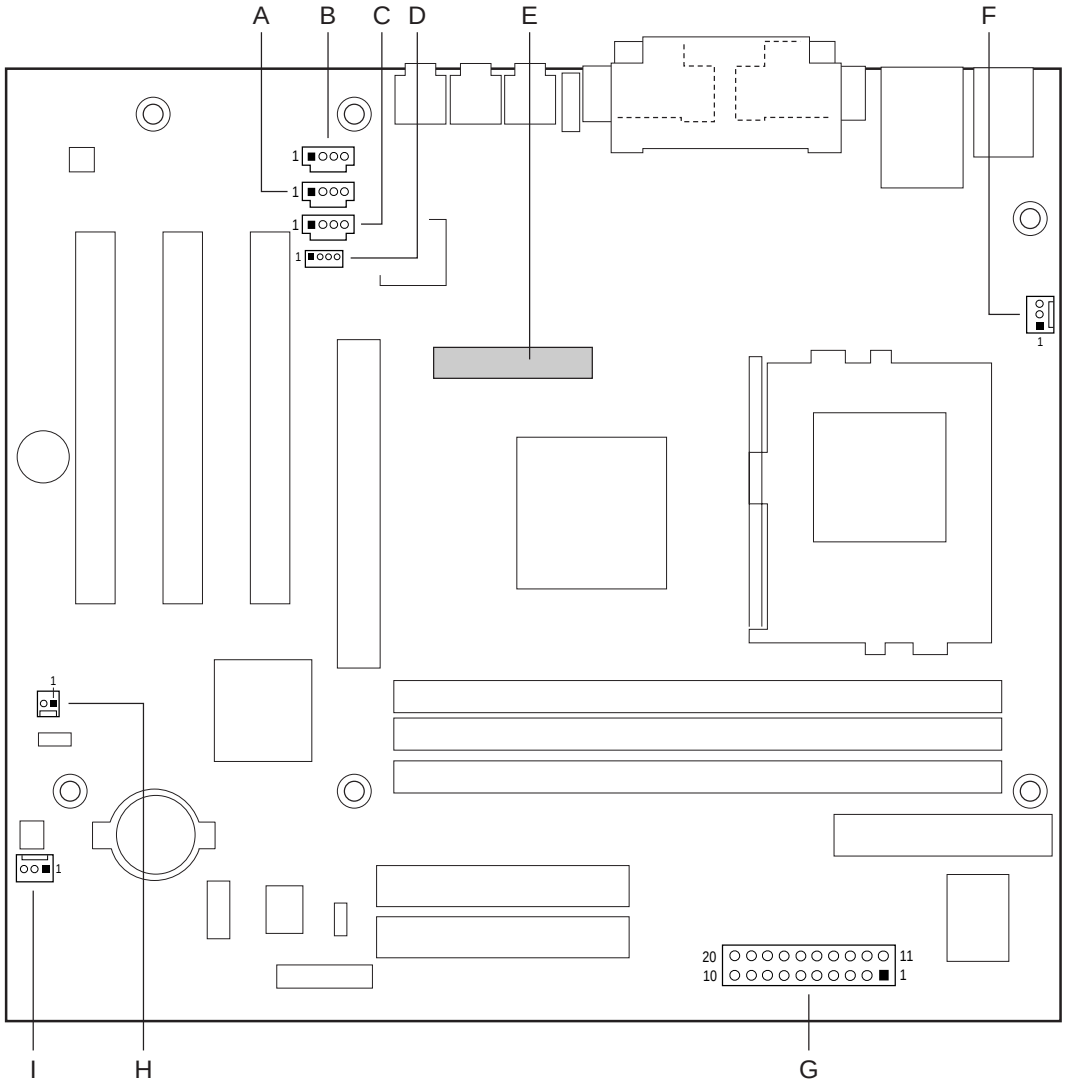
Pin	Signal Name
Tip	Audio left in
Ring	Audio right in
Sleeve	Ground

Table 26. Mic In Connector

Pin	Signal Name
Tip	Mono in
Ring	Mic bias voltage
Sleeve	Ground

2.8.2 Audio, Video, Power, and Hardware Control Connectors

Figure 7 shows the location of the audio, video, power, and hardware control connectors.



Item	Description	Color	Reference Designator	For more information, see:
A	Telephony, ATAPI-style	N/A	J2C1	Table 27
B	Auxiliary line in, ATAPI-style	Black	J1C1	Table 28
C	CD-ROM, ATAPI	Green	J2C2	Table 29
D	CD-ROM, legacy-style 2-mm	White	J2C3	Table 30
E	Digital video out	N/A	J3E1	Table 31
F	Processor fan (Fan 2)	N/A	J3K1	Table 32
G	Power	N/A	J8H1	Table 33
H	Chassis intrusion	N/A	J6A1	Table 34
I	Chassis fan (Fan 1)	N/A	J8A1	Table 35

Figure 7. Audio, Video, Hardware Control, and Fan Connectors

For information about	Refer to
The power connector	Section 1.12.2.1, page 40
The functions of the fan connectors	Section 1.12.2.2, page 40

Table 27. Telephony Connector, ATAPI-style (J2C1)

Pin	Signal Name
1	Analog audio mono input
2	Ground
3	Ground
4	Analog audio mono output

Table 28. Auxiliary Line In Connector, ATAPI-style (J1C1)

Pin	Signal Name
1	Left auxiliary line in
2	Ground
3	Ground
4	Right auxiliary line in

Table 29. CD-ROM Connector, ATAPI (J2C2)

Pin	Signal Name
1	Left audio input from CD-ROM
2	CD audio differential ground
3	CD audio differential ground
4	Right audio input from CD-ROM

Table 30. CD-ROM Connector, Legacy-style 2-mm (J2C3)

Pin	Signal Name
1	CD_Ground
2	CD_IN-Left
3	CD_Ground
4	CD_IN-Right

Table 31. Digital Video Out Connector (J3E1)

Pin	Signal Name	Pin	Signal Name
1	LTVCLKIN	2	+5 VDC
3	P_RST_SLOTS#	4	LTVCL_3V
5	Ground	6	LTVDA_3V
7	Ground	8	LTVVSYNC
9	Ground	10	LTVHSYNC
11	Ground	12	LTVDAT0
13	Ground	14	LTVDAT1
15	Ground	16	LTVDAT2
17	Ground	18	LTVDAT3
19	Ground	20	LTVDAT4
21	Ground	22	LTVDAT5
23	Ground	24	LTVDAT6
25	Ground	26	LTVDAT7
27	Ground	28	LTVDAT8
29	Ground	30	LTVDAT9
31	Ground	32	LTVDAT10
33	Ground	34	LTVDAT11
35	Ground	36	LTVCLKOUT0
37	Ground	38	LTVCLKOUT1
39	Ground	40	LTVBLNK#

Table 32. Processor Fan Connector (J3K1)

Pin	Signal Name
1	Ground
2	+12 V
3	FAN1_TACH

Table 33. Power Connector (J8H1)

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	11	+3.3 V
2	+3.3 V	12	-12 V
3	Ground	13	Ground
4	+5 V	14	PS-ON# (Power Supply Remote On/off)
5	Ground	15	Ground
6	+5 V	16	Ground
7	Ground	17	Ground
8	PWRGD (Power good)	18	No connect
9	+5 V (Standby)	19	+5 V
10	+12 V	20	+5 V

Table 34. Chassis Intrusion Connector (J6A1)

Pin	Signal Name
1	INTRUDER#
2	Ground

Table 35. Chassis Fan Connector (J8A1)

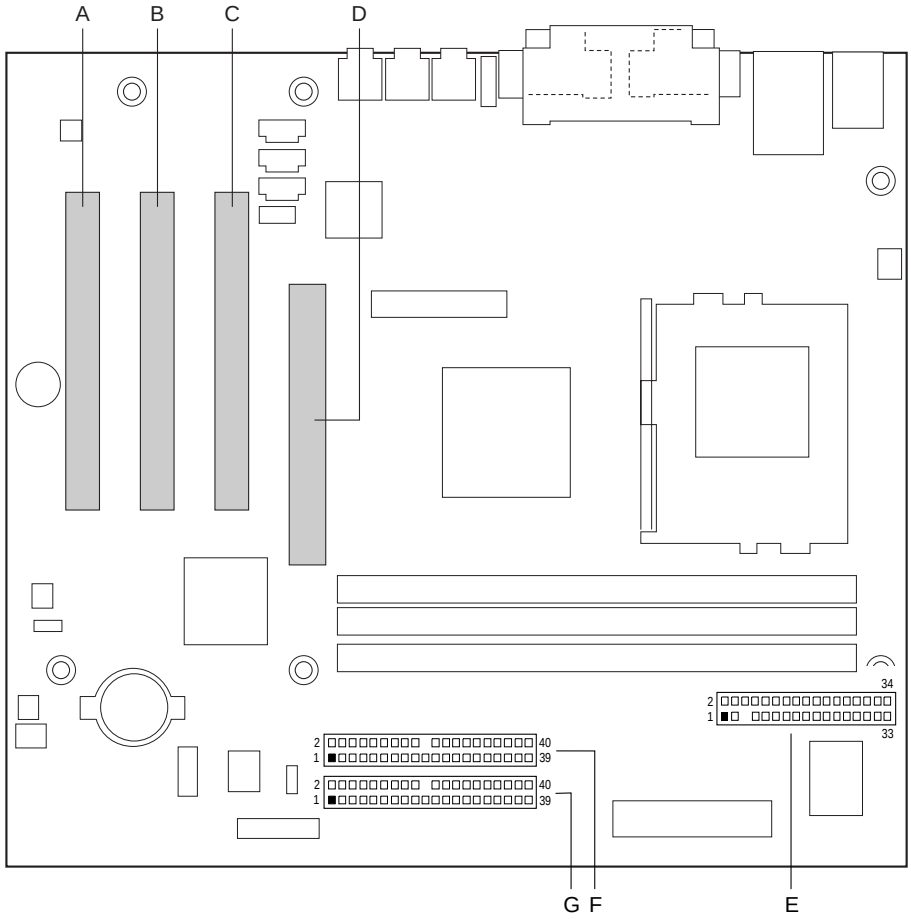
Pin	Signal Name
1	Ground
2	+12 V
3	FAN2_TACH

For information about	Refer to
The power connector	Section 1.12.2.1, page 40
The functions of the fan connectors	Section 1.12.2.2, page 40
Wake on LAN technology	Section 1.12.2.3, page 41

2.8.3 Add-in Board and Peripheral Interface Connectors

Figure 8 shows the location of the add-in board connectors and peripheral connectors. Note the following considerations for the PCI bus connectors:

- All of the PCI bus connectors are bus master capable.
- SMBUS signals are routed to PCI bus connector 2. This enables PCI bus add-in boards with SMBus support to access sensor data on the board. The specific SMBus signals are as follows:
  - The SMBus clock line is connected to pin A40
  - The SMBus data line is connected to pin A41



Item	Description	Reference Designator	For more information see:
A	PCI bus connector 3	J4A1	Table 36
B	PCI bus connector 2	J4B1	Table 36
C	PCI bus connector 1	J4C1	Table 36
D	AGP universal connector	J5D1	Table 37
E	Diskette drive	J7J1	Table 38
F	Secondary IDE	J8E1	Table 39
G	Primary IDE	J8E2	Table 39

Figure 8. Add-in Board and Peripheral Interface Connectors

Table 36. PCI Bus Connectors (J4A1, J4B1, J4C1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	Ground (TRST#)*	B1	-12 V	A32	AD16	B32	AD17
A2	+12 V	B2	Ground (TCK)*	A33	+3.3 V	B33	C/BE2#
A3	+5 V (TMS)*	B3	Ground	A34	FRAME#	B34	Ground
A4	+5 V (TDI)*	B4	no connect (TDO)*	A35	Ground	B35	IRDY#
A5	+5 V	B5	+5 V	A36	TRDY#	B36	+3.3 V
A6	INTA#	B6	+5 V	A37	Ground	B37	DEVSEL#
A7	INTC#	B7	INTB#	A38	STOP#	B38	Ground
A8	+5 V	B8	INTD#	A39	+3.3 V	B39	LOCK#
A9	Reserved	B9	no connect (PRSNT1#)*	A40	Reserved **	B40	PERR#
A10	+5 V (I/O)	B10	Reserved	A41	Reserved ***	B41	+3.3 V
A11	Reserved	B11	no connect (PRSNT2#)*	A42	Ground	B42	SERR#
A12	Ground	B12	Ground	A43	PAR	B43	+3.3 V
A13	Ground	B13	Ground	A44	AD15	B44	C/BE1#
A14	+3.3 V Aux	B14	Reserved	A45	+3.3 V	B45	AD14
A15	RST#	B15	Ground	A46	AD13	B46	Ground
A16	+5 V (I/O)	B16	CLK	A47	AD11	B47	AD12
A17	GNT#	B17	Ground	A48	Ground	B48	AD10
A18	Ground	B18	REQ#	A49	AD09	B49	Ground
A19	PME#	B19	+5 V (I/O)	A50	Key	B50	Key
A20	AD30	B20	AD31	A51	Key	B51	Key
A21	+3.3 V	B21	AD29	A52	C/BE0#	B52	AD08
A22	AD28	B22	Ground	A53	+3.3 V	B53	AD07
A23	AD26	B23	AD27	A54	AD06	B54	+3.3 V
A24	Ground	B24	AD25	A55	AD04	B55	AD05
A25	AD24	B25	+3.3 V	A56	Ground	B56	AD03
A26	IDSEL	B26	C/BE3#	A57	AD02	B57	Ground
A27	+3.3 V	B27	AD23	A58	AD00	B58	AD01
A28	AD22	B28	Ground	A59	+5 V (I/O)	B59	+5 V (I/O)
A29	AD20	B29	AD21	A60	REQ64C#	B60	ACK64C#
A30	Ground	B30	AD19	A61	+5 V	B61	+5 V
A31	AD18	B31	+3.3 V	A62	+5 V	B62	+5 V

* These signals (in parentheses) are optional in the PCI specification and are not currently implemented.

** On PCI bus connector 2 (J4B1), this pin is connected to the SMBus clock line.

*** On PCI bus connector 2 (J4B1), this pin is connected to the SMBus data line.

Table 37. AGP Universal Connector (J5D1)

Pin	Signal Name	Pin	Signal Name	Pin	Signal Name	Pin	Signal Name
A1	+12V	B1	No Connect	A34	Vcc3.3	B34	Vcc3.3
A2	TYPEDET#	B2	Vcc	A35	AD22	B35	AD21
A3	Reserved	B3	Vcc	A36	AD20	B36	AD19
A4	No Connect	B4	No Connect	A37	Ground	B37	Ground
A5	Ground	B5	Ground	A38	AD18	B38	AD17
A6	INTA#	B6	INTB#	A39	AD16	B39	C/BE2#
A7	RST#	B7	CLK	A40	Vcc3.3	B40	Vcc3.3
A8	GNT1#	B8	REQ#	A41	FRAME#	B41	IRDY#
A9	Vcc3.3	B9	Vcc3.3	A42	Reserved	B42	+3.3 V aux
A10	ST1	B10	ST0	A43	Ground	B43	Ground
A11	Reserved	B11	ST2	A44	Reserved	B44	Reserved
A12	PIPE#	B12	RBF#	A45	Vcc3.3	B45	Vcc3.3
A13	Ground	B13	Ground	A46	TRDY#	B46	DEVSEL#
A14	WBF#	B14	No Connect	A47	STOP#	B47	Vcc3.3
A15	SBA1	B15	SBA0	A48	PME#	B48	PERR#
A16	Vcc3.3	B16	Vcc3.3	A49	Ground	B49	Ground
A17	SBA3	B17	SBA2	A50	PAR	B50	SERR#
A18	SBSTB#	B18	SB_STB	A51	AD15	B51	C/BE1#
A19	Ground	B19	Ground	A52	Vcc3.3	B52	Vcc3.3
A20	SBA5	B20	SBA4	A53	AD13	B53	AD14
A21	SBA7	B21	SBA6	A54	AD11	B54	AD12
A22	Key	B22	Key	A55	Ground	B55	Ground
A23	Key	B23	Key	A56	AD9	B56	AD10
A24	Key	B24	+3.3 V aux	A57	C/BE0#	B57	AD8
A25	Key	B25	Key	A58	Vcc3.3	B58	Vcc3.3
A26	AD30	B26	AD31	A59	AD_STB0#	B59	AD_STB0
A27	AD28	B27	AD29	A60	AD6	B60	AD7
A28	Vcc3.3	B28	Vcc3.3	A61	Ground	B61	Ground
A29	AD26	B29	AD27	A62	AD4	B62	AD5
A30	AD24	B30	AD25	A63	AD2	B63	AD3
A31	Ground	B31	Ground	A64	Vcc3.3	B64	Vcc3.3
A32	AD_STB1#	B32	AD_STB1	A65	AD0	B65	AD1
A33	C/BE3#	B33	AD23	A66	VRREFG_C	B66	VREFC_G

Table 38. Diskette Drive Connector (J7J1)

Pin	Signal Name	Pin	Signal Name
1	Ground	2	DENSEL
3	Ground	4	Reserved
5	Key	6	FDEDIN
7	Ground	8	FDINDX# (Index)
9	Ground	10	FDM00# (Motor Enable A)
11	Ground	12	No connect
13	Ground	14	FDDS0# (Drive Select A)
15	Ground	16	No connect
17	No connect	18	FDDIR# (Stepper Motor Direction)
19	Ground	20	FDSTEP# (Step Pulse)
21	Ground	22	FDWD# (Write Data)
23	Ground	24	FDWE# (Write Enable)
25	Ground	26	FDTRK0# (Track 0)
27	No connect	28	FDWPD# (Write Protect)
29	Ground	30	FDRDATA# (Read Data)
31	Ground	32	FDHEAD# (Side 1 Select)
33	Ground	34	DSKCHG# (Diskette Change)

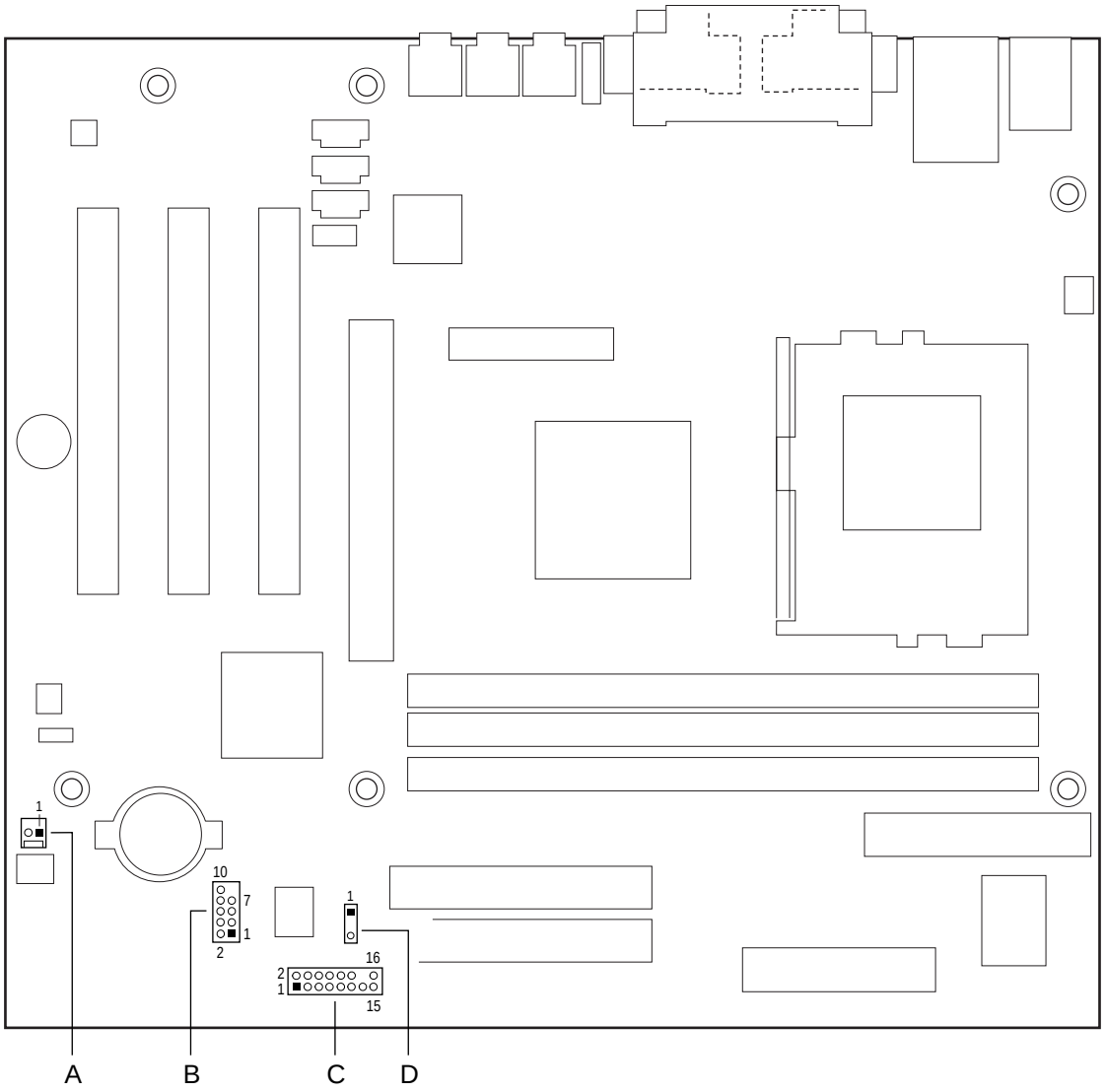
Table 39. PCI IDE Connectors (J8E2, Primary and J8E1, Secondary)

Pin	Signal Name	Pin	Signal Name
1	Reset IDE	2	Ground
3	Data 7	4	Data 8
5	Data 6	6	Data 9
7	Data 5	8	Data 10
9	Data 4	10	Data 11
11	Data 3	12	Data 12
13	Data 2	14	Data 13
15	Data 1	16	Data 14
17	Data 0	18	Data 15
19	Ground	20	Key
21	DDRQ0 [DDRQ1]	22	Ground
23	I/O Write#	24	Ground
25	I/O Read#	26	Ground
27	IOCHRDY	28	P_ALE (Cable Select Pull-up)
29	DDACK0# [DDACK1#]	30	Ground
31	IRQ 14 [IRQ 15]	32	Reserved
33	DAG1 (Address 1)	34	GPIO_DMA66_Detect_Pri (GPIO_DMA66_Detect_Sec)
35	DAG0 (Address 0)	36	DAG2 (Address 2)
37	Chip Select 1P# [Chip Select 1S#]	38	Chip Select 3P# [Chip Select 3S#]
39	Activity#	40	Ground

Note: Signal names in brackets ([ ]) are for the secondary IDE connector.

2.8.4 External I/O Connectors

Figure 9 shows the locations of the external I/O connectors.



Item	Description	Reference Designator	For more information see:
A	SCSI hard drive activity LED	J7A1	Table 40
B	Front panel USB	J8B1	Table 41
C	Front panel	J9C1	Table 42
D	Auxiliary front panel power LED	J8C1	Table 45

Figure 9. External I/O Connectors

2.8.4.1 SCSI Hard Drive Activity LED Connector

The SCSI hard drive activity LED connector is a 1 x 2-pin connector that allows add-in SCSI controller to use the same LED as the IDE controller. This connector can be connected to the LED output of the add-in controller card. The LED will indicate when data is being read or written using the add-in controller. Table 40 lists the signal names of the SCSI hard drive activity LED connector.

Table 40. SCSI Hard Drive Activity LED Connector (J7A1)

Pin	Signal Name
1	SCSI activity
2	Not connected

2.8.4.2 Front Panel USB Connector

If the chassis has a USB connector in the front panel, the onboard connector at J8B1 can be cabled to it.

Table 41. Front Panel USB Connector (J8B1)

Pin	Signal Name	Pin	Signal Name
1	VREG_FP_USB_PWR	2	VREG_FP_USB_PWR
3	ICH_U_P2#	4	ICH_U_P3#
5	ICH_U_P2	6	ICH_U_P3
7	Ground	8	Ground
9	Key (no pin)	10	ICU_U_OC1_2#

2.8.4.3 Front Panel Connector

This section describes the functions of the front panel connector. Table 42 lists the signal names of the front panel connector.

Table 42. Front Panel Connector (J9C1)

Pin	Signal	In/Out	Description	Pin	Signal	In/Out	Description
1	HD_PWR	Out	Hard disk LED pull-up (330 Ω) to +5 V	2	HDR_BLNK_GRN	Out	Front panel green LED
3	HDA#	Out	Hard disk active LED	4	HDR_BLNK_YEL	Out	Front panel yellow LED
5	GND		Ground	6	FPBUT_IN	In	Power switch
7	FP_RESET#	In	Reset switch	8	GND		Ground
9	+5 V	Out	Power	10	N/C		Not connected
11	Reserved			12	GND		Ground
13	GND		Ground	14	(pin removed)		Not connected
15	Reserved			16	+5 V	Out	Power

2.8.4.3.1 Hard Drive Activity LED Connector

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. For the LED to function properly, an IDE drive must be connected to the onboard IDE interface. The LED will also show activity for devices connected to the SCSI hard drive activity LED connector.

For information about	Refer to
The SCSI hard drive activity LED connector	Section 2.8.4.1, page 66

2.8.4.3.2 Reset Switch Connector

Pins 5 and 7 can be connected to a momentary SPST type switch that is normally open. When the switch is closed, the D815BN board resets and runs the POST.

2.8.4.3.3 Power/Sleep/Message Waiting LED Connector

Pins 2 and 4 can be connected to a single- or dual-colored LED. Table 43 shows the possible states for a single-colored LED. Table 44 shows the possible states for a dual-colored LED.

Table 43. States for a Single-colored Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running
Blinking Green	Running/message waiting

Table 44. States for a Dual-colored Power LED

LED State	Description
Off	Power off
Steady Green	Running
Blinking Green	Running/message waiting
Steady Yellow	Sleeping
Blinking Yellow	Sleeping/message waiting

NOTE

To use the message waiting function, ACPI must be enabled in the operating system and a message-capturing application must be invoked.

2.8.4.3.4 Power Switch Connector

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. The time requirement is due to internal debounce circuitry on the D815BN board. At least two seconds must pass before the power supply will recognize another on/off signal.

2.8.4.4 Auxiliary Front Panel Power LED Connector

This connector duplicates the signals on pins 2 and 4 of the front panel connector.

Table 45. Auxiliary Front Panel Power LED Connector (J8C1)

Pin	Signal Name	In/Out	Description
1	HDR_BLNK_GRN	Out	Front panel green LED
2	No connect		
3	HDR_BLNK_YEL	Out	Front panel yellow LED

2.9 Jumper Block

CAUTION

Do not move any jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 10 shows the location of the jumper block. This 3-pin jumper block determines the BIOS Setup program's mode. Table 46 describes the jumper settings for the three modes: normal, configure, and recovery.

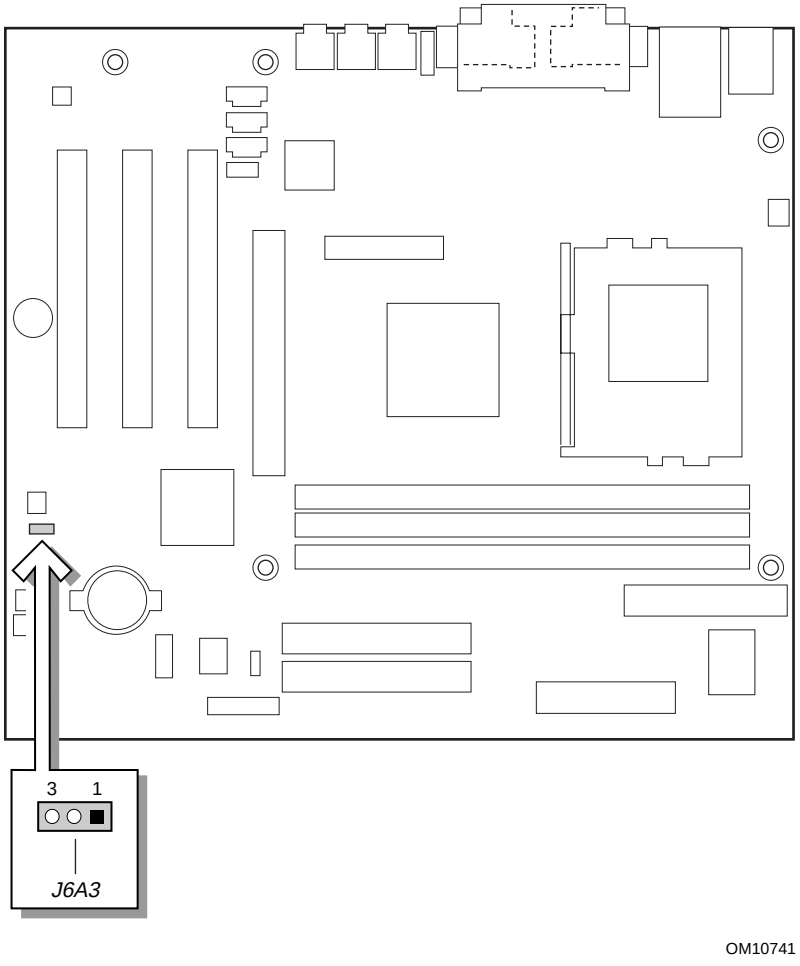
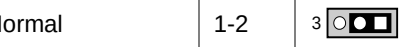
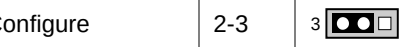


Figure 10. Location of the Jumper Block

Table 46. BIOS Setup Configuration Jumper Settings (J6A3)

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The Maintenance menu is displayed.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery diskette is required.

For information about	Refer to
How to access the BIOS Setup program	Section 4.1, page 91
The maintenance menu of the BIOS Setup program	Section 4.2, page 92
BIOS recovery	Section 3.7, page 87

2.10 Mechanical Considerations

2.10.1 Form Factor

The D815BN board is designed to fit into a microATX-form-factor chassis. Figure 11 illustrates the mechanical form factor for the D815BN board. Dimensions are given in inches [millimeters]. The outer dimensions are 9.60 inches by 8.50 inches [243.84 millimeters by 215.90 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the microATX specification (see Section 1.3).

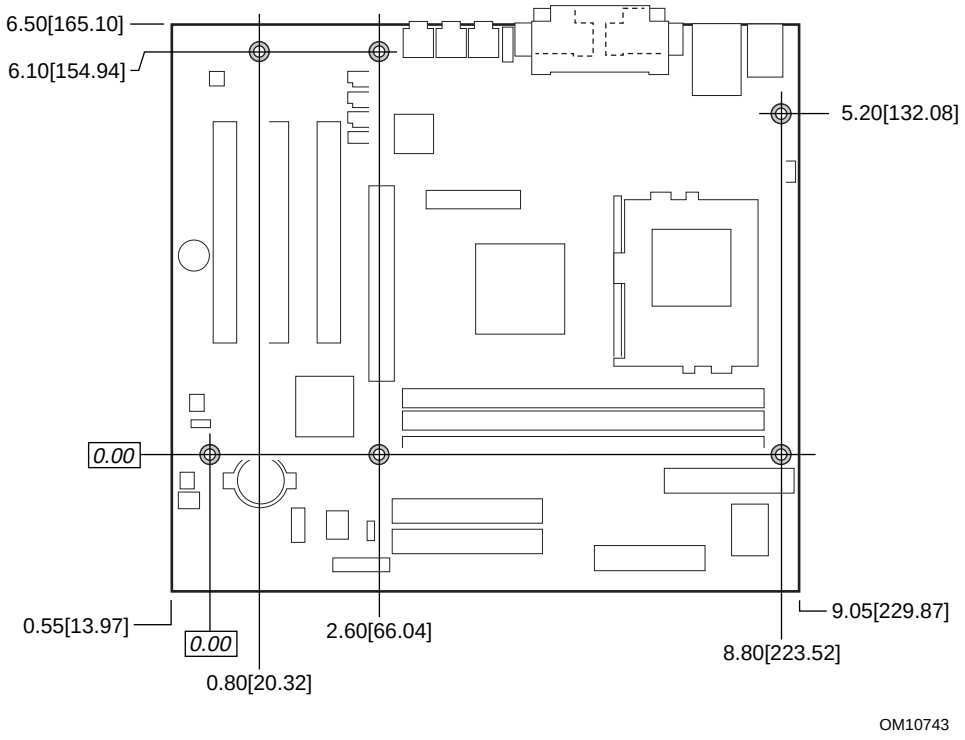


Figure 11. D815BN Board Dimensions

2.10.2 I/O Shield

The back panel I/O shield for the D815BN board must meet specific dimension and material requirements. Systems based on this board need the back panel I/O shield to pass certification testing. Figure 12 shows the critical dimensions of the chassis-dependent I/O shield. Dimensions are given in inches, to a tolerance of ±0.02 inches.

These figures also indicate the position of each cutout. Additional design considerations for I/O shields relative to chassis requirements are described in the microATX specification. See Section 1.3 on page 16 for information about the microATX specification.

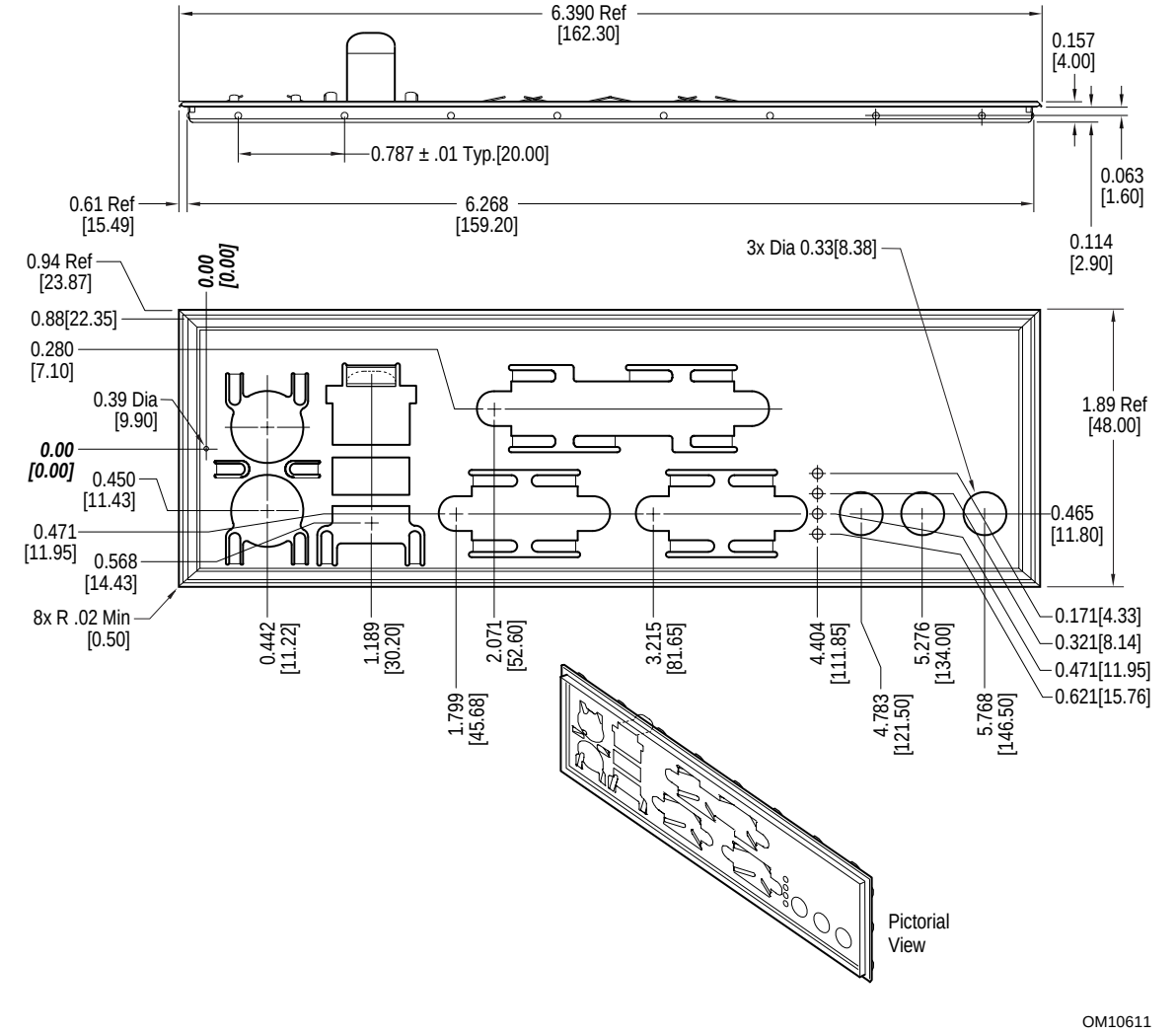


Figure 12. I/O Shield Dimensions

2.11 Electrical Considerations

2.11.1 Power Consumption

Table 47 lists voltage and current measurements for a computer that contains the D815BN board and the following:

- 667 MHz Intel Pentium III processor with a 512 KB cache
- 128 MB SDRAM
- 3.5-inch diskette drive
- 1.6 GB IDE hard disk drive
- 24X IDE CD-ROM drive

This information is provided only as a guide for calculating approximate power usage with additional resources added.

Values for the Windows 98 desktop mode are measured at 640 x 480 x 256 colors and 60 Hz refresh rate. AC watts are measured with the computer connected to a typical 200 W power supply, at nominal input voltage and frequency, with a true RMS wattmeter at the line input.

NOTE

Actual system power consumption depends upon system configuration. The power supply should comply with the recommendations found in the ATX Specification document (see Section 1.3, page 16 for specification information).

Table 47 lists the power usage for a D815BN board with the configuration listed above and including the audio subsystem and the onboard LAN subsystem.

Table 47. Power Usage For Board with Audio and Onboard LAN

		DC Current at:				
Mode	**AC Power**	**+3.3 V**	**+5 V**	**+12 V**	**-12 V**	**+5 VSB**
Windows 98 APM full on	48.8 W	1.72 A	2.03 A	0.012 A	0.036 A	0.08 A
Windows 98 APM Suspend	48.5 W	1.32 A	2.95 A	0.024 A	0.18 A	0.101 A
Windows 98 ACPI S0	35.6 W	1.7 A	0.5 A	0.053 A	0.196 A	0.56 A
Windows 98 ACPI S1	9.5 W	1.7 A	0.2 A	0.1 A	0.1 A	0.1 A
Windows 98 ACPI S3	3.5 W	0.1 A	0.1 A	0.1 A	0.1 A	0.1 A
Windows 98 ACPI Off	2.5 W	0.2 A	0 A	0.19 A	0.18 A	0.028 A

2.11.2 Add-in Board Considerations

The D815BN board is designed to provide 2 A (average) of +5 V current for each add-in board. The total +5 V current draw for add-in boards in a fully-loaded D815BN board (all four expansion slots filled) must not exceed 8 A.

2.11.3 Standby Current Requirements

⚠ CAUTION

Power supplies used with the board must provide enough standby current to support the Instantly Available (ACPI S3 sleep state) configuration. If the standby current necessary to support multiple wake events from the PCI and/or USB buses exceeds power supply capacity, the board may lose register settings stored in memory and may not awaken properly.

To estimate the standby current required for a specific system configuration, the standby current requirements of all installed components must be combined. Refer to Table 48 and follow these steps:

1. List the board's standby current requirement (767 mA).
2. List the PS/2 ports' standby current requirement (see note below).
3. List, from the AGP and PCI 2.2 slots (wake-enabled devices) row, the total number of wake-enabled devices installed and multiply by the standby current requirement.
4. List, from the AGP and PCI 2.2 slots (non-wake-enabled devices) row, the total number of wake-enabled devices installed and multiply by the standby current requirement.
5. List all additional wake-enabled devices' and non-wake-enabled devices' standby current requirements as applicable.
6. Add all the listed standby current totals from steps 1 through 5 to determine the total estimated standby current power supply requirement.

Table 48. Standby Current Requirements

Instantly Available Current Support Requirements	Description	Standby Current Requirements (mA)
Minimum	Total for the board	767
Optional	Onboard LAN (optional)	95
	PS/2 ports (Note)	345
	AGP and PCI 2.2 slots (wake-enabled devices) (Note)	375
	AGP and PCI 2.2 slots (non-wake-enabled devices) (Note)	20
	USB ports (Note)	517.5 (max)

Note: Dependent upon system configuration. See the note on the following page.

NOTE

AGP and PCI requirements are calculated by totaling the following:

- *One wake-enabled device @ 375 mA*
- *Five non-wake-enabled devices @ 20 mA each*

PS/2 Ports requirements per the IBM PS/2 Port Specification (Sept 1991):

- *Keyboard @ 275 mA (Actual measurements are 220 mA-300 mA, depending on the type of keyboard and the operational state of the keyboard's LEDs.)*
- *Mouse @ 70 mA*

USB requirements are calculated by totaling the following:

- *One wake-enabled device @ 500 mA*
- *Three USB non-wake-enabled devices @ 2.5 mA each*

The USB ports are limited to a combined total of 700 mA.

2.11.4 Fan Connector Current Capability

The D815BN board is designed to supply a maximum of 225 mA per fan connector.

2.11.5 Power Supply Considerations

⚠ CAUTION

The 5-V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options. Refer to Section 2.11.3 on page 74 for additional information.

System integrators should refer to the power usage values listed in Section 2.11.1, on page 73 when selecting a power supply for use with the D815BN board.

Measurements account only for current sourced by the D815BN board while running in idle modes of the started operating systems.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the following recommendations found in the indicated sections of the ATX form factor specification.

- The potential relation between 3.3 VDC and +5 VDC power rails (Section 4.2)
- The current capability of the +5 VSB line (Section 4.2.1.2)
- All timing parameters (Section 4.2.1.3)
- All voltage tolerances (Section 4.2.2)

For information about	Refer to
The ATX form factor specification	Section 1.3, page 16

2.12 Thermal Considerations

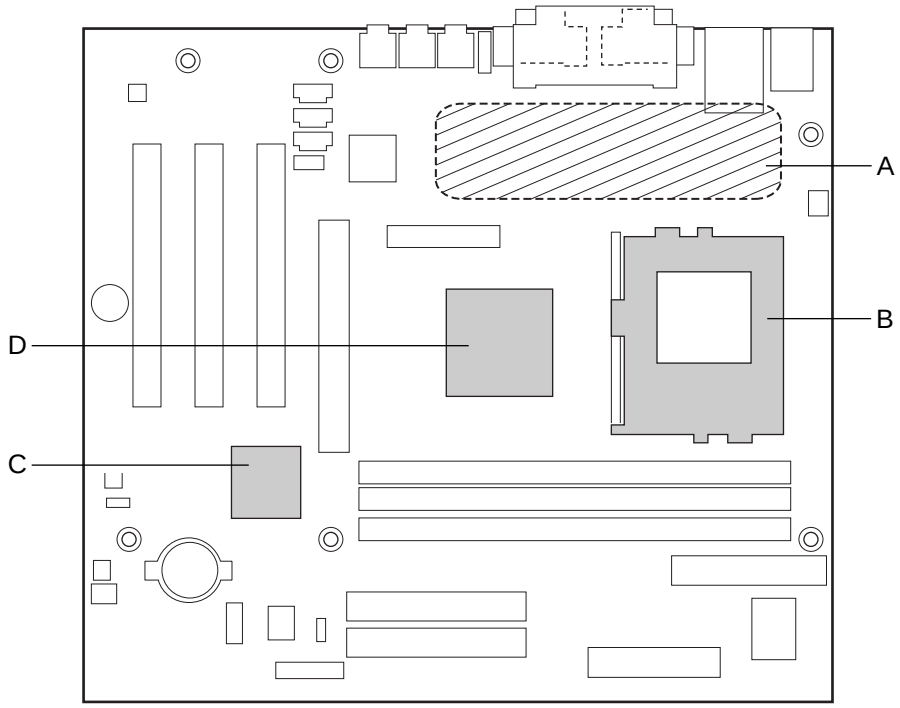
CAUTION

An ambient temperature that exceeds the board's maximum operating temperature by 5 °C to 10 °C could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 2.14.

CAUTION

The processor voltage regulator area (item A in Figure 13) can reach a temperature of up to 85 °C in an open chassis. System integrators should ensure that proper airflow is maintained in the voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit.

Figure 13 shows the locations of the localized high temperature zones.



A Processor voltage regulator area
B Processor
C Intel 82801AA ICH
D Intel 82815 GMCH

Figure 13. Localized High Temperature Zones

Table 49 provides maximum case temperatures for D815BN board components that are sensitive to thermal changes. Case temperatures could be affected by the operating temperature, current load, or operating frequency. Maximum case temperatures are important when considering proper airflow to cool the D815BN board.

Table 49. Thermal Considerations for Components

Component	Maximum Case Temperature
Intel Pentium III processor	For processor case temperature, see processor datasheets and processor specification updates
Intel Celeron processor	
Intel 82815 GMCH	116 °C (under bias)
Intel 82801AA ICH	109 °C (under bias)

For information about	Refer to
Intel Pentium III processor datasheets and specification updates	Section 1.2, page 16
Intel Celeron processor datasheets and specification updates	Section 1.2, page 16

2.13 Reliability

The mean time between failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Bellcore Reliability Prediction Procedure, TR-NWT-000332, Issue 4, September 1991. The MTBF prediction is used to estimate repair rates and spare parts requirements.

The Mean Time Between Failures (MTBF) data is calculated from predicted data at 35 ºC.

D815BN board MTBF: 417, 602 hours

2.14 Environmental

Table 50 lists the environmental specifications for the D815BN board.

Table 50. D815BN Board Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-40 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	30 g trapezoidal waveform		
	Velocity change of 170 inches/second		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/sec)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz : 0.01 g^2 Hz sloping up to 0.02 g^2 Hz		
	20 Hz to 500 Hz : 0.02 g^2 Hz (flat)		
Packaged	10 Hz to 40 Hz : 0.015 g^2 Hz (flat)		
	40 Hz to 500 Hz : 0.015 g^2 Hz sloping down to 0.00015 g^2 Hz		

2.15 Regulatory Compliance

This section describes the D815BN board's compliance with safety and EMC regulations.

2.15.1 Safety Regulations

Table 51 lists the safety regulations the D815BN board complies with when it is correctly installed in a compatible host system.

Table 51. Safety Regulations

Regulation	Title
UL 1950/CSA950, 3rd edition, Dated 07-28-95	Bi-National Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA and Canada)
EN 60950, 2nd Edition, 1992 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Community)
IEC 950, 2nd edition, 1991 (with Amendments 1, 2, 3, and 4)	The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)
EMKO-TSE (74-SEC) 207/94	Summary of Nordic deviations to EN 60950. (Norway, Sweden, Denmark, and Finland)

2.15.2 EMC Regulations

Table 52 lists the EMC regulations with which the D815BN board complies when it is correctly installed in a compatible host system.

Table 52. EMC Regulations

Regulation	Title
FCC Class B	Title 47 of the Code of Federal Regulations, Parts 2 and 15, Subpart B, pertaining to unintentional radiators. (USA)
CISPR 22, 2nd Edition, 1993 (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)
VCCI Class B (ITE)	Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)
EN55022 (1994) (Class B)	Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)
EN50082-1 (1992)	Generic Immunity Standard; currently compliance is determined via testing to IEC 801-2, -3, and -4. (Europe)
ICES-003 (1997)	Interference-Causing Equipment Standard, Digital Apparatus, Class B (Including CRC c.1374). (Canada)
AS/NZ 3548	Australian Communications Authority (ACA), Standard for Electromagnetic Compatibility.

2.15.3 Certification Markings

This printed circuit assembly has the following markings related to product certification:

- UL Joint Recognition Mark: Consists of small c followed by a stylized backward UR and followed by a small US (Component side).
- Manufacturer's recognition mark: Consists of a unique UL recognized manufacturer's logo, along with a flammability rating (94V-0). (Solder side)
- UL file number for D815BN boards: E210882 (Component side).
- PB part number: Intel bare circuit board part number (Solder side) A27603-003.
- Battery "+ Side Up" marking: Located in close proximity to the battery holder (Component side).
- FCC logo/declaration: (Solder side)
- ACA (C-Tick) mark: Consists of a unique letter C, with a tick mark; followed by N-232. Located on the component side of the D815BN board and on the shipping container.
- CE mark: (Component side) The CE mark should also be on the shipping container.

3 Overview of BIOS Features

What This Chapter Contains

3.1 Introduction

The D815BN board uses an Intel/AMI BIOS, which is stored in flash memory and can be updated using a disk-based program. In addition to the BIOS, the flash memory contains the BIOS Setup program, POST, APM, the PCI auto-configuration utility, and Plug and Play support.

The D815BN board supports system BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.

The BIOS displays a message during POST identifying the type of BIOS and a revision code. The initial production BIOS is identified as BN81510A.86A.

When the D815BN board jumper is set to configuration mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

For information about	Refer to
The D815BN board's compliance level with APM and Plug and Play	Section 1.3, page 16

3.2 BIOS Flash Memory Organization

The Intel 82802AB Firmware Hub (FWH) includes a 4 Mbit (512 KB) symmetrical flash memory device. Internally, the device is grouped into eight 64-KB blocks that are individually erasable, lockable, and unlockable.

3.3 Resource Configuration

3.3.1 PCI Autoconfiguration

The BIOS can automatically configure PCI devices. PCI devices may be onboard or add-in cards. Autoconfiguration lets a user insert or remove PCI cards without having to configure the system. When a user turns on the system after adding a PCI card, the BIOS automatically configures interrupts, the I/O space, and other system resources. Any interrupts set to Available in Setup are considered to be available for use by the add-in card.

For information about the versions of PCI and Plug and Play supported by the BIOS, see Section 1.3.

3.3.2 PCI IDE Support

If you select Auto in the BIOS Setup program, the BIOS automatically sets up the two PCI IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to Ultra ATA-66 and recognizes any ATAPI devices, including CD-ROM drives, tape drives, and Ultra DMA drives (see Section 1.3 for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying manual configuration in the BIOS Setup program.

To use Ultra ATA-66 features the following items are required:

- An Ultra ATA-66 peripheral device
- An Ultra ATA-66 compatible cable
- Ultra ATA-66 operating system device drivers

NOTES

Ultra ATA-66 compatible cables are backward compatible with drives using slower IDE transfer protocols. If an Ultra ATA-66 disk drive and a disk drive using any other IDE transfer protocol are attached to the same cable, the maximum transfer rate between the drives is 33 MB/sec.

Do not connect an ATA device as a slave on the same IDE cable as an ATAPI master device. For example, do not connect an ATA hard drive as a slave to an ATAPI CD-ROM drive.

3.4 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the management information format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party client manager software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems, such as Windows NT, require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information.

For information about	Refer to
The D815BN board's compliance level with SMBIOS	Section 1.3, page 16

3.5 USB Legacy Support

USB legacy support enables USB devices such as keyboards, mice, and hubs to be used even when the operating system's USB drivers are not yet available. USB legacy support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, USB legacy support is set to Enabled.

USB legacy support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. USB legacy support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.
5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if USB legacy support was set to Disabled in the BIOS Setup program.)
6. recognized by the operating system, and USB legacy support from the BIOS is no longer used.

To install an operating system that supports USB, verify that USB Legacy support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

NOTE

USB legacy support is for keyboards, mice, and hubs only. Other USB devices are not supported.

3.6 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel World Wide Web site:

- Intel® Express BIOS Update utility, which enables automated updating while in the Windows environment. Using this utility, the BIOS can be updated from a file on a hard disk, a 1.44 MB diskette, or a CD-ROM, or from the file location on the Web.
- Intel® Flash Memory Update Utility, which requires creation of a boot diskette and manual rebooting of the system. Using this utility, the BIOS can be updated from a file on a 1.44 MB diskette (from a legacy diskette drive or an LS-120 diskette drive) or a CD-ROM.

Both utilities support the following BIOS maintenance functions:

- Verifying that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.
- Updating both the BIOS boot block and the main BIOS. This process is fault tolerant to prevent boot block corruption.
- Updating the BIOS boot block separately.
- Changing the language section of the BIOS.
- Updating replaceable BIOS modules, such as the video BIOS module.
- Inserting a custom splash screen.

NOTE

Review the instructions distributed with the update utility before attempting a BIOS update.

For information about	Refer to
The Intel World Wide Web site	Section 1.2, page 16

3.6.1 Language Support

The BIOS Setup program and help messages are supported in five languages: US English, German, Italian, French, and Spanish. The default language is US English, which is present unless another language is selected in the BIOS Setup program. Although five languages are supported, only three language options are available in Setup at a time. To change the language options in Setup, update the BIOS languages using the BIOS update utility.

3.6.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be replaced with a custom splash screen. A utility is available from Intel to assist with creating a custom splash screen. The custom splash screen can be programmed into the flash memory using the BIOS update utility. Information about this capability is available on the Intel Support World Wide Web site. See Section 1.2 for more information about this site.

3.7 Recovering BIOS Data

Some types of failure can destroy the BIOS. For example, the data can be lost if a power outage occurs while the BIOS is being updated in flash memory. The BIOS can be recovered from a diskette using the BIOS recovery mode. When recovering the BIOS, be aware of the following:

- Because of the small amount of code available in the non-erasable boot block area, there is no video support. You can only monitor this procedure by listening to the speaker or looking at the diskette drive LED.
- The recovery process may take several minutes; larger BIOS flash memory devices require more time.
- Two beeps and the end of activity in the diskette drive indicate successful BIOS recovery.
- A series of continuous beeps indicates a failed BIOS recovery.

To create a BIOS recovery diskette, a bootable diskette must be created and the BIOS update files copied to it. BIOS upgrades and the Intel Flash Memory Upgrade Utility are available from Intel Customer Support through the Intel World Wide Web site.

NOTE

If the computer is configured to boot from an LS-120 diskette (in the Setup program's Removable Devices submenu), the BIOS recovery diskette must be a standard 1.44 MB diskette not a 120 MB diskette.

For information about	Refer to
The BIOS recovery mode jumper settings	Table 46, page 70
The Boot menu in the BIOS Setup program	Section 4.7, page 108
Contacting Intel customer support	Section 1.2, page 16

3.8 Boot Options

In the BIOS Setup program, the user can choose to boot from a diskette drive, hard drives, CD-ROM, or the network. The default setting is for the diskette drive to be the first boot device, the hard drive second, and the ATAPI CD-ROM third. The fourth device is disabled.

3.8.1 CD-ROM and Network Boot

Booting from CD-ROM is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, ATAPI CD-ROM is listed as a boot device. Boot devices are defined in priority order. If the CD-ROM is selected as the boot device, it must be the first device with bootable media.

The network can be selected as a boot device. This selection allows booting from the onboard LAN device or a network add-in card with a remote boot ROM installed.

For information about	Refer to
The El Torito specification	Section 1.3, page 16

3.8.2 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

3.9 Fast Booting Systems with Intel® Rapid BIOS Boot

Three factors affect system boot speed:

- Peripheral selection and configuration
- Use of an optimized BIOS, such as the Intel® Rapid BIOS
- Selection of a compatible operating system

3.9.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters, such as “power-up to data ready" of less than eight seconds, that minimize hard drive startup delays.
- Select a CD-ROM drive with a fast initialization rate. This rate can influence the POST execution time.
- Eliminate unnecessary add-in adapter features , such as logo displays, screen repaints, or mode changes in the POST. These features may add time to the boot process.
- Try using different monitors. Some monitors initialize and communicate with BIOS more quickly, which enables the system to boot more quickly.

3.9.2 BIOS Settings

Use of the following BIOS Setup program settings reduces the POST execution time.

In the Boot menu:

- Set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- Disable Quiet Boot, which eliminates display of the logo splash screen. This could save several seconds of painting complex graphic images and changing video modes.
- Enable Intel Rapid BIOS Boot. This feature bypasses the memory count and the search for a diskette drive.

In the Peripheral Configuration submenu, disable LAN Device if it will not be used. This can reduce up to four seconds of option ROM boot time.

NOTES

It is possible to optimize the boot process to the point where the system boots so quickly that the Intel logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen. If this should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds using the Hard Disk Pre-Delay feature in the IDE Configuration Submenu of the BIOS Setup Program.

The boot time may be so fast that some drives might not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from 3 to 30 seconds (using the Hard Disk Pre-Delay feature of the Advanced menu in the IDE Configuration Submenu of the BIOS Setup Program).

For information about	Refer to
IDE Configuration Submenu in the BIOS Setup Program	Table 61, page 94

3.9.3 Operating System

The Microsoft Windows Millennium Edition (Windows Me) operating system has built-in capabilities for making PCs boot more quickly.

To speed operating system availability at boot time, limit the number of applications that load into the system tray or the task bar.

3.10 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.

Table 53 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 53. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

For information about	Refer to
Setting user and supervisor passwords	Section 4.5, page 106

4 BIOS Setup Program

What This Chapter Contains

4.1 Introduction

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the POST memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	Main	Advanced	Security	Power	Boot	Exit

Table 54 lists the BIOS Setup program menu features.

Table 54. BIOS Setup Program Menu Bar

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Clears passwords and Boot Integrity Services (BIS)* credentials, and enables extended configuration mode	Allocates resources for hardware components	Configures advanced features available through the chipset	Sets passwords and security features	Configures power management features	Selects boot options and power supply controls	Saves or discards changes to Setup program options

* For information about BIS, refer to the Intel Web site at:

http://developer.intel.com/design/security/index1.htm

NOTE

In this chapter, all examples of the BIOS Setup Program menu bar include the maintenance menu; however, the maintenance menu is displayed only when the board is in configuration mode. Section 2.9 on page 69 tells how to put the board in configuration mode.

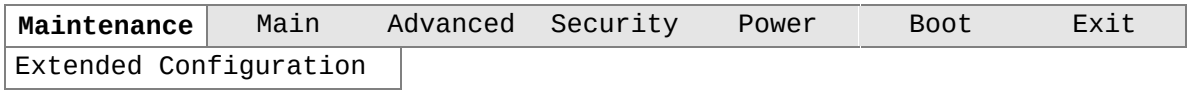
Table 55 lists the function keys available for menu screens.

Table 55. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 Maintenance Menu

To access this menu, select Maintenance on the menu bar at the top of the screen.



The menu shown in Table 56 is for clearing Setup passwords and enabling extended configuration mode. Setup only displays this menu in configuration mode. See Section 2.9 on page 69 for configuration mode setting information.

Table 56. Maintenance Menu

Feature	Options	Description
Clear All Passwords	No options	Clears the user and administrative passwords.
Clear BIS Credentials	No options	Clears the Wired for Management BIS* credentials.
Extended Configuration	• **Default (default)** • User-Defined	Invokes the Extended Configuration submenu.
CPU Microcode Update Revision	No options	Displays the CPU microcode update revision.
CPU Stepping Signature	No options	Displays the CPU stepping signature.

* For information about BIS, refer to the Intel Web site at:

http://developer.intel.com/design/security/index1.htm

4.2.1 Extended Configuration Submenu

To access this submenu, select Maintenance on the menu bar, then Extended Configuration.

Maintenance	Main	Advanced	Security	Power	Boot	Exit
Extended Configuration						

The submenu represented by Table 57 is for setting video memory cache mode. This submenu becomes available when User Defined is selected under Extended Configuration.

Table 57. Extended Configuration Submenu

Feature	Options	Description
Extended Configuration	• **Default (default)** • User-Defined	*User Defined* allows setting memory control and video memory cache mode. If selected here, will also display in the Advanced Menu as: "Extended Menu: *Used*."
Video Memory Cache Mode	• USWC • **UC (default)**	Selects Uncacheable Speculative Write-Combining (USWC) video memory cache mode. Full 32 byte contents of the Write Combining buffer are written to memory as required. Cache lookups are not performed. Both the video driver and the application must support Write Combining. Selects UnCacheable (UC) video memory cache mode. This setting identifies the video memory range as uncacheable by the processor. Memory writes are performed in program order. Cache lookups are not performed. Well suited for applications not supporting Write Combining.
SDRAM Auto-configuration (Note 1)	• **Auto (default)** • User Defined	Sets extended memory configuration options to auto or user defined.
CAS# Latency (Note 2)	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles required to address a column in memory.
SDRAM RAS# to CAS# Delay (Note 2)	• 3 • 2 • **Auto (default)**	Selects the number of clock cycles between addressing a row and addressing a column.
SDRAM RAS# Precharge (Note 2)	• 3 • 2 • **Auto (default)**	Selects the length of time required before accessing a new row.

Notes:

1. These options can only be set if Extended Configuration is set to *User Defined*.
2. These options can only be set if SDRAM Auto-configuration is set to *User Defined*.

4.3 Main Menu

To access this menu, select Main on the menu bar at the top of the screen.

Maintenance	**Main**	Advanced	Security	Power	Boot	Exit

Table 58 describes the Main Menu. This menu reports processor and memory information and is for configuring the system date and system time.

Table 58. Main Menu

Feature	Options	Description
BIOS Version	No options	Displays the version of the BIOS.
Processor Type	No options	Displays processor type.
Processor Speed	No options	Displays processor speed in MHz.
System Bus Frequency	No options	Displays the system bus frequency.
Cache RAM	No options	Displays the size of second-level cache and whether it is ECC-capable.
Total Memory	No options	Displays the total amount of RAM.
Memory Bank 0 Memory Bank 1 Memory Bank 2	No options	Displays the amount and type of RAM in the memory banks.
Language	• **English (default)** • Español • Deutsch	Selects the current default language used by the BIOS. For other language options, see Language Support page 86.
Processor Serial Number	• **Disabled (default)** • Enabled	Enables and disables the processor serial number. (Present only when a Pentium III processor is installed.)
System Time	Hour, minute, and second	Specifies the current time.
System Date	Day of week Month/day/year	Specifies the current date.

4.4 Advanced Menu

To access this menu, select Advanced on the menu bar at the top of the screen.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

Table 59 describes the Advanced Menu. This menu is used for setting advanced features that are available through the chipset.

Table 59. Advanced Menu

Feature	Options	Description
Extended Configuration	No options	If *Used* is displayed, *User Defined* has been selected in Extended Configuration under the Maintenance menu.
PCI Configuration	No options	Configures individual PCI slot's IRQ priority. When selected, displays the PCI Configuration submenu.
Boot Settings Configuration	No options	Configures Plug and Play and the Numlock key, and resets configuration data. When selected, displays the Boot Configuration submenu.
Peripheral Configuration	No options	Configures peripheral ports and devices. When selected, displays the Peripheral Configuration submenu.
IDE Configuration	No options	Specifies type of connected IDE device.
Diskette Configuration	No options	When selected, displays the Diskette Configuration submenu.
Event Log Configuration	No options	Configures Event Logging. When selected, displays the Event Log Configuration submenu.
Video Configuration	No options	Configures video features. When selected, displays the Video Configuration submenu.

4.4.1 PCI Configuration Submenu

To access this submenu, select Advanced on the menu bar, then PCI Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 60 is for configuring the IRQ priority of PCI slots individually.

Table 60. PCI Configuration Submenu

Feature	Options	Description
PCI Slot 1 IRQ Priority	• **Auto (default)** • 3 • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot 2 IRQ Priority	• **Auto (default)** • 3 • 9 • 10 • 11	Allows selection of IRQ priority.
PCI Slot 3 IRQ Priority	• **Auto (default)** • 3 • 9 • 10 • 11	Allows selection of IRQ priority. IRQ Priority selections for PCI slots 3 and 5 are linked. Selections made to PCI Slot 3 IRQ Priority are repeated in PCI Slot 5 IRQ Priority.

4.4.2 Boot Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Boot Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 61 is for setting Plug and Play options, resetting configuration data, and the power-on state of the Numlock key.

Table 61. Boot Configuration Submenu

Feature	Options	Description
Plug & Play O/S	• **No (default)** • Yes	Specifies if manual configuration is desired. *No* lets the BIOS configure all devices. This setting is appropriate when using a Plug and Play operating system. *Yes* lets the operating system configure Plug and Play devices not required to boot the system. This option is available for use during lab testing.
Reset Config Data	• **No (default)** • Yes	*No* does not clear the PCI/PnP configuration data stored in flash memory on the next boot. *Yes* clears the PCI/PnP configuration data stored in flash memory on the next boot.
Numlock	• Off • **On (default)**	Specifies the power-on state of the Numlock feature on the numeric keypad of the keyboard.

4.4.3 Peripheral Configuration Submenu

To access this submenu, select Advanced on the menu bar, then Peripheral Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 62 is used for configuring computer peripherals.

Table 62. Peripheral Configuration Submenu

Feature	Options	Description
Serial Port A	• Disabled • Enabled • **Auto (default)**	Configures the serial port. *Auto* assigns the first free COM port, normally COM1, the address 3F8h, and the interrupt IRQ4. An * (asterisk) displayed next to an address indicates a conflict with another device.
Base I/O Address (This feature is present only when Serial Port A is set to *Enabled*)	• **3F8 (default)** • 2F8 • 3E8 • 2E8	Specifies the base I/O address for the serial port, if Serial Port A is set to *Enabled*.
Interrupt (This feature is present only when Serial Port A is set to *Enabled*)	• IRQ 3 • **IRQ 4 (default)**	Specifies the interrupt for the serial port, if Serial Port A is set to *Enabled*.

continued

Table 62. Peripheral Configuration Submenu (continued)

Feature	Options	Description
Parallel port	• Disabled • Enabled • **Auto (default)**	Configures the parallel port. *Auto* assigns LPT1 the address 378h and the interrupt IRQ7. An * (asterisk) displayed next to an address indicates a conflict with another device.
Mode	• Output Only • **Bi-directional (default)** • EPP • ECP	Selects the mode for the parallel port. Not available if the parallel port is disabled. *Output Only* operates in AT†-compatible mode. *Bi-directional* operates in PS/2-compatible mode. *EPP* is Extended Parallel Port mode, a high-speed bi-directional mode. *ECP* is Enhanced Capabilities Port mode, a high-speed bi-directional mode.
Base I/O address (This feature is present only when Parallel Port is set to *Enabled*)	• **378 (default)** • 278	Specifies the base I/O address for the parallel port.
Interrupt (This feature is present only when Parallel Port is set to *Enabled*)	• IRQ 5 • **IRQ 7 (default)**	Specifies the interrupt for the parallel port.
DMA Channel (This feature is present only when Parallel Port Mode is set to *ECP*)	• 1 • **3 (default)**	Specifies the DMA channel.
Audio Device	• Disabled • **Enabled (default)**	Enables or disables the onboard audio subsystem.
LAN Device	• Disabled • **Enabled (default)**	Enables or disables the LAN device.
Legacy USB Support	• Disabled • **Enabled (default)**	Enables or disables USB legacy support. (See Section 3.5 on page 85 for more information.)

4.4.4 IDE Configuration Submenu

To access this submenu, select Advanced on the menu bar, then IDE Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The menu represented in Table 63 is used to configure IDE device options.

Table 63. IDE Configuration Submenu

Feature	Options	Description
IDE Controller	• Disabled • Primary • Secondary • **Both (default)**	Specifies the integrated IDE controller. *Primary* enables only the primary IDE controller. *Secondary* enables only the secondary IDE controller. *Both* enables both IDE controllers.
Hard Disk Pre-Delay	• **Disabled (default)** • 3 Seconds • 6 Seconds • 9 Seconds • 12 Seconds • 15 Seconds • 21 Seconds • 30 Seconds	Specifies the hard disk drive pre-delay.
Primary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Master submenu.
Primary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Primary IDE Slave submenu.
Secondary IDE Master	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Master submenu.
Secondary IDE Slave	No options	Reports type of connected IDE device. When selected, displays the Secondary IDE Slave submenu.

4.4.4.1 Primary/Secondary IDE Master/Slave Submenus

To access these submenus, select Advanced on the menu bar, then IDE Configuration and then the master or slave to be configured.

Maintenance Main	**Advanced**	Security Power	Boot Exit
	PCI Configuration		
	Boot Configuration		
	Peripheral Configuration		
	IDE Configuration **Primary IDE Master** **Primary IDE Slave** **Secondary IDE Master** **Secondary IDE Slave**		
	Diskette Configuration		
	Event Log Configuration		
	Video Configuration		

There are four IDE submenus: primary master, primary slave, secondary master, and secondary slave. Table 64 shows the format of the IDE submenus. For brevity, only one example is shown.

Table 64. Primary/Secondary IDE Master/Slave Submenus

Feature	Options	Description
Drive Installed	No options	Displays the type of drive installed.
Type	• None • User • **Auto (default)** • CD-ROM • ATAPI Removable • Other ATAPI • IDE Removable	Specifies the IDE configuration mode for IDE devices. *User* allows capabilities to be changed. *Auto* fills-in capabilities from ATA/ATAPI device.
Maximum Capacity	No options	Displays the capacity of the drive.
LBA Mode Control	• Disabled • **Enabled (default)**	Enables or disables LBA mode control.
Multi-sector Transfers	• Disabled • 2 Sectors • 4 Sectors • 8 Sectors • **16 Sectors (default)**	Specifies number of sectors per block for transfers from the hard disk drive to memory. Check the hard disk drive's specifications for optimum setting.

continued

Table 64. Primary/Secondary IDE Master/Slave Submenus (continued)

Feature	Options	Description
PIO Mode	• **Auto (default)** • 0 • 1 • 2 • 3 • 4	Specifies the PIO mode.
Ultra DMA	• **Disabled (default)** • Mode 0 • Mode 1 • Mode 2 • Mode 3 • Mode 4 • Mode 5	Specifies the Ultra DMA mode for the drive.
Cable Detected	No options	Displays the type of cable connected to the IDE interface: 40-conductor or 80-conductor (for Ultra ATA-66 devices).

4.4.5 Diskette Configuration Submenu

To access this menu, select Advanced on the menu bar, then Diskette Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 65 is used for configuring the diskette drive.

Table 65. Diskette Configuration Submenu

Feature	Options	Description
Diskette Controller	• Disabled • **Enabled (default)**	Disables or enables the integrated diskette controller.
Floppy A	• Not Installed • 360 KB 5¼" • 1.2 MB 5¼" • 720 KB 3½" • **1.44/1.25 MB 3½" (default)** • 2.88 MB 3½"	Specifies the capacity and physical size of diskette drive A.
Diskette Write Protect	• **Disabled (default)** • Enabled	Disables or enables write-protect for the diskette drive.

4.4.6 Event Log Configuration Submenu

To access this menu, select Advanced on the menu bar, then Event Log Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented by Table 66 is used to configure the event logging features.

Table 66. Event Log Configuration Submenu

Feature	Options	Description
Event Log	No options	Indicates if there is space available in the event log.
Event Log Validity	No options	Indicates if the contents of the event log are valid.
View Event Log	[Enter]	Displays the event log.
Clear All Event Logs	• **No (default)** • Yes	Clears the event log after rebooting.
Event Logging	• Disabled • **Enabled (default)**	Enables logging of events.
Mark Events as Read	[Enter]	Marks all events as read.

4.4.7 Video Configuration Submenu

To access this menu, select Advanced on the menu bar, then Video Configuration.

Maintenance	Main	**Advanced**	Security	Power	Boot	Exit

PCI Configuration
Boot Configuration
Peripheral Configuration
IDE Configuration
Diskette Configuration
Event Log Configuration
Video Configuration

The submenu represented in Table 67 is for configuring the video features.

Table 67. Video Configuration Submenu

Feature	Options	Description
Primary Video Adapter	• **AGP (default)** • PCI	Selects primary video adapter to be used during boot.
AGP Hardware Detected	No options	Specifies whether the integrated video solution or an add-in AGP card is in use. Displays the mode of the add-in AGP video card.

4.5 Security Menu

To access this menu, select Security from the menu bar at the top of the screen.

Maintenance	Main	Advanced	**Security**	Power	Boot	Exit

The menu represented by Table 68 is for setting passwords and security features.

Table 68. Security Menu

If no password entered previously:		
Feature	**Options**	**Description**
Supervisor Password Is	No options	Reports if there is a supervisor password set.
User Password Is	No options	Reports if there is a user password set.
Set Supervisor Password	Password can be up to seven alphanumeric characters.	Specifies the supervisor password.
Set User Password	Password can be up to seven alphanumeric characters.	Specifies the user password.
Clear User Password (Note 1)	• **Yes (default)** • No	Clears the user password.
User Access Level (Note 2)	• Limited • No Access • View Only • **Full (default)**	Sets the user's BIOS Setup Utility access rights. *Limited* allows the user to change only certain fields. *No Access* prevents the user from accessing BIOS Setup. *View Only* allows the user to view but not change BIOS Setup. *Full* allows the user to change any field except the supervisor password.
Unattended Start (Note 1)	• Enabled • **Disabled (default)**	Enabled allows system to complete the boot process without a password. The keyboard remains locked until a password is entered. A password is required to boot from a diskette.

Notes:

1. This feature appears only if a user password has been set.
2. This feature appears only if a supervisor password have been set.

4.6 Power Menu

To access this menu, select Power from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	**Power**	Boot	Exit

The menu represented in Table 69 is for setting the power management features.

Table 69. Power Menu

Feature	Options	Description
Power Management	• Disabled • **Enabled (default)**	Enables or disables the BIOS power management feature.
Inactivity Timer	• Off • 1 Minute • 5 Minutes • 10 Minutes • **20 Minutes (default)** • 30 Minutes • 60 Minutes • 120 Minutes	Specifies the amount of time before the computer enters standby mode.
Hard Drive	• Disabled • **Enabled (default)**	Enables power management for hard disks during standby modes.
ACPI Suspend State	• **S1 State (default)** • S3 State	Specifies the ACPI suspend state.
Video Repost	• **Disabled (default)** • Enabled	Allows the video BIOS to be initialized coming out of the S3 state. Some video controllers require this option to be enabled. This feature is present only when the ACPI suspend state is set to S3.

4.7 Boot Menu

To access this menu, select Boot from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The menu represented in Table 70 is used to set the boot features and the boot sequence.

Table 70. Boot Menu

Feature	Options	Description
Quiet Boot	• Disabled • **Enabled (default)**	*Disabled* displays normal POST messages. *Enabled* displays OEM graphic instead of POST messages.
Intel Rapid BIOS Boot	• Disabled • **Enabled (default)**	Enables the computer to boot without running certain POST tests.
Scan User Flash Area	• **Disabled (default)** • Enabled	Enables the BIOS to scan the flash memory for user binary files that are executed at boot time.
After Power Failure	• Stay Off • **Last State (default)** • Power On	Specifies the mode of operation if an AC power loss occurs. *Power On* restores power to the computer. *Stay Off* keeps the power off until the power button is pressed. *Last State* restores the previous power state before power loss occurred.
On Modem Ring	• **Stay Off (default)** • Power-On	In APM mode only, specifies how the computer responds to an incoming call on an installed modem when the power is off.
On LAN	• Stay Off • **Power-On (default)**	In APM mode only, determines how the system responds to a LAN wake up event.
On PME	• **Stay Off (default)** • Power-On	In APM mode only, determines how the system responds to a PCI power management event.
On ACPI S5	• **Stay Off (default)** • Power-On	IN ACPI mode only, determines the action of the system when a LAN wake up event occurs.

continued

Table 70. Boot Menu (continued)

Feature	Options	Description
1st Boot Device 2nd Boot Device 3rd Boot Device 4th Boot Device	• Floppy • ARMD-FDD (Note 1) • ARMD-HDD (Note 2) • IDE-HDD (Note 3) • ATAPI CDROM • Disabled	Specifies the boot sequence from the available devices. To specify boot sequence: 1. Select the boot device with <↑> or <↓>. 2. Press <Enter> to set the selection as the intended boot device. The operating system assigns a drive letter to each boot device in the order listed. Changing the order of the devices changes the drive lettering. The default settings for the first through fourth boot devices are, respectively: • Floppy • IDE-HDD • ATAPI CDROM • Disabled
IDE Drive Configuration	No Options	Configures IDE drives. When selected, displays the IDE Drive Configuration submenu.

Notes:

1 ARMD-FDD = ATAPI removable device - floppy disk drive

2 ARMD-HDD = ATAPI removable device - hard disk drive

3 HDD = Hard Disk Drive

4.7.1 IDE Drive Configuration Submenu

Maintenance	Main	Advanced	Security	Power	**Boot**	Exit
					IDE Drive Configuration	

The submenu represented in Table 71 is used to set the order in which the IDE drives boot. Changing the boot-order of a given drive causes the boot-order for the other drives to change automatically to accommodate your selection.

Table 71. IDE Drive Configuration Submenu

Feature	Options	Description
Primary Master IDE	**1st IDE (default)** 1 through 4	Allows you to select the order in which the Primary Master IDE drive boots.
Primary Slave IDE	**2nd IDE (default)** 1 through 4	Allows you to select the order in which the Primary Slave IDE drive boots.
Secondary Master IDE	**3rd IDE (default)** 1 through 4	Allows you to select the order in which the Secondary Master IDE drive boots.
Secondary Slave IDE	**4th IDE (default)** 1 through 4	Allows you to select the order in which the Secondary Slave IDE drive boots.

4.8 Exit Menu

To access this menu, select Exit from the menu bar at the top of the screen.

Maintenance	Main	Advanced	Security	Power	Boot	**Exit**

The menu represented in Table 72 is for exiting the BIOS Setup program, saving changes, and loading and saving defaults.

Table 72. Exit Menu

Feature	Description
Exit Saving Changes	Exits and saves the changes in CMOS SRAM.
Exit Discarding Changes	Exits without saving any changes made in the BIOS Setup program.
Load Setup Defaults	Loads the factory default values for all the Setup options.
Load Custom Defaults	Loads the custom defaults for Setup options.
Save Custom Defaults	Saves the current values as custom defaults. Normally, the BIOS reads the Setup values from flash memory. If this memory is corrupted, the BIOS reads the custom defaults. If no custom defaults are set, the BIOS reads the factory defaults.
Discard Changes	Discards changes without exiting Setup. The option values present when the computer was turned on are used.

5 Error Messages and Beep Codes

What This Chapter Contains

5.1 BIOS Error Messages

Table 73 lists the error messages and provides a brief description of each.

Table 73. BIOS Error Messages

Error Message	Explanation
GA20 Error	An error occurred with Gate A20 when switching to protected mode during the memory test.
Pri Master HDD Error Pri Slave HDD Error Sec Master HDD Error Sec Slave HDD Error	Could not read sector from corresponding drive.
Pri Master Drive - ATAPI Incompatible Pri Slave Drive - ATAPI Incompatible Sec Master Drive - ATAPI Incompatible Sec Slave Drive - ATAPI Incompatible	Corresponding drive in not an ATAPI device. Run Setup to make sure device is selected correctly.
A: Drive Error (Note)	No response from diskette drive.
Cache Memory Bad	An error occurred when testing L2 cache. Cache memory may be bad.
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Display Type Wrong	The display type is different than what has been stored in CMOS. Check Setup to make sure type is correct.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
CMOS Settings Wrong	CMOS values are not the same as the last boot. These values have either been corrupted or the battery has failed.
CMOS Date/Time Not Set	The time and/or date values stored in CMOS are invalid. Run Setup to set correct values.
DMA Error	Error during read/write test of DMA controller.
FDC Failure	Error occurred trying to access diskette drive controller.

continued

Note: Drive A is not checked if Intel Rapid BIOS Boot is enabled.

Table 73. BIOS Error Messages (continued)

Error Message	Explanation
HDC Failure	Error occurred trying to access hard disk controller.
Checking NVRAM.....	NVRAM is being checked to see if it is valid.
Update OK!	NVRAM was invalid and has been updated.
Updated Failed	NVRAM was invalid but was unable to be updated.
Keyboard Error	Error in the keyboard connection. Make sure keyboard is connected properly.
KB/Interface Error	Keyboard interface test failed.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed then memory may be bad.
Memory Size Increased	Memory size has increased since the last boot. If no memory was added there may be a problem with the system.
Memory Size Changed	Memory size has changed since the last boot. If no memory was added or removed then memory may be bad.
No Boot Device Available	System did not find a device to boot.
Off Board Parity Error	A parity error occurred on an off-board card. This error is followed by an address.
On Board Parity Error	A parity error occurred in onboard memory. This error is followed by an address.
Parity Error	A parity error occurred in onboard memory at an unknown address.
NVRAM/CMOS/PASSWORD Cleared by Jumper	NVRAM, CMOS, and passwords have been cleared. The system should be powered down and the jumper removed.
<CTRL_N> Pressed	CMOS is ignored and NVRAM is cleared. User must enter Setup.

5.2 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST-codes requires an add-in card, often called a POST card (PCI not ISA). The POST card can decode the port and display the contents on a medium such as a seven-segment display.

The tables below offer descriptions of the POST codes generated by the BIOS. Table 74 defines the Uncompressed INIT Code Checkpoints, Table 75 describes the Boot Block Recovery Code Checkpoints, and Table 76 lists the Runtime Code Uncompressed in F000 Shadow RAM. Some codes are repeated in the tables because that code applies to more than one operation.

Table 74. Uncompressed INIT Code Checkpoints

Code	Description of POST Operation
D0	NMI is disabled. Onboard KBC, RTC enabled (if present). Init code checksum verification starting.
D1	Keyboard controller BAT test, CPU ID saved, and going to 4 GB flat mode.
D3	Do necessary chipset initialization, start memory refresh, and do memory sizing.
D4	Verify base memory.
D5	Init code to be copied to segment 0 and control to be transferred to segment 0.
D6	Control is in segment 0. To check recovery mode and verify main BIOS checksum. If either it is recovery mode or main BIOS checksum is bad, go to check point E0 for recovery else go to check point D7 for giving control to main BIOS.
D7	Find main BIOS module in ROM image.
D8	Uncompress the main BIOS module.
D9	Copy main BIOS image to F000 shadow RAM and give control to main BIOS in F000 shadow RAM.

Table 75. Boot Block Recovery Code Checkpoints

Code	Description of POST Operation
E0	Onboard floppy controller (if any) is initialized. Compressed recovery code is uncompressed in F000:0000 in shadow RAM and give control to recovery code in F000 shadow RAM. Initialize interrupt vector tables, initialize system timer, initialize DMA controller and interrupt controller.
E8	Initialize extra (Intel recovery) module.
E9	Initialize floppy drive.
EA	Try to boot from floppy. If reading of boot sector is successful, give control to boot sector code.
EB	Booting from floppy failed, look for ATAPI (LS120, Zip) devices.
EC	Try to boot from ATAPI. If reading of boot sector is successful, give control to boot sector code.
EF	Booting from floppy and ATAPI device failed. Give two beeps. Retry the booting procedure again (go to check point E9).

Table 76. Runtime Code Uncompressed in F000 Shadow RAM

Code	Description of POST Operation
03	NMI is disabled. To check soft reset / power-on.
05	BIOS stack set. Going to disable cache if any.
06	POST code to be uncompressed.
07	CPU init and CPU data area init to be done.
08	CMOS checksum calculation to be done next.
0B	Any initialization before keyboard BAT to be done next.
0C	KB controller I/B free. To issue the BAT command to keyboard controller.
0E	Any initialization after KB controller BAT to be done next.
0F	Keyboard command byte to be written.
10	Going to issue Pin-23,24 blocking / unblocking command.
11	Going to check pressing of <INS>, <END> key during power-on.
12	To init CMOS if "Init CMOS in every boot" is set or <END> key is pressed. Going to disable DMA and Interrupt controllers.
13	Video display is disabled and port-B is initialized. Chipset init about to begin.
14	8254 timer test about to start.
19	About to start memory refresh test.
1A	Memory Refresh line is toggling. Going to check 15 µs ON/OFF time.
23	To read 8042 input port and disable Megakey GreenPC feature. Make BIOS code segment writeable.
24	To do any setup before Int vector init.
25	Interrupt vector initialization to begin. To clear password if necessary.
27	Any initialization before setting video mode to be done.
28	Going for monochrome mode and color mode setting.
2A	Different buses init (system, static, output devices) to start if present. (See Section 5.3 for details of different buses.)
2B	To give control for any setup required before optional video ROM check.
2C	To look for optional video ROM and give control.
2D	To give control to do any processing after video ROM returns control.
2E	If EGA / VGA not found then do display memory R/W test.
2F	EGA / VGA not found. Display memory R/W test about to begin.
30	Display memory R/W test passed. About to look for the retrace checking.
31	Display memory R/W test or retrace checking failed. To do alternate Display memory R/W test.
32	Alternate display memory R/W test passed. To look for the alternate display retrace checking.
34	Video display checking over. Display mode to be set next.
37	Display mode set. Going to display the power-on message.
38	Different buses init (input, IPL, general devices) to start if present. (See Section 5.3 for details of different buses.)
39	Display different buses initialization error messages. (See Section 5.3 for details of different buses.)
3A	New cursor position read and saved. To display the Hit <DEL> message.

continued

Table 76. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
40	To prepare the descriptor tables.
42	To enter in virtual mode for memory test.
43	To enable interrupts for diagnostics mode.
44	To initialize data to check memory wrap around at 0:0.
45	Data initialized. Going to check for memory wrap around at 0:0 and finding the total system memory size.
46	Memory wrap around test done. Memory size calculation over. About to go for writing patterns to test memory.
47	Pattern to be tested written in extended memory. Going to write patterns in base 640k memory.
48	Patterns written in base memory. Going to find out amount of memory below 1M memory.
49	Amount of memory below 1M found and verified. Going to find out amount of memory above 1M memory.
4B	Amount of memory above 1M found and verified. Check for soft reset and going to clear memory below 1M for soft reset. (If power on, go to check point # 4Eh).
4C	Memory below 1M cleared. (SOFT RESET) Going to clear memory above 1M.
4D	Memory above 1M cleared. (SOFT RESET) Going to save the memory size. (Go to check point # 52h).
4E	Memory test started. (NOT SOFT RESET) About to display the first 64k memory size.
4F	Memory size display started. This will be updated during memory test. Going for sequential and random memory test.
50	Memory testing/initialization below 1M complete. Going to adjust displayed memory size for relocation/ shadow.
51	Memory size display adjusted due to relocation / shadow. Memory test above 1M to follow.
52	Memory testing / initialization above 1M complete. Going to save memory size information.
53	Memory size information is saved. CPU registers are saved. Going to enter in real mode.
54	Shutdown successful, CPU in real mode. Going to disable gate A20 line and disable parity/NMI.
57	A20 address line, parity/NMI disable successful. Going to adjust memory size depending on relocation / shadow.
58	Memory size adjusted for relocation / shadow. Going to clear Hit <DEL> message.
59	Hit <DEL> message cleared. <WAIT...> message displayed. About to start DMA and interrupt controller test.
60	DMA page register test passed. To do DMA#1 base register test.
62	DMA#1 base register test passed. To do DMA#2 base register test.
65	DMA#2 base register test passed. To program DMA unit 1 and 2.
66	DMA unit 1 and 2 programming over. To initialize 8259 interrupt controller.
7F	Extended NMI sources enabling is in progress.
80	Keyboard test started. Clearing output buffer, checking for stuck key, to issue keyboard reset command.
81	Keyboard reset error / stuck key found. To issue keyboard controller interface test command.
82	Keyboard controller interface test over. To write command byte and init circular buffer.
83	Command byte written, global data init done. To check for lock-key.

continued

Table 76. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
84	Lock-key checking over. To check for memory size mismatch with CMOS.
85	Memory size check done. To display soft error and check for password or bypass setup.
86	Password checked. About to do programming before setup.
87	Programming before setup complete. To uncompress SETUP code and execute CMOS setup.
88	Returned from CMOS setup program and screen is cleared. About to do programming after setup.
89	Programming after setup complete. Going to display power-on screen message.
8B	First screen message displayed. <WAIT...> message displayed. PS/2 Mouse check and extended BIOS data area allocation to be done.
8C	Setup options programming after CMOS setup about to start.
8D	Going for hard disk controller reset.
8F	Hard disk controller reset done. Floppy setup to be done next.
91	Floppy setup complete. Hard disk setup to be done next.
95	Init of different buses optional ROMs from C800 to start. (See Section 5.3 for details of different buses.)
96	Going to do any init before C800 optional ROM control.
97	Any init before C800 optional ROM control is over. Optional ROM check and control will be done next.
98	Optional ROM control is done. About to give control to do any required processing after optional ROM returns control and enable external cache.
99	Any initialization required after optional ROM test over. Going to setup timer data area and printer base address.
9A	Return after setting timer and printer base address. Going to set the RS-232 base address.
9B	Returned after RS-232 base address. Going to do any initialization before Coprocessor test.
9C	Required initialization before Coprocessor is over. Going to initialize the Coprocessor next.
9D	Coprocessor initialized. Going to do any initialization after Coprocessor test.
9E	Initialization after coprocessor test is complete. Going to check extended keyboard, keyboard ID and num-lock.
A2	Going to display any soft errors.
A3	Soft error display complete. Going to set keyboard typematic rate.
A4	Keyboard typematic rate set. To program memory wait states.
A5	Going to enable parity/NMI.
A7	NMI and parity enabled. Going to do any initialization required before giving control to optional ROM at E000.
A8	Initialization before E000 ROM control over. E000 ROM to get control next.
A9	Returned from E000 ROM control. Going to do any initialization required after E000 optional ROM control.
AA	Initialization after E000 optional ROM control is over. Going to display the system configuration.
AB	Put INT13 module runtime image to shadow.
AC	Generate MP for multiprocessor support (if present).
AD	Put CGA INT10 module (if present) in Shadow.

continued

Table 76. Runtime Code Uncompressed in F000 Shadow RAM (continued)

Code	Description of POST Operation
AE	Uncompress SMBIOS module and init SMBIOS code and form the runtime SMBIOS image in shadow.
B1	Going to copy any code to specific area.
00	Copying of code to specific area done. Going to give control to INT-19 boot loader.

5.3 Bus Initialization Checkpoints

The system BIOS gives control to the different buses at several checkpoints to do various tasks. Table 77 describes the bus initialization checkpoints.

Table 77. Bus Initialization Checkpoints

Checkpoint	Description
2A	Different buses init (system, static, and output devices) to start if present.
38	Different buses init (input, IPL, and general devices) to start if present.
39	Display different buses initialization error messages.
95	Init of different buses optional ROMs from C800 to start.

While control is inside the different bus routines, additional checkpoints are output to port 80h as WORD to identify the routines under execution. In these WORD checkpoints, the low byte of the checkpoint is the system BIOS checkpoint from which the control is passed to the different bus routines. The high byte of the checkpoint is the indication of which routine is being executed in the different buses. Table 78 describes the upper nibble of the high byte and indicates the function that is being executed.

Table 78. Upper Nibble High Byte Functions

Value	Description
0	func#0, disable all devices on the bus concerned.
1	func#1, static devices init on the bus concerned.
2	func#2, output device init on the bus concerned.
3	func#3, input device init on the bus concerned.
4	func#4, IPL device init on the bus concerned.
5	func#5, general device init on the bus concerned.
6	func#6, error reporting for the bus concerned.
7	func#7, add-on ROM init for all buses.

Table 79 describes the lower nibble of the high byte and indicates the bus on which the routines are being executed.

Table 79. Lower Nibble High Byte Functions

Value	Description
0	Generic DIM (Device Initialization Manager)
1	On-board System devices
2	ISA devices
3	EISA devices
4	ISA PnP devices
5	PCI devices

5.4 Speaker

A 47 Ω inductive speaker is mounted on the D815BN board. The speaker provides audible error code (beep code) information during POST.

For information about	Refer to
The location of the onboard speaker	Figure 1, page 14

5.5 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS displays an error message describing the problem (see Table 80). The BIOS also issues a beep code (one long tone followed by two short tones) during POST if the video configuration fails (a faulty video card or no card installed) or if an external ROM module does not properly checksum to zero.

An external ROM module (for example, a video BIOS) can also issue audible errors, usually consisting of one long tone followed by a series of short tones. For more information on the beep codes issued, check the documentation for that external device.

There are several POST routines that issue a POST terminal error and shut down the system if they fail. Before shutting down the system, the terminal-error handler issues a beep code signifying the test point error, writes the error to I/O port 80h, attempts to initialize the video and writes the error in the upper left corner of the screen (using both monochrome and color adapters).

If POST completes normally, the BIOS issues one short beep before passing control to the operating system.

Table 80. Beep Codes

Beep	Description
1	Refresh failure
2	Parity cannot be reset
3	First 64 KB memory failure
4	Timer not operational
5	Not used
6	8042 GateA20 cannot be toggled
7	Exception interrupt error
8	Display memory R/W error
9	Not used
10	CMOS Shutdown register test error
11	Invalid BIOS (e.g. POST module not found, etc.)

5.6 Diagnostic LEDs

The enhanced diagnostics feature consists of a hardware decoder and four LEDs located between the audio connectors and the serial port connector on the back panel. This feature requires no modifications to the chassis (other than I/O back panel shield) or cabling.

Figure 14 shows the location of the diagnostic LEDs. Table 81 lists the diagnostic codes displayed by the LEDs.

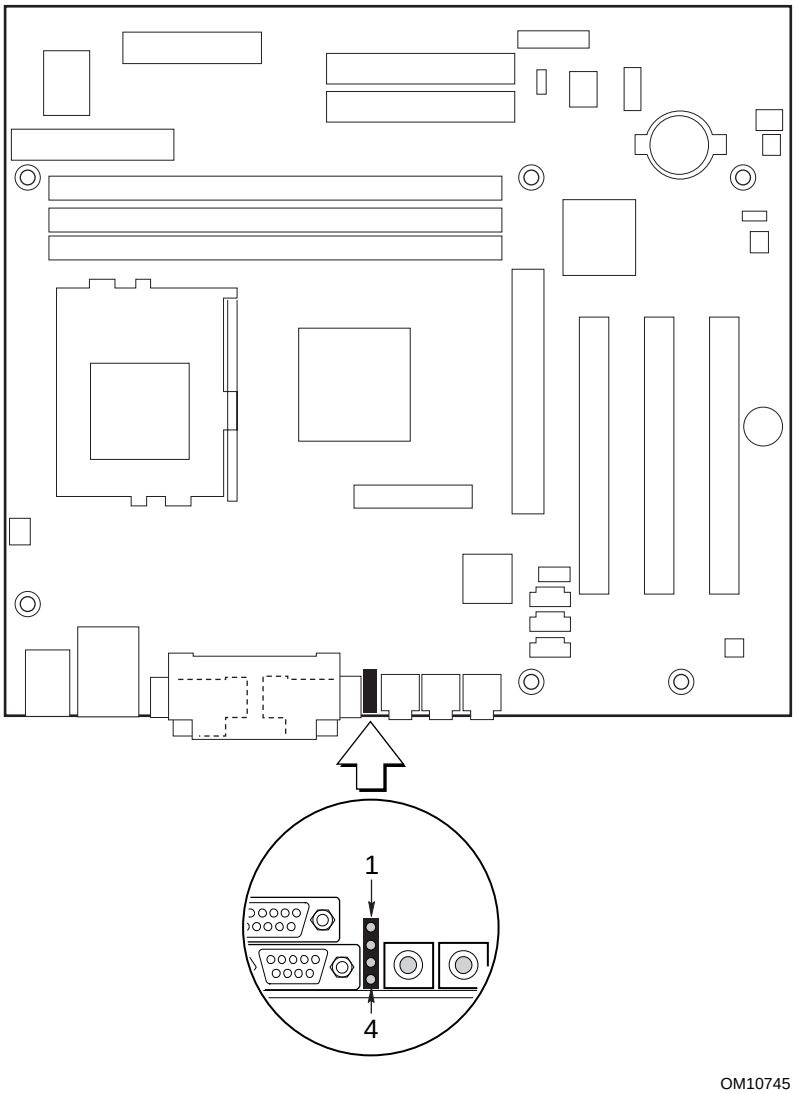
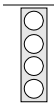
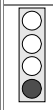
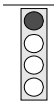
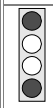
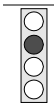
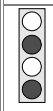
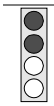
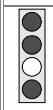
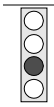
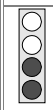
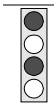
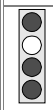
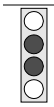
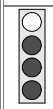
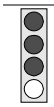
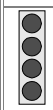


Figure 14. Diagnostic LEDs

Table 81. Diagnostic LED Codes

Display	BIOS Operation	Display	BIOS Operation
 Amber Amber Amber Amber	Power on, starting BIOS	 Amber Amber Amber Green	Reserved for future use
 Green Amber Amber Amber	Recovery mode	 Green Amber Amber Green	Reserved for future use
 Amber Green Amber Amber	Processor, cache, etc.	 Amber Green Amber Green	Reserved for future use
 Green Green Amber Amber	Memory, auto-size, shadow, etc.	 Green Green Amber Green	Reserved for future use
 Amber Amber Green Amber	PCI bus initialization	 Amber Amber Green Green	Reserved for future use
 Green Amber Green Amber	Video	 Green Amber Green Green	Reserved for future use
 Amber Green Green Amber	IDE bus initialization	 Amber Green Green Green	Reserved for future use
 Green Green Green Amber	USB initialization	 Green Green Green Green	Booting operating system

NOTE

After the computer has booted, the diagnostic LEDs remain off during normal operation.