YM430TX
Baby AT Motherboard
Technical Product Specification

June, 1997

Revision History

Revision	Revision History	Date
-001	Production Review.	17 June 97

This product specification applies only to standard YM430TX motherboards with BIOS identifier 1.00.XX.YM1.

Contents

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Motherboard Description

Overview

The YM430TX motherboard supports Pentium® processors and Pentium processors with MMX™ technology. The motherboard features:

- Baby AT form factor
- Socket 7 Pentium OverDrive® processor socket

Main Memory

I. DIMMS

- Two 168-pin DIMM sockets
- Support for up to 256 MB of:
  - — extended data out (EDO) memory
  - — unbuffered 4-clock synchronous DRAM (SDRAM) memory
- Up to 64 MB of main memory cacheable

II. SIMMS

- Four 72-pin SIMM sockets
- Support for up to 256 MB of:
  - — fast page mode (FPM) memory
  - — extended data out (EDO) memory

Second Level Cache Memory

- 512 KB pipeline burst static RAM (PBSRAM) soldered to the motherboard

Chipset and PCI/IDE Interface

- Intel 82430TX PCIset
- Integrated PCI bus mastering controller
- Two fast IDE interfaces
- Support for up to four IDE drives or devices
- Support for Ultra ATA drives

I/O Features

- Winbond* W83977TF-A Super Multi I/O controller
- Integrates standard I/O functions: floppy drive interface, one multimode parallel port, two FIFO serial ports, keyboard and mouse controller
- Support for two Universal Serial Bus (USB) interfaces
- Expansion Slots
  - — Three PCI
  - — Two ISA
  - — One shared PCI/ISA

Other features

- Plug and Play compatible
- Support for Advanced Power Management
- Year 2000 support

In the Box: This product will be shipped with the following contents per box.

- 1 YM430TX motherboard in anti-static bag

- 1 IDE cable
- 1 floppy drive cable
- 1 bracket with 2 serial cables
- 1 bracket with parallel cable
- 1 bracket with riser card with 2 USB ports and PS/2 mouse port
- 1 CD including BIOS flash utility, User manual with Warranty, Windows 95 update utility for 430TX PCIset, ISA Configuration Utility, Readme SW license agreement, Readme file describing contents
- 1 Adhesive label with diagrams for Motherboard layout and jumper configurations
- Intel hologram
- Foam packing material

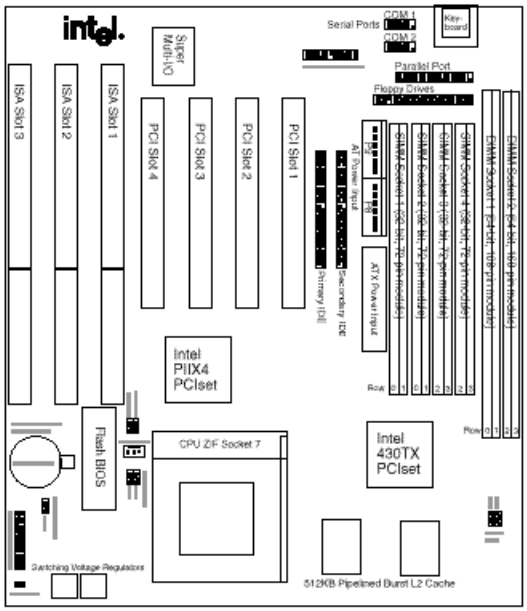

Figure 1. Motherboard Components

Form Factor

The motherboard is designed to fit into a standard Baby AT form factor chassis. Figure 22 illustrates the form factor for the motherboard. The locations of the mounting holes are in strict compliance with the Baby AT specification (see Specifications section for compliance level).

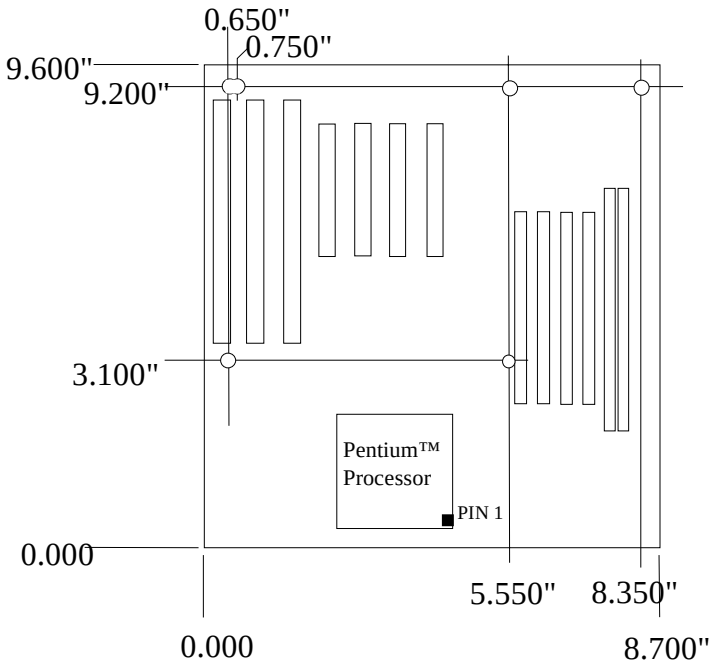

Figure 2. Motherboard Dimensions

Microprocessor

The motherboard supports:

- Pentium processors operating at 90, 100, 120, 133, 150, 166, and 200 MHz
- Pentium processors with MMX technology operating at 166, 200, and 233 MHz

An onboard voltage regulator derives the necessary voltage from the computer's power supply and enables use of standard or VRE-specified processors. The motherboard automatically detects the type of processor (Pentium processor or Pentium processor with MMX technology).

Microprocessor Upgrade

The motherboard has a 321-pin Socket 7 zero insertion force (ZIF) microprocessor socket. Socket 7 supports upgrades to higher performance Pentium OverDrive processors not supported by Socket 5. The motherboard's BIOS has support for Pentium OverDrive processors with MMX technology.

Memory

Main Memory

The motherboard has two 168-pin DIMM sockets. Memory can be installed in one or two sockets. Minimum memory size is 8 MB. Maximum memory size is 256 MB.
The motherboard supports the following:

- 168-pin 3.3 V DIMMs with gold-plated contacts
- 60 and 66 MHz bus speeds
- 60 ns 3.3 V EDO DRAM

- 60 ns unrestricted CAS Latency 2 unbuffered 4-clock 3.3 V SDRAM
- Caching for the first 64 MB of main memory
- 64-bit data path
- Single- or double-sided DIMMs in the following sizes:

DIMM size	Type	Configuration	Technology
8 MB	60 ns EDO	1M x 64	16 Mbit
16 MB	60 ns EDO	2M x 64	16 Mbit
32 MB	60 ns EDO	4M x 64	16 Mbit
64 MB	60 ns EDO	8M x 64	16 Mbit
8 MB	CAS Latency 2 SDRAM	1M x 64	16 Mbit
16 MB	CAS Latency 2 SDRAM	2M x 64	16 Mbit
32 MB	CAS Latency 2 SDRAM	4M x 64	16 Mbit
64 MB	CAS Latency 2 SDRAM	8M x 64	64 Mbit
128 MB	CAS Latency 2 SDRAM	16M x 64	64 Mbit

Memory type, size, and speed can vary between sockets, so EDO and SDRAM can be installed on the same motherboard. Parity (x 72) DIMMs can be installed but are not recommended for the following reasons:

- The motherboard does not provide parity checking or ECC

The motherboard also has four 72-pin SIMM sockets. Memory must be installed in pairs. Minimum memory size is 8 MB. Maximum memory size is 256 MB.
The motherboard supports the following:

- 72-pin 5 V SIMMs with tin-plated contacts
- 60 and 66 MHz bus speeds
- 60 ns 5 V FPM or EDO DRAM
- Caching for the first 64 MB of main memory
- Single- or double-sided SIMMs in the following sizes:

SIMM size	Type	Configuration	Technology
4 MB	60 ns EDO	1M x 32	16 Mbit
8 MB	60 ns EDO	1M x 64	16 Mbit
16 MB	60 ns EDO	2M x 64	16 Mbit
32 MB	60 ns EDO	4M x 64	16 Mbit
64 MB	60 ns EDO	8M x 64	16 Mbit

EDO DRAM

EDO DRAM improves memory read performance by holding the memory data valid until the next CAS# falling edge, unlike fast page mode DRAM, which tri-states the memory data when CAS# negates to precharge for the next memory cycle. With EDO DRAM, the CAS# precharge overlaps the data-valid time, which allows CAS# to negate earlier while still satisfying the memory data-valid window.

SDRAM

Synchronous DRAM (SDRAM) is designed to improve main memory performance. Unlike fast page or EDO DRAM, SDRAM is synchronous with the memory clock. This simplifies the timing design and increases memory

speed because all timing is dependent on the number of memory clock cycles. SDRAM DIMM modules should meet the Intel "4-clock 66 MHz 64-bit unbuffered SDRAM DIMM, V. 1.0" specification.

⚠ CAUTION

SIMMS and DIMMS cannot be used simultaneously due to the data output voltage level differences between 5V SIMMS and 3.3V DIMMS. The board does not support SDRAM DIMMs with an n x 4 DRAM base due to loading anomalies. For example, a DIMM that uses sixteen 16 Mbit x 4 devices should not be used.

NOTE

The YM430TX supports unbuffered, 4-clock 3.3 V SDRAM DIMMs only. Buffered, 5 V, or 2-clock SDRAM DIMMs should not be used.

Second Level Cache

The 512 KB direct-mapped write-back L2 cache consists of two 64K x 32 global write enable (GWE) pipeline burst static RAMs (PBSRAMs) and a 32K or 16K x 8 external tag SRAM. These devices are soldered to the motherboard.

Chipset

The Intel 82430TX PCIset consists of the TX System Controller (MTXC) device and the PCI ISA IDE Xcelerator (PIIX4) device.

430TX System Controller (MTXC)

The MTXC integrates the cache and main memory DRAM control functions and provides bus control to handle transfers between the processor, cache, main memory, and the PCI bus. The MTXC allows PCI masters to achieve full PCI bandwidth by using the snoop ahead feature. For increased system performance the MTXC integrates posted write and read prefetch buffers. The MTXC comes in a 324-pin MBGA package that features:

- Microprocessor interface control
- Integrated L2 write-back cache controller
  - — Supports pipeline burst SRAM
  - — 64 MB maximum DRAM cacheability
  - — Direct mapped organization—write back only
  - — Cache hit read/write cycle timings at 3-1-1-1
  - — Back to back read/write cycles at 3-1-1-1-1-1-1-1
- Integrated DRAM controller
  - — 8 MB to 256 MB main memory
  - — 64-Mbit DRAM/SDRAM technology support
  - — 3.3 V EDO and unbuffered synchronous DRAM support
  - — Non-parity (x64) support only
- Fully synchronous minimum latency PCI bus interface
  - — PCI compliance (see Specifications section for compliance level)
  - — 30 and 33 MHz bus speeds
  - — PCI to DRAM data throughput at greater than 100 MB/sec
  - — Up to four PCI masters in addition to the PIIX4
- Power management control

- Provides PCI CLKRUN# signal to control memory clock on the PCI bus (on/off)

430TX PCI ISA IDE Xcelerator (PIIX4)

The Intel 430TX PCI ISA IDE Xcelerator (PIIX4) is a multifunction PCI device implementing a PCI to ISA bridge, PCI IDE functionality, a Universal Serial Bus (USB) host/hub function, and Enhanced Power Management. The PIIX4 comes in a 324-pin MBGA package that features:

- Multifunction PCI to ISA bridge
  - Supports the PCI bus at 30 and 33 MHz
  - PCI compliant (see Specifications section for compliance level)
  - Full ISA or extended I/O (EIO) bus support
- USB controller
  - Two USB ports (see Specifications section for compliance level)
  - Supports UHCI design guide revision 1.1 interface
- Integrated dual-channel enhanced IDE interface
  - Support for up to four IDE devices
  - PIO Mode 4 transfers at up to 14 MB/sec
  - Supports "Ultra ATA" synchronous DMA mode transfers up to 33 MB/sec
  - Integrated 8 x 32-bit buffer for bus master PCI IDE burst transfers
  - Bus master mode
- Enhanced DMA controller
  - Two 8237-based DMA controllers
  - Supports PCI DMA with three PC/PCI channels and distributed DMA protocols
  - Fast type-F DMA for reduced PCI bus usage
- Interrupt controller based on 82C59
  - Support for 15 interrupts
  - Programmable for edge/level sensitivity
- Power management logic
  - Sleep/resume logic
  - Support for Wake On Modem through Ring Indicate input
- Real-Time Clock
  - 256 byte battery-backed CMOS SRAM
  - Includes date alarm
- 16-bit counters/timers based on 82C54

Universal Serial Bus (USB) Support

The motherboard features two USB ports on the USB / PS/2 Mouse connector card. The ports permit the direct connection of two USB peripherals without an external hub. If more devices are required, an external hub can be connected to either of the ports. The motherboard fully supports the standard universal host controller interface (UHCI) and uses standard software drivers that are UHCI-compatible. Features of the USB include:

- Self-identifying, hot pluggable peripherals
- Automatic mapping of function to driver and configuration
- Support for isochronous and asynchronous transfer types over the same set of wires
- Support for up to 127 physical devices

- Guaranteed bandwidth and low latencies appropriate for telephony, audio, and other applications
- Error handling and fault recovery mechanisms built into protocol

NOTE

Computers that have an unshielded cable attached to the USB port might not meet FCC Class B requirements, even if no device or a low speed USB device is attached to the cable. Use shielded cable that meets the requirements for full speed devices.

IDE Support

The motherboard has two independent bus mastering PCI IDE interfaces that support PIO Mode 3, PIO Mode 4, ATA-33 (Ultra ATA), and ATAPI (e.g., CD-ROM) devices. The BIOS supports Logical Block Addressing (LBA) and Extended Cylinder Head Sector (ECHS) translation modes. IDE device transfer rate and translation mode are automatically detected by the BIOS.

Normally, programmed I/O operations require a substantial amount of processor bandwidth; however, in multi-tasking operating systems like Windows† 95, the bandwidth freed by bus mastering IDE can be devoted to other tasks while disk transfers are occurring.

Super I/O Controller

The Winbond W83977TF-A Super Multi I/O Controller is a multifunction I/O device that provides the following features:

- Serial ports:
  - Two 16550-software compatible UARTs
  - Send/receive 16-byte FIFO
- Multimode bidirectional parallel port
  - Standard mode, IBM† compatible
  - Enhanced Parallel Port (EPP) mode with BIOS and driver support
  - High-speed Extended Capabilities Port (ECP) mode
- Floppy disk controller
  - 82077 compatible
  - 16 byte FIFO
- Keyboard and mouse controller
  - Industry standard 8042 compatible
  - General purpose microcontroller
  - 8 bit internal data bus

By default, the I/O controller interfaces are automatically configured during boot up. The I/O controller can also be manually configured in the Setup program, or disabled by jumper.

Serial Ports

The motherboard has two keyed 10-pin header located on the motherboard for cabling to the back panel. The 16550 compatible UARTs support data transfers at speeds up to 921.6 Kbits/sec, while the extended UART mode supports data rates up to 1.5 Mbits/sec.

Parallel Port

The motherboard has a keyed 26-pin header for the multimode bidirectional parallel port. In the Setup program, there are four options for parallel port operation:

- Normal (standard mode)
- Enhanced Parallel Port (EPP) (see Specifications section for EPP specification compliance level)
- Extended Capabilities Port (ECP)
- Bidirectional (ECP + EPP)

Floppy Controller

The I/O controller is software compatible with the 82077 floppy drive controller and supports both PC-AT and PS/2 modes. In the Setup program, the floppy interface can be configured for the following floppy drive capacities and sizes:

- 360 KB, 5.25-inch
- 1.2 MB, 5.25-inch
- 720 KB, 3.5-inch
- 1.2 MB, 3.5-inch (driver required)
- 1.25/1.44 MB, 3.5-inch
- 2.88 MB, 3.5-inch

Keyboard and Mouse Interface

An AT keyboard connector is located on the back panel of the motherboard. A PS/2 mouse connector is located on the USB / PS/2 mouse connector card.

The 5 V lines to these connectors are protected with a PolySwitch† circuit that, like a self-healing fuse, reestablishes the connection after an over-current condition is removed. While this device eliminates the possibility of having to replace a fuse, power to the computer should be turned off before connecting or disconnecting a keyboard or mouse.

The keyboard controller contains the AMIkey† keyboard and mouse controller code, which provides the traditional keyboard and mouse control functions, and also supports Power On/Reset password protection. A Power On/Reset password can be specified in the Setup program.

The keyboard controller also supports software reset (<Ctrl><Alt><Del>). This key sequence resets the computer's software by jumping to the beginning of the BIOS code and running the Power-on Self Test (POST).

Motherboard Connectors

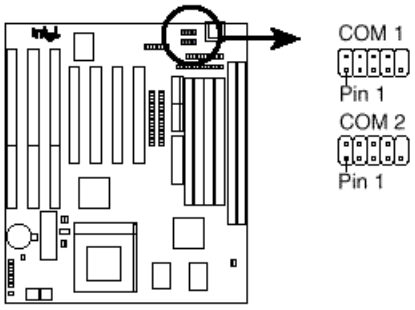

Figure 3. Serial Port Headers

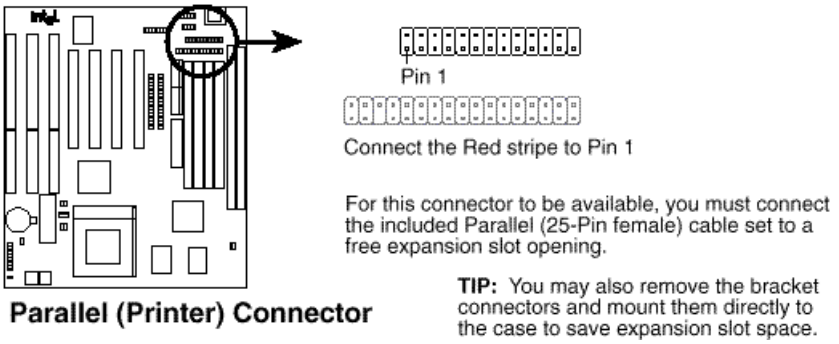

Figure 4. Parallel Port Connector

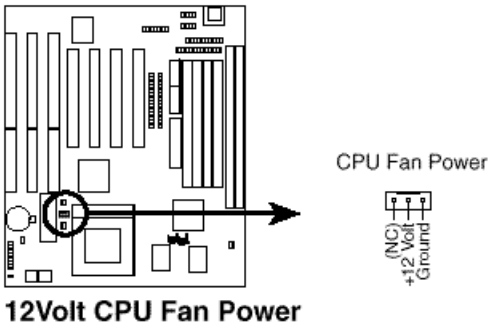

Figure 5. CPU Fan Connector

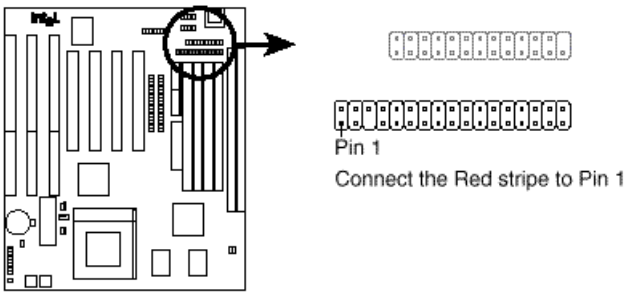

Figure 6. Floppy Drive Connector

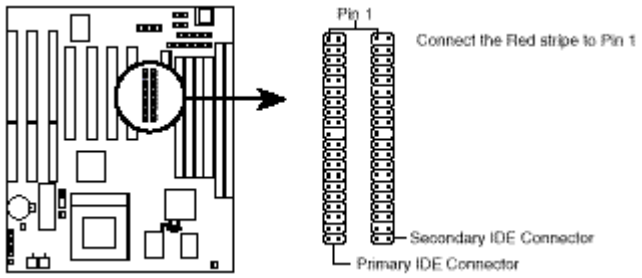

Figure 7. PCI IDE Connectors

Power Supply Connectors

The YM430TX features both a standard AT power connector and a standard ATX power connector to support an AT or ATX power supply with soft on/off features. When used with a power supply that supports remote power on/off, the motherboard can turn off the computer's power through software control. Pin 14 of the ATX power supply connector lets the motherboard recognize a power supply that supports this "soft-off" feature; the power supply must tie pin 14 to ground. When the BIOS receives the correct APM command from the operating system, the BIOS turns off power to the computer. For example, in the Windows 95 Start menu, the user selects Shutdown to turn off the power. If power to the computer is interrupted by a power outage or a disconnected power cord, when power resumes, the computer returns to the off state until the power switch is pressed.

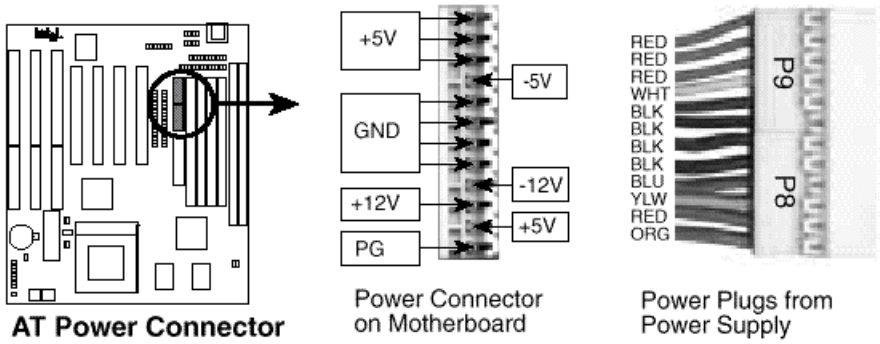

Figure 8. AT Power Connector

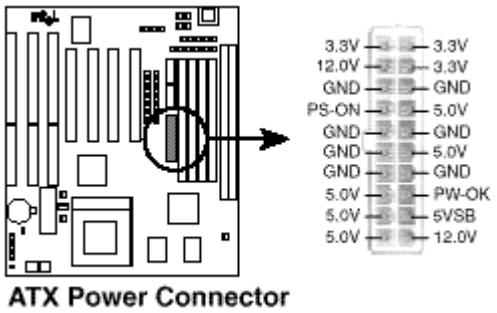

Figure 9. ATX Power Connector

Front Panel Connectors

The front panel connector includes headers for these I/O connections:

- Speaker
- Reset switch
- SMI Lead
- Hard drive activity LED
- Keyboard lock
- ATX Power switch
- Power LED
- Message LED

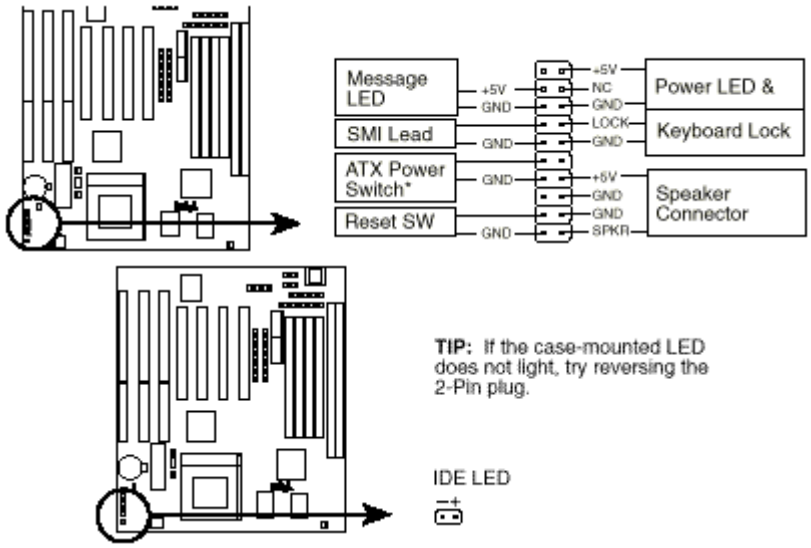

Figure10. Front Panel I/O Connectors

ATX Power Switch / Soft Power Switch (PWR SW) (For ATX power supplies)

With an ATX power supply, system power can be controlled by a momentary switch connected to this lead. Pressing the switch once toggles the system between on

and sleep. The power management section in BIOS setup, has an option to use the PWR button to suspend the system. In this mode, pressing the switch for more than 4 seconds turns the system off. The system power LED shows the status of the system's power.

SMI Suspend Switch Lead (SMI)

When Advanced Power Management (APM) is enabled in the BIOS and the operating system's APM driver is loaded, the computer can enter Sleep (Standby) mode in one of two ways:

- Optional front panel Sleep/Resume button
- Inactive for one to sixteen minutes, as configured in the power menu in BIOS Setup

A sleep/resume button is supported by the 2-pin header located on the front panel I/O connector. The front panel sleep/resume switch must be a momentary SPST type that is normally open.

Closing the sleep/resume switch generates a system management interrupt (SMI) to the processor, which immediately goes into system management mode (SMM). While the computer is in sleep mode it is fully capable of responding to and servicing external interrupts (such as an incoming fax) even though the monitor turns on only if a keyboard or mouse interrupt occurs. To reactivate the computer, or resume, you must press the sleep/resume button again, or use the keyboard or mouse.

IDE activity LED (IDE LED)

This connector supplies power to the cabinet's IDE activity LED. Read or write activity by devices connected to the primary or secondary IDE connectors will cause the LED to light up.

Power LED

You can connect this header to an LED that will light when the computer is powered on. This LED will also blink when the computer is in a power-managed state.

Message LED

This LED indicates whether a message has been received from a FAX/modem. The LED will remain lit when there is no signal, and blink when data has been transferred.

Reset

You can connect this header to a momentary SPST type switch that is normally open. When the switch is closed, the board resets and runs the POST.

Speaker

A speaker may be installed on the motherboard as a manufacturing option. The speaker provides error beep code information during the Power-on Self Test (POST) in the event that the computer cannot use the video interface. The speaker is not connected to the audio subsystem, and does not receive output from the audio subsystem.

Keyboard Lock

This connector connects to a case mounted keyboard lock switch for locking the keyboard.

Back Panel Connectors

Figure 11 shows the location of the back panel I/O connectors, which include:

- Two USB connectors
- PS/2-style mouse connector

Figure 12 shows the location of the standard AT keyboard connector.

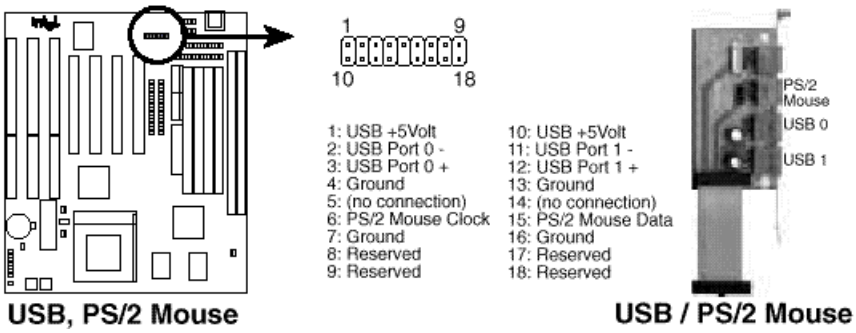

Figure 11. USB / PS/2 Mouse Connector Card

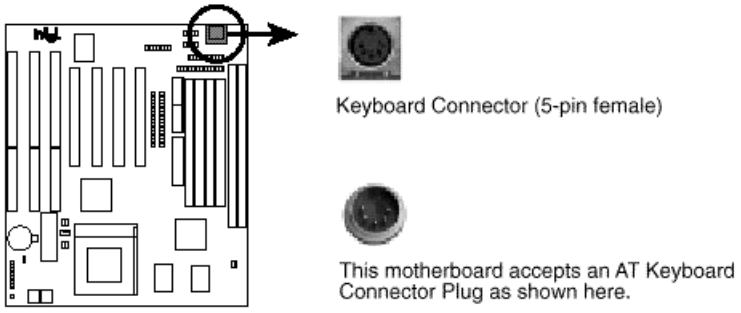

Figure 12. Keyboard Connector

Add-in Board Expansion Connectors

The PCI bus supports up to four bus masters through the four PCI connectors (see Specifications section for information about compliance with the PCI specification).

Jumper Settings

Flash ROM Boot Block Programming (BBLKW)

This sets the operation mode of the boot block area of the Programmable Flash ROM to allow programming in the *Enabled* position. This is required only if prompted by the **Flash Memory Writer Utility** as shown in BIOS and Setup.

Programming	BBLKW
Boot Block Write-Protect	[1-2] (Default)
Boot BLock Write Enable	[2-3]

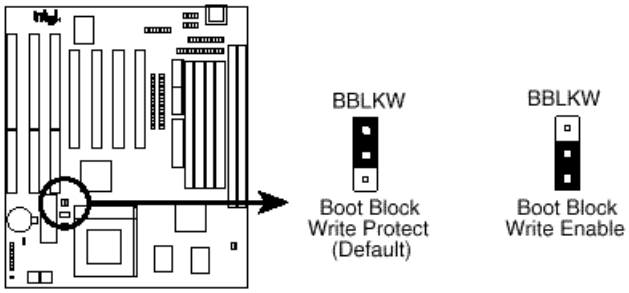

Figure 13. BBLKW Jumper

Real Time Clock (RTC) RAM (RTCLR)

The CMOS RAM is powered by the onboard button cell battery. To clear the RTC data: (1) Turn off your computer, (2) Move this jumper to "Clear Data," (3) Move the jumper back to "Operation," (4) Turn on your computer, (5) Hold down <Delete> during bootup and enter BIOS setup to re-enter user preferences.

Battery Test Jumper (RTCLR)

You can test the battery's current by removing this jumper and attaching a cur-rent meter to pins 2&3. **WARNING: You must unplug the power cord to your power supply to ensure that there is no power to your motherboard. The CMOS RAM containing BIOS setup information *may* be cleared by this action. You *should* enter BIOS to "Load Setup Defaults" and re-enter any user information after removing and reapplying this jumper.**

RTC RAM	RTCLR
Keep CMOS	[1-2] (Default)
Clear CMOS	[2-3] (momentarily)

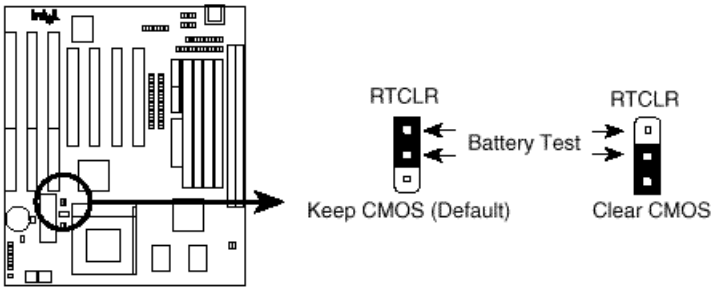

Figure 14. RTC, RTCLR Jumper

Voltage Regulator Output Selection (VID0, 1, 2)

These jumpers set the voltage supplied to the CPU. The voltage regulators will automatically detect and switch **between Single Power Plane & Dual Power Planes**.

	(Single Plane)		(Dual Plane)		
Type	Vcore	Vio	Vcore	Vio	VID0
VRE	3.5V	3.5V	2.9V	3.3V	[1-2]
STD	3.4V	3.4V	2.8V	3.3V	[2-3]

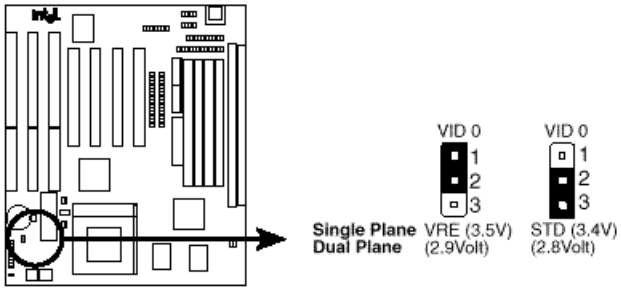

Figure 15. VID Jumper

CPU External (BUS) Frequency Selection (FS0, FS1,)

These jumpers tell the clock generator what frequency to send to the CPU. These allow the selection of the CPU's *External* frequency (or *BUS Clock*). The BUS Clock times the BUS Ratio equals the CPU's *Internal* frequency (the advertised CPU speed).

CPU to BUS Frequency Ratio (BF0, BF1)

These jumpers set the frequency ratio between the *Internal* frequency of the CPU
and the *External* frequency (called the *BUS Clock*) within the CPU. These must be set together with the above jumpers *CPU External (BUS) Frequency Selection.*

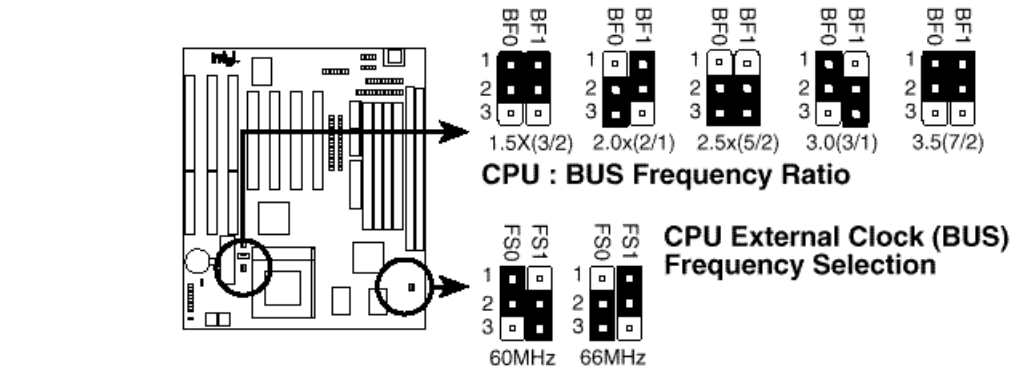

Figure 16. BF Jumper

Processor Configuration

The motherboard must be configured for the frequency of the installed processor. Table 1 shows the jumper settings for each frequency and the corresponding host bus frequencies.

Table . 1 Jumper Settings for Processor and Bus Frequencies

Processor Freq. (MHz)	Jumper FS0	Jumper FS1	Jumper BF0	Jumper BF1	Host Bus Freq. (MHz)	Bus/Processor Freq. Ratio
233	2-3	1-2	1-2	1-2	66	3.5
200	2-3	1-2	1-2	2-3	66	3
166	2-3	1-2	2-3	2-3	66	2.5
150	1-2	2-3	2-3	2-3	60	2.5
133	2-3	1-2	2-3	1-2	66	2
120	1-2	2-3	2-3	1-2	60	2
100	2-3	1-2	1-2	1-2	66	1.5
90	1-2	2-3	1-2	1-2	60	1.5

⚠ **CAUTION**

Do not move any of the jumpers with the power on. Always turn off the power and unplug the power cord from the computer before changing jumpers. Changing the jumper settings when the power is off ensures that the changes will be recognized.

CAUTION

When installing a processor in the motherboard for the first time or upgrading to a new processor, check the processor's documentation for the correct voltage setting. Operating the processor at the wrong voltage can cause unreliable performance.

Environmental

Table 2. Motherboard Environmental Specifications

Parameter	Specification
Temperature	
Operating	0 °C to +55 °C

Power Consumption

Tables 3 and 4 list voltage and current specifications for a computer that contains the motherboard, a 200 MHz Pentium processor with MMX technology, 32 MB SDRAM, 512KB cache, 2 MB SGRAM graphics memory, a 3.5-inch floppy drive, a 1.6 GB hard drive, an 8X IDE CD-ROM, and a 28.8 Kbits/sec ISA faxmodem. This information is preliminary and is provided only as a guide for calculating **approximate** power usage with additional resources added.

NOTE

AC power measurements include all peripheral components mentioned above. DC current measurements include only the motherboard components.

Table 3. DC Voltage

DC Voltage	Acceptable Tolerance
+3.3 V	± 5%
+5 V	± 5%
-5 V	± 5%
+12 V	± 5%
-12 V	± 5%

Table 4. Power Usage for a Static Windows 95 Desktop

APM Mode	System AC (watts)	Motherboard DC (amps)				
		+3.3 V	**+5 V**	**-5 V**	**+12 V**	**-12 V**
APM disabled in BIOS	58	0.9	5.0	0.01	0.16	0.03
Maximum power savings	28	0.6	2.0	0.01	0.13	0.03

Regulatory Compliance

This printed circuit assembly complies with the following safety and EMI regulations when correctly installed in a compatible host system.

Safety

UL 1950 - CSA 950-95, 3rd edition, Dated 3-28-95

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (USA & Canada)

CSA C22.2 No. 950-93, 3rd Edition

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (Canada)

EN 60 950, 2nd Edition, 1992 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (European Union)

IEC 950, 2nd edition, 1991 (with Amendments 1, 2 & 3)

The Standard for Safety of Information Technology Equipment including Electrical Business Equipment. (International)

EMKO-TSE (74-SEC) 207/94

Summary of Nordic deviations to EN 60 950. (Norway, Sweden, Denmark & Finland)

EMI

FCC Class B

Title 47 of the Code of Federal Regulations, Parts 2 & 15, Subpart B, pertaining to unintentional radiators. (USA)

CISPR 22, 2nd Edition, 1993

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (International)

EN 55 022, 1995

Limits and methods of measurement of Radio Interference Characteristics of Information Technology Equipment. (Europe)

EN 50 082-1 (1992)

Generic Immunity Standard; Currently compliance is determined via testing to IEC 801-2, -3 and -4. (Europe)

VCCI Class 2 (ITE)

Implementation Regulations for Voluntary Control of Radio Interference by Data Processing Equipment and Electronic Office Machines. (Japan)

ICES-003, Issue 2

Interference-Causing Equipment Standard, Digital Apparatus. (Canada)

Product Certification Markings

This printed circuit assembly has the following product certification markings:

- European CE Marking: Consists of the European Community "CE" mark on the board and shipping container.
- UL Recognition Mark: Consists of the company name "Intel" and the board model number "YM430TX" and AA#682162-xxx on the component side of the board. Board material flammability is 94V-1 or -0.
- Australian C-Tick EMI Compliance Mark: Consists of a solid circle with a white tick (check) mark within the circle, accompanied by the Intel 4-digit supplier code (N232). Marking provided on shipping container.

Motherboard Resources

Memory Map

Table 5 Memory Map

Address Range (Decimal)	Address Range (hex)	Size	Description
1024K-262144K	100000-10000000	255M	Extended Memory
960K-1023K	F0000-FFFFF	64K	Award System BIOS
896K-959K	E0000-EFFFF	64K	BIOS reserved while boot-up. Available HI DOS memory after execute boot-strap loader
800-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA and PCI** bus)
640K-799K	A0000-C7FFF	160K	Video memory and BIOS
512K-640K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

** Peripheral Component Interconnect

I/O Map

Table 6 I/O Map

Address (hex)	Size	Description	Address (hex)	Size	Description
0000 - 000F	16 bytes	PIIX4 - DMA 1			
0020 - 0021	2 bytes	PIIX4 - Interrupt Controller 1	0376	1 byte	Sec Integrated Drive Electronics (IDE) Chan Cmd Port
002E - 002F	2 bytes	87308B Base Configuration	0377	1 byte	Sec IDE Chan Stat Port
0040 - 0043	4 bytes	PIIX4 - Timer 1	0378 - 037F	8 bytes	Parallel Port 1
0060	1 byte	Keyboard Controller Byte - Reset IRQ	03BC - 03BF	4 bytes	Parallel Port 3
0061	1 byte	PIIX4 - NMI, speaker control	03E8 - 03EF	8 bytes	COM 3

continued ☛

Table 7 I/O Map (continued)

Address (hex)	Size	Description	Address (hex)	Size	Description
0064	1 byte	Keyboard Controller, CMD/STAT Byte	03F0 - 03F5	6 bytes	Floppy Channel 1
0070, bit 7	1 bit	PIIX4 - Enable NMI	03F6	1 byte	Primary IDE Chan Cmd Port
0070, bits 6:0	7 bits	PIIX4 - Real Time Clock, Address	03F7 (Write)	1 byte	Floppy Chan 1 Cmd
0071	1 byte	PIIX4 - Real Time Clock, Data	03F7, bit 7	1 bit	Floppy Disk Chg Chan 1
0072	1 byte	PIIX4 - RTC Extended Index	03F7, bits 6:0	7 bits	Primary IDE Chan Status Port
0073	1 byte	PIIX4 - RTC Extended data	03F8 - 03FF	8 bytes	COM1
0080 - 008F	16 bytes	PIIX4 - DMA Page Register	04D0 - 04D1	2 bytes	Edge/level triggered
00A0 - 00A1	2 bytes	PIIX4 - Interrupt Controller 2	LPT + 400h	8 bytes	Extended Capabilities Port (ECP) Port, LPT + 400h
00C0 - 00DE	31 bytes	PIIX4 - DMA 2	0CF8*	1 byte	PCI Configuration Address Register
00F0	1 byte	Reset Numeric Error	0CF9	1 byte	Turbo & Reset Control Registers
0170 - 0177	8 bytes	Secondary IDE Channel	0CFC-0CFF*	4 bytes	PCI Config Data Register
01F0 - 01F7	8 bytes	Primary IDE Channel			
0278 - 027B	4 bytes	LPT			
02F8 - 02FF	8 bytes	COM2			

* Only by DWORD accesses.

PCI Configuration Space Map

Table 8 PCI Configuration Space Map

Bus Number (hex)	Dev Number (hex)	Function Number (hex)	Description
00	00	00	Intel 82430TX
00	01	00	Intel 82371AB (PIIX4) PCI/ISA bridge
00	01	01	Intel 82371AB (PIIX4) IDE Bus Master
00	01	02	Intel 82371AB (PIIX4) USB
00	01	03	Intel 82371AB (PIIX4) Power management
00	0C	00	PCI Expansion Slot: 1
00	0B	00	PCI Expansion Slot: 2
00	0A	00	PCI Expansion Slot: 3
00	09	00	PCI Expansion Slot: 4

DMA Channels

Table 9 DMA Channels

DMA	Data Width	System Resource
0	8- or 16-bits	Available
1	8- or 16-bits	Parallel Port
2	8- or 16-bits	Floppy
3	8- or 16-bits	Parallel Port (for ECP*/EPP** Configuration)
4		Reserved - Cascade channel
5	16-bits	Available
6	16-bits	Available
7	16-bits	Available

* Extended Capabilities Port

** Enhanced Parallel Port

Interrupts

Table 10 Interrupts

IRQ	System Resource
NMI	I/O Channel Check
0	Reserved, Interval Timer
1	Reserved, Keyboard Buffer full
2	Reserved, Cascade Interrupt from Slave PIC
3	COM2
4	COM1
5	Free assigned by BIOS
6	Floppy
7	LPT1*
8	Real Time Clock
9	Free assigned by BIOS
10	Free assigned by BIOS
11	Free assigned by BIOS
12	Onboard Mouse Port if present
13	Reserved, Math Coprocessor
14	Primary IDE if present, else user available
15	Secondary IDE if present, else user available

* Typical Configuration (Plug and Play determined)

PCI Interrupt Routing Map

The PCI specification allows for sharing of interrupts between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the normal operation or throughput of the devices. However, in some special cases where maximum performance is needed from a device, you may want to ensure that it does not share an interrupt with other PCI devices.

This section describes the interrupt sharing mechanism and how the interrupt signals are connected between the motherboard's PCI expansion slots and onboard PCI devices. Use this information to avoid sharing an interrupt for a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- INTA: By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- INTB: Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- INTC and INTD: Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The PIIX4 PCI-to-ISA bridge has four Programmable Interrupt Request (PIRQ) input signals. Any PCI interrupt source (either onboard or from a PCI add-in card) connects to one of these PIRQ signals. Because

there are only four signals, some PCI interrupt sources are mechanically tied together on the motherboard and therefore share the same interrupt.

BIOS and Setup Program

Introduction

The motherboard uses an Award BIOS, which is stored in flash memory and can be upgraded using a floppy disk-based program. In addition to the BIOS, the flash memory contains the Setup program, Power-on Self Tests (POST), Advanced Power Management (APM), the PCI auto-configuration utility, and Windows 95-ready Plug and Play. See Specifications section for the supported versions of these specifications.
This motherboard supports BIOS shadowing, allowing the BIOS to execute from 64-bit onboard write-protected DRAM.
The BIOS displays a sign-on message during POST identifying the type of BIOS and a revision code. The initial production BIOS on the motherboard is identified as 1.00.01.YM1.

BIOS Upgrades

Flash memory simplifies distributing BIOS upgrades. You can install a new version of the BIOS from a diskette. BIOS upgrades are available to be downloaded from the secure section on the Intel World Wide Web site.
The disk-based flash upgrade utility has two options for BIOS upgrades:

- Update the BIOS from a file on a disk
- Copy the current BIOS code from the flash memory to a disk file as a backup, in the event that an upgrade cannot be successfully completed

Plug and Play: PCI Auto-configuration

The PCI auto-configuration utility operates in conjunction with the Setup program to let you insert and remove PCI cards without user configuration (Plug and Play). When you turn on the computer after adding a PCI card, the BIOS automatically configures interrupts, I/O space, and other parameters. Any interrupts set to “No/ICU” in Setup are considered free for use by PCI add-in cards. PCI interrupts are distributed to available ISA interrupts that have not been assigned to an ISA card or to system resources. The assignment of PCI interrupts to ISA IRQs is nondeterministic. An ISA device cannot share an interrupt allocated to an add-in PCI card. PCI configuration information is stored in ESCD format. You can clear the ESCD data with the disk-based flash upgrade utility.For information about the version of PCI and Plug and Play supported by this BIOS, see Specifications section . You can obtain copies of the specifications from the Intel World Wide Web site. Peer-to-peer hierarchical PCI bridge is supported.

PCI IDE Support

If you select “Auto” in Setup, the BIOS automatically sets up the two local bus IDE connectors with independent I/O channel support. The IDE interface supports hard drives up to PIO Mode 4 and recognizes any ATAPI devices, including CD-ROM drives and tape drives (see Specifications section for the supported version of ATAPI). The BIOS determines the capabilities of each drive and configures them to optimize capacity and performance. To take advantage of the high capacities typically available today, hard drives are automatically configured for Logical Block Addressing (LBA) and to PIO Mode 3 or 4, depending on the capability of the drive. You can override the auto-configuration options by specifying User configuration in Setup. The ATAPI Specification recommends that ATAPI devices be configured as shown in Table 11.

Table 11 Recommendations for Configuring an ATAPI Device

	Primary Cable	Secondary Cable

	Drive 0	Drive 1	Drive 0	Drive 1
Normal, no ATAPI	ATA			
Disk and CD-ROM for enhanced IDE systems	ATA		ATAPI	
Legacy IDE system with only one cable	ATA	ATAPI		
Enhanced IDE system with a CD-ROM and a tape or two CD-ROMs	ATA		ATAPI	ATAPI

ISA Plug and Play

If you select No/ICU in Setup to boot with a Plug and Play OS, the BIOS auto-configures only ISA Plug and Play cards that are required for booting (initial program load devices). If you select to not boot with a Plug and Play OS, the BIOS auto-configures all Plug and Play ISA cards.

ISA Legacy Devices

Since ISA legacy devices are not auto-configurable, the resources for them must be reserved. You can reserve resources in the Setup program or with an ISA configuration utility.
The computer's configuration information is stored in ESCD format. You can clear the ESCD data by using the disk-based upgrade utility.

Desktop Management Interface

Desktop Management Interface (DMI) is a method of managing computers in an enterprise. The main component of DMI is the Management Information Format (MIF) database, which contains information about the computer and its components. Using DMI, a system administrator can obtain the system types, capabilities, operational status, installation date, and other information about the computer's components. The DMI specification requires that certain information about the computer's motherboard be made available to an applications program. This information is located in a series of data structures which are accessed in various ways by the DMI service layer. Component instrumentation allows the service layer to gain access to information stored in the general-purpose area of non-volatile RAM. The MIF database defines the data and provides the method for accessing the information.
The BIOS support for DMI enables the maximum benefit from applications such as LANDesk Client Manager from Intel. The BIOS stores and can report on the following types of DMI information:

- BIOS data, such as the BIOS revision level
- Fixed information, such as data about the motherboard, peripherals, serial numbers and asset tags, etc.
- Information discovered during bootup, such as memory size, cache size, processor speed, etc.
- Dynamic information, such as event detection

An OEM can use a utility that makes DMI calls to program system and chassis-related information into the Flash memory, so the BIOS can also report that information. Once this information is written, it is locked (read-only).
Intel can provide a utility for making DMI calls to the BIOS. The latest DMI specification is available from Intel and other sites.
DMI does not work directly under non-Plug and Play operating systems (e.g., Windows NT). However, the BIOS supports a DMI table interface for such operating systems. Using this support, a DMI service-level application running on a non-Plug and Play OS can access the DMI BIOS information.

Advanced Power Management

The BIOS supports Advanced Power Management (APM); see Specifications section for the version supported. You can initiate the energy saving Standby mode in these ways:

- Optional front panel Sleep/Resume button

- Prolonged inactivity; the timeout period is adjustable in the Setup program

When in Standby mode, the motherboard reduces power consumption by using the processor's System Management Mode (SMM) capabilities and by spinning down hard drives.
While in Standby mode, the computer retains the ability to respond to external interrupts; it can service requests such as incoming faxes or network messages while unattended. Any keyboard or mouse activity brings the computer out of Standby mode and immediately restores power to the monitor.
APM is enabled in the BIOS by default; however, the computer must be configured with an OS-dependent APM driver for the power-saving features to take effect. For example, Windows 95 enables APM automatically upon detecting the presence of the APM BIOS.

Boot Options

Booting from CD-ROM is supported in adherence to the "El Torito" bootable CD-ROM format specification developed by Phoenix Technologies and IBM. Under the Boot Screen field in Setup, CD-ROM is one of four possible boot devices, which are defined in priority order. The default settings are:

- First boot device - Hard drive
- Second boot device - Removable devices (floppy drive)

NOTE

A copy of the "El Torito" specification is available on the Phoenix Technologies Web site http://www.ptltd.com/techs/specs.html.

USB Support

The USB connectors on the USB / PS/2 mouse connector card allow you to attach any of several USB devices as they become available. Typically, the device driver for USB devices will be managed by the OS.

Specifications

The motherboard complies with the following specifications:

Table 12 Compliance with Specifications

Specification	Description	Revision Level
APM	Advanced Power Management BIOS interface specification	Revision 1.2, February, 1996 Intel, Microsoft
ATA-33	Synchronous DMA Transfer Protocol specification (to be proposed as Ultra DMA/33 standard)	Revision 0.7, May 21, 1996 Quantum document no. 70-108412-1
DMI	Desktop Management Interface BIOS specification	Version 2.0, October 16, 1995 American Megatrends Inc., Award Software International Inc., Dell Computer Corporation, Intel, Phoenix Technologies Ltd, SystemSoft Corporation
EPP	Enhanced Parallel Port	IEEE 1284 standard, Mode [1 or 2]
PCI	PCI Local Bus specification	Revision 2.1, June 1, 1995 PCI Special Interest Group
Plug and Play	Plug and Play BIOS specification	Version 1.0a, May 5, 1994 Compaq Computer Corp, Phoenix Technologies, Intel
UHCI	Universal Host Controller Interface	Revision 1.0
USB	Universal Serial Bus specification	Revision 1.0, January 15, 1996

		Compaq, Digital Equipment Corporation, IBM PC Company, Intel, Microsoft, NEC, Northern Telecom