Advanced/ATX Memory Map, I/O Map, IRQs and DMA

MEMORY MAP

Address Range (Decimal)	*Address Range (hex)*	*Size*	*Description*
1024K-131072K	100000-8000000	127M	Extended Memory
960K-1023K	F0000-FFFFF	64K	AMI System BIOS (not available for UMB)
952K-959K	EE000-EFFFF	8K	Main BIOS (Currently available as UMB)
948K-951K	ED000-EDFFF	4K	ESCD (Plug 'N' Play configuration area)
944-947K	EC000-ECFFF	4K	OEM LOGO (available as UMB)
896K-943K	E0000-EBFFF	47K	BIOS RESERVED (Currently available as UMB)
800-895K	C8000-DFFFF	96K	Available HI DOS memory (open to ISA and PCI bus)
640K-799K	A0000-C7FFF	160K	On-board video memory and BIOS
639K	9FC00-9FFFF	1K	Extended BIOS Data (moveable by QEMM, 386MAX)
512K-638K	80000-9FBFF	127K	Extended conventional
0K-511K	00000-7FFFF	512K	Conventional

Table C-1. Advanced/ATX Memory Map

The table above details the Advanced/ATX memory map. The ESCD area from ED000-EDFFF is not available for use as an Upper Memory Block (UMB) by memory managers. The area from E0000-EBFFF is currently not used by the BIOS and is available for use as UMB by memory managers. (Some memory managers may require the user to include the specific ranges.) Parts of this area may be used by future versions of the BIOS to add increased functionality.

I/O MAP

The following table lists the I/O addresses used by baseboard devices. Some of these devices (audio and graphics) may not be present in all configurations. Some devices (serial ports, parallel ports etc.) may be configured for various addresses or disabled. These I/O locations are listed in the Variable Baseboard Resources column. Note: the Crystal audio controller is a plug and play device, only standard audio addresses are listed below.

Address (hex)	*Size*	*Fixed Baseboard Resources*	*Variable Baseboard Resources*
0000 – 000F	16 bytes	PIIX - DMA 1	
0020 – 0021	2 bytes	PIIX - Interrupt Controller 1	
002E – 002F	2 bytes	Ultra I/O configuration registers	
0040 – 0043	4 bytes	PIIX - Timer 1	
0060	1 byte	Keyboard Controller Data Byte	
0061	1 byte	PIIX - NMI, speaker control	
0064	1 byte	Kbd Controller, CMD/STAT Byte	
0070, bit 7	1 bit	PIIX - Enable NMI	
0070, bits 6:0	7 bits	87C307PIIX - Real Time Clock,	
0071	1 byte	87C307PIIX - Real Time Clock,	
0078	1 byte	Reserved - Brd. Config.	
0079	1 byte	Reserved - Brd. Config.	
0080 – 008F	16 bytes	PIIX - DMA Page Register	
00A0 – 00A1	2 bytes	PIIX - Interrupt Controller 2	
00B2 – 00B3	2 bytes	PIIX - APM	
00C0 – 00DE	31 bytes	PIIX - DMA 2	
00F0	1 byte	Reset Numeric Error	
0170 – 0177	8 bytes		Secondary IDE Channel
01F0 - 01F7	8 bytes		Primary IDE Channel
0200 – 0207	8 bytes		Gameport Joystick
0220 – 022F	16 bytes		Audio - WSS
0270 – 0273	4 bytes	I/O read port for Plug and Play	
0278 – 027B	4 bytes		Parallel Port 2

Table D-1 Advanced/ATX I/O Address Map (continued on next page)

I/O ADDRESS MAP (CONTINUED)

Address (hex)	*Size*	*Fixed Baseboard Resources*	*Variable Baseboard Resources*
02E8 – 02EF	8 bytes		Serial Port 4
02F8 - 02FF	8 bytes		Serial Port 2
0330 - 0331	2 bytes		Audio - MUP-401
0376	1 byte		Sec IDE Chan Cmd Port
0377	1 byte		Sec IDE Chan Stat Port
0378 - 037F	8 bytes		Parallel Port 1
0388 - 038B	4 bytes		Audio - WSS
03B0 - 03BB	4 bytes		S3 Trio64V+
03BC - 03BF	4 bytes		Parallel Port 3 (add-in device)
03C0 - 03DF	16 bytes		S3 Trio64V+
03E8 - 03EF	8 bytes		Serial Port 3
03F0 - 03F5	6 bytes		Floppy Channel 1
03F6	1 bytes		Pri IDE Chan Cmnd Port
03F7 (Write)	1 byte		Floppy Chan 1 Cmd
03F7, bit 7	1 bit		Floppy Disk Chg Chan 1
03F7, bits 6:0	7 bits		Pri IDE Chan Status Port
03F8 - 03FF	8 bytes		Serial Port 1
LPT + 400h	3 bytes		ECP regs, LPT base + 400h
4D0 - 4D1	2 bytes	Edge/Level INTR Control Reg.	
608 - 60B	4 bytes		Audio - WSS
0CF8 - 0CFC*	4 bytes	PCI Config Address Reg.	
0CF9	1 byte	Turbo & Reset control Reg.	
0CFC - 0CFF	4 bytes	PCI Config Data Reg	
0F00 - 0F07	8 bytes		Audio - CS4232 support regs
FFA0 - FFA7	8 bytes		Primary Bus Master IDE regs
FFA8 - FFAF	8 bytes		Secondary Bus Master IDE
FF00-FF07	8 bytes		IDE Bus Master Reg.

Table D-1. Advanced/ATX I/O Address Map (*only accessible by DWORD accesses)

I/O Port 78 is reserved for BIOS use. Port 79 is a read only port, the bit definitions are shown below in Table D-2.

Bit #	*Description*	*Bit = 1*	*Bit = 0*
0	Reserved	n/a	n/a
1	Soft Off capable power supply present	No	Yes
2	On-bd Audio present	Yes	No
3	External CPU clock (Jumper 2)	Table B-2	Table B-2
4	External CPU clock (Jumper 1)	Table B-2	Table B-2
5	Setup Disable (Jumper 8)	Enable access	Disable access
6	Clear CMOS (Jumper 5)	Keep values	Clear values
7	Password Clear (Jumper 6)	Keep password	Clear password

Table D-2. Advanced/ATX Port 79 Definition

PCI CONFIGURATION SPACE MAP

The 82430FX chipset uses Configuration Mechanism 1 to access PCI configuration space. The PCI Configuration Address register is a 32-bit i/o register located at 0CF8h, the PCI Configuration Data register is a 32-bit i/o register located at 0CFCh. The PCI Configuration Address register is only accessible by a DWORD access, the PCI Configuration Data register is accessible by DWORD, WORD or BYTE accesses.

ACCESS TO I/O CONFIGURATION SPACE USING MECHANISM #1

1. Using a DWORD write command, output the desired I/O configuration address to I/O port CF8H

2. Using a DWORD read or write command, read or write data from the I/O port CFCH

NOTE: Any address output to CF8H is always on a 4 byte (DWORD) boundry. You can read or write any BYTE, WORD or DWORD in the four byte range by using the correct offset as follows:

DWORD @ CFCh

WORD @ CFCh or CFEh

BYTE @ CFCh, CFDh, CFEh or CFFh

CONFIGURATION ADDRESS REGISTER BIT DEFINITION

31	30 24	23 16	15 11	10 8	7 2	1	0
1	RESERVED	BUS NUMBER	DEVICE NUMBER	FUNCTION NUMBER	REGISTER NUMBER	0	0

CONFIG SPACE ENABLE FLAG (Bit 31): Always 1 to indicate I/O access is to configuration space.

RESERVED (Bits 30-24): Always 00h

BUS NUMBER (Bits 23-16): Always 00h unless a bridge card is installed in a PCI slot

DEVICE NUMBER (Bits 15-11): Used to indicate a specific PCI device. The TSC has a predefined device number of 00000h. The PIIX and four PCI slots also have specific device numbers, that device number is determined by which PCI Addess/Data line is connected to the device's ID SEL pin. Table E-1 details the specific mapping information.

FUNCTION NUMBER (Bits 10-8): Used to indicate a specific funtion in multifunction PCI devices. The PIIX is the only multi-function device on ADVANCED/ATX located on the baseboard. Use 00h for the basic PIIX device and 01h for the PCI IDE BUS MASTER FUNCTION. For a multi-function PCI add-in card, refer to the card's documentation to determine the allowable function numbers.

REGISTER NUMBER (Bits 7-2): Defines one of 64 DWORD locations for a specific PCI device.

Note that Bits 1 and 0 must always be 0h for DWORD access.

The table below lists the PCI bus and device numbers used by the baseboard. It also lists the data range that must be written to the I/O Configuration Address register to access the device.

DEVICE	*BUS/DEVICE/FUNCTION*	*ID SEL*	*I/O CONFIG ADDRESS REGISTER*
TSC	00/00/0	N/A	8000 0000 - 8000 00FC
PIIX	00/07/0	AD18	8000 3800 - 8000 38FC
PIIX-IDE BUS MASTER	00/07/1	AD18	8000 3900 - 8000 39FC
S3 Trio 64V+	00/08/0	AD19	8000 4000 - 8000 40FC
PCI SLOT 1 (closest to ISA slots)	00/0D/0	AD24	8000 6800 - 8000 68FC
PCI SLOT 2	00/0E/0	AD25	8000 7000 - 8000 70FC
PCI SLOT 3	00/0F/0	AD26	8000 7800 - 8000 78FC
PCI SLOT 4 (farthest from ISA slots)	00/10/0	AD27	8000 8000 - 8000 80FC

Table E-1. Advanced/ATX PCI Configuration. Space Map

INTERRUPTS & DMA CHANNELS

The following tables list the Interrupt and DMA Channel configuration options for on-board devices. The serial ports, parallel ports, and IDE controller can be configured via SETUP, the ICU, or any other Plug and Play resource manager (such as the Windows 95 Device Manager). The Audio controller can only be configured via a Plug and Play resource manager. The Graphics interupt is assigned by the auto-configure utility during boot up.

IRQ	*Reserved Interrupts*	*Serial Port 1*	*Serial Port 2*	*Parallel Port*	*IDE*	*Audio*	*Graphics*
NMI	I/O Channel Check						
0	Interval Timer						
1	Keyboard buffer full						
2	Cascade interrupt from slave PIC						
3		X	X				X
4		X	X				X
5				X		X	X
6	Floppy Controller						
7				X		X	X
8							X
9						X	X
10							X
11							X
12	PS/2 Mouse (if present)						
13	Math co-processor						
14					X		
15					X		

Table F-1. Advanced/ATX Interrupts

DMA	*Reserved*	*Paralllel Port*	*Audio*
0			X
1			X
2	Floppy		
3		X	
4	Cascade channel		
5			
6			
7			

Table F-2. Advanced/ATX DMA Map